REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																			
SHEET																			
REV																			
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33

REV STATUS OF SHEETS	REV															
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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DRAWING APPROVAL DATE
98-01-06

REVISION LEVEL

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216

MICROCIRCUIT, MEMORY, DIGITAL, CMOS
512 X 36 X 2 CLOCKED FIFO, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-95628**

SHEET 1 OF 33

DSCC FORM 2233
APR 97

5962-E137-98

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

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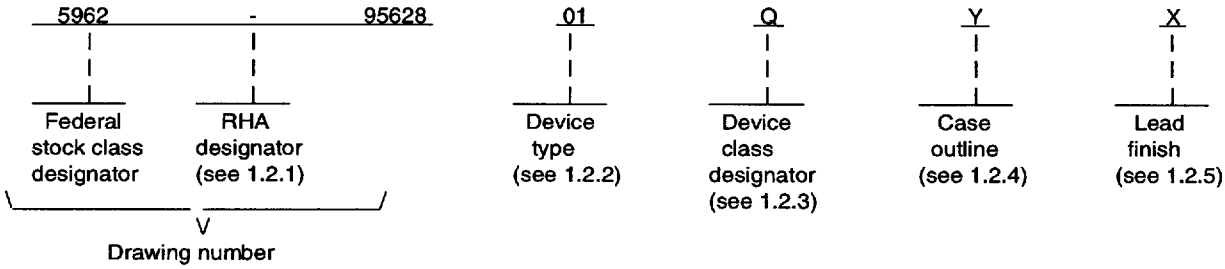
1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	ACT3632	512 X 36 X 2 clocked FIFO

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
Y	See figure 1	132	Ceramic quad flat package

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/ 2/ 3/

Supply voltage range (V_{CC})	-0.5 V dc to +7.0 V dc
DC input voltage range (I/O ports) (V_{IN})	-0.5 V dc to V_{CC} + 0.5 V dc 4/
DC output voltage range (V_{OUT})	-0.5 V dc to V_{CC} + 0.5 V dc 4/
DC output current (I_O) (per output)(V_O = 0.0 V to V_{CC})	±50 mA
DC input clamp current (I_{IK}) (V_{IN} < 0.0 V or V_{IN} > V_{CC})	±20 mA
DC output clamp current (I_{OK}) (V_{OUT} < 0.0 V or V_{OUT} > V_{CC})	±50 mA
Storage temperature range (T_{STG})	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (Θ_{JC})	2.0°C/W
Junction temperature (T_J)	+150°C
Maximum power dissipation (P_D) at T_A = +55°C in still air	1.8 W 5/
V_{CC} current (I_{VCC})	±400 mA
Ground current (I_{GND})	±400 mA

1.4 Recommended operating conditions. 2/ 3/

Supply voltage range (V_{CC})	+4.5 V dc to +5.5 V dc
Maximum low level input voltage (V_{IL})	+0.8 V
Minimum high level input voltage (V_{IH})	+2.0 V
Maximum high level output current (I_{OH})	-4.0 mA
Maximum low level output current (I_{OL})	+8.0 mA
Case operating temperature range (T_C)	-55°C to +125°C

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	XX percent 6/

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Interface Standard for Microcircuit Case Outlines.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Unless otherwise noted, all voltages are referenced to GND.
3/ The limits for the parameters specified herein shall apply over the full specified V_{CC} range and case temperature range of -55°C to +125°C.
4/ The input negative voltage rating may be exceeded provided that the input clamp current rating is observed.
5/ The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
6/ Values will be added when they become available.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table(s). The truth table(s) shall be as specified on figure 3.

3.2.4 Block or logic diagram(s). The block or logic diagram(s) shall be as specified on figure 4.

3.2.5 Test circuit and switching waveforms. The test circuit and switching waveforms shall be as specified on figures 5 and 6.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

TABLE I. Electrical performance characteristics.

Test	Symbol	Test conditions 1/ $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified			Device types	Group A subgroups	Limits 2/		Unit
							Min	Max	
High level output voltage	V_{OH}	For all inputs affecting output under test, V_{IN} = 2.0 V or 0.8 V, I_{OH} = -4.0 mA, V_{CC} = 4.5 V			01	1, 2, 3	2.4		V
Low level output voltage	V_{OL}	For all inputs affecting output under test, V_{IN} = 2.0 V or 0.8 V, I_{OL} = 8 mA, V_{CC} = 4.5 V			01	1, 2, 3		0.5	V
Input current	I_I 3/	For input under test, $V_I = V_{CC}$ or GND, V_{CC} = 5.5 V			01	1, 2, 3		±5	µA
Three-state output leakage current high	I_{OZH} 4/	$V_{OUT} = V_{CC}$, V_{CC} = 5.5 V			01	1, 2, 3		5	µA
Three-state output leakage current low	IOZL 4/	V_{OUT} = GND, V_{CC} = 5.5 V			01	1, 2, 3		-5	µA
Quiescent supply current, outputs high	I_{CC}	For all inputs, Output = port B, I_{OUT} = 0A, V_{CC} = 5.5 V, $V_{IN} = V_{CC}$ -0.2 V or GND			01	1, 2, 3		400	µA
Quiescent supply current, delta	ΔI_{CC}	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND.	$\overline{CSA} = V_{IH}$	A0-A35	01	1, 2, 3	0		mA
			$\overline{CSB} = V_{IH}$	B0-B35			0		
			$\overline{CSA} = V_{IL}$	A0-A35				1	
			$\overline{CSB} = V_{IL}$	B0-B35				1	
			All other inputs					1	
Input capacitance	C_{IN}	See 4.4.1e, V_I = 0			01	4		7	pF
I/O capacitance	C_{OUT}	See 4.4.1e, V_O = 0				4		10	
Functional tests	5/	V_{IH} = 2.0 V, V_{IL} = 0.8 V, verify output V_O, V_{CC} = 4.5 V and 5.5 V, 4.4.1c			01	7, 8A, 8B	L	H	
Clock frequency CLKA or CLKB	f_{clock}	C_L = 20 pF minimum, V_{CC} = 4.5 V and 5.5 V, see figures 5 and 6 as applicable			01	9, 10, 11		50	MHz
Clock cycle time CLKA or CLKB	t_c				01	9, 10, 11	20		ns
Pulse duration, CLKA and CLKB high or low	t_w				01	9, 10, 11	8		
Setup time, A0-A35 before CLKA↑, and B0-B35 before CLKB↑	$t_{su(D)}$				01	9, 10, 11	5		
Setup time, $\overline{CSA}$, W/$\overline{RA}$, ENA and MBA before CLKA↑; $\overline{CSB}$, $\overline{W}$/RB, MBB and ENB before CLKB↑	$t_{su(EN)}$				01	9, 10, 11	5		
Setup time, $\overline{RST\ 1}$ or $\overline{RST\ 2}$ low before CLKA↑ or CLKB↑	$t_{su(RS)}$ 6/				01	9, 10, 11	6		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified	Device types	Group A subgroups	Limits 2/		Unit
					Min	Max	
Setup time, FS0 and FS1 before $\overline{RST1}$ and $\overline{RST2}$ high	$t_{su(FS)}$	C_L = 20 pF minimum, V_{CC} = 4.5 V and 5.5 V, See figures 5 and 6 as applicable	01	9, 10, 11	8.5		ns
Hold time, A0-A35 after CLKA↑ and B0-B35 after CLKB↑	$t_{h(D)}$		01	9, 10, 11	1		
Hold time, $\overline{CSA}$, W/$\overline{RA}$, ENA and MBA after CLKA↑ and $\overline{CSB}$, W/$\overline{RB}$, MBB and ENB after CLKB↑	$t_{h(EN)}$		01	9, 10, 11	1		
Hold time, $\overline{RST1}$ or $\overline{RST2}$ low after CLKA↑ or CLKB↑	$t_{h(RS)}$ 6/		01	9, 10, 11	4		
Hold time, FS0 and FS1 after $\overline{RST1}$ and $\overline{RST2}$ high	$t_{h(FS)}$		01	9, 10, 11	3		
Skew time, between CLKA↑ and CLKB↑ for ORA, ORB, IRA, and IRB	$t_{sk(1)}$ 7/		01	9, 10, 11	9		
Skew time, between CLKA↑ and CLKB↑ for $\overline{AEA}$, $\overline{AEB}$, $\overline{AFA}$, and $\overline{AFB}$	$t_{sk(2)}$ 7/		01	9, 10, 11	16		
Access time, CLKA↑ to A0-A35 and CLKB↑ to B0-B35	t_a		01	9, 10, 11	3	15	
Propagation delay time, CLKA↑ to IRA and CLKB↑ to IRB	$t_{pd(C-IR)}$		01	9, 10, 11	2	10	
Propagation delay time, CLKA↑ to ORA and CLKB↑ to ORB	$t_{pd(C-OR)}$		01	9, 10, 11	1	10	
Propagation delay time, CLKA↑ to $\overline{AEA}$ and CLKB↑ to $\overline{AEB}$	$t_{pd(C-AE)}$		01	9, 10, 11	1	10	
Propagation delay time, CLKA↑ to $\overline{AFA}$ and CLKB↑ to $\overline{AFB}$	$t_{pd(C-AF)}$		01	9, 10, 11	1	10	
Propagation delay time, CLKA↑ to $\overline{MBF1}$ low or $\overline{MBF2}$ high and CLKB↑ to $\overline{MBF2}$ low or $\overline{MBF1}$ high	$t_{pd(C-MF)}$		01	9, 10, 11	0	10	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified	Device types	Group A subgroups	Limits 2/		Unit
					Min	Max	
Propagation delay time, CLKA↑ to B0-B35↑ 8/ and CLKB↑ to A0-A35↑ 9/	$t_{pd(C-MR)}$	C_L = 20 pF minimum, V_{CC} = 4.5 V and 5.5 V, See figures 5 and 6 as applicable	01	9, 10, 11	3	18.7	ns
Propagation delay time, MBA to A0-A35 valid and MBB to B0-B35 valid	$t_{pd(M-DV)}$		01	9, 10, 11	3	13	
Propagation delay time, $\overline{RST1}$ low to $\overline{AEB}$ low, $\overline{AFA}$ high, and $\overline{MBF1}$ high, and $\overline{RST2}$ low to $\overline{AEA}$ low, $\overline{AFB}$ high, and $\overline{MBF2}$ high	$t_{pd(R-F)}$		01	9, 10, 11	1	20	
Enable time, $\overline{CSA}$ and W/$\overline{RA}$ low to A0-A35 active and $\overline{CSB}$ low and $\overline{W}$/RB high to B0-B35 active	t_{en}		01	9, 10, 11	2	18	
Disable time, $\overline{CSA}$ or W/$\overline{RA}$ high to A0-A35 at high impedance and $\overline{CSB}$ high or $\overline{W}$/RB low to B0-B35 at high impedance	t_{dis}		01	9, 10, 11	1	13	

1/ Each input/output, as applicable, shall be tested at the specified temperature, for the specified limits, to the tests in table I herein. Output terminals not designated shall be high level logic, low level logic, or open, except for all I_{CC} tests, where the output terminals shall be open. When performing these tests, the current meter shall be placed in the circuit such that all current flows through the meter. For input terminals not designated, V_{IN} = GND or $V_{IN} \ge 3.0$ V.

2/ For negative and positive voltage and current values, the sign designates the potential difference in reference to GND and the direction of current flow, respectively, and the absolute value of the magnitude, not the sign, is relative to the minimum and maximum limits, as applicable, listed herein.

3/ For I/O ports, the limit includes I_I leakage current from the input circuitry.

4/ For I/O ports, the limit includes I_{OZH} or I_{OZL} leakage current from the output circuitry. This test is guaranteed when the control inputs affecting the output under test are at 2.0 V or 0.8 V.

5/ Tests shall be performed in sequence, attributes data only. Functional tests shall include the truth table and other logic patterns used for fault detection. The test vectors used to verify the truth table shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth table in figure 3 herein. Functional tests shall be performed in sequence as approved by the qualifying activity on qualified devices. After incorporating allowable tolerances per MIL-STD-883, V_{IL} = 0.4 V and V_{IH} = 2.4 V. For outputs, L ≤ 0.8 V, H ≥ 2.0 V.

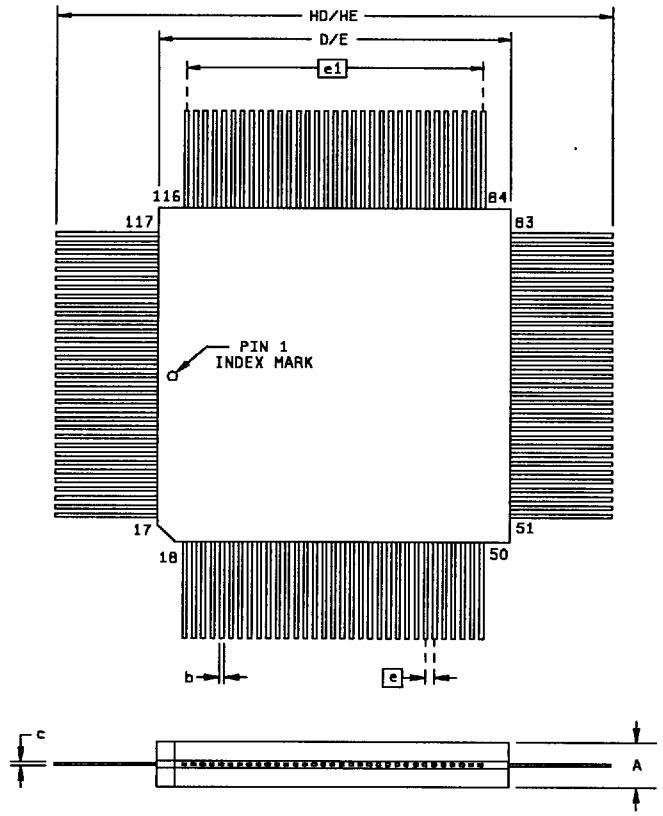
6/ Requirements to count the clock edge as one of at least four needed to reset the FIFO.

7/ Skew time is not a timing constraint for proper device operation and is only included to illustrate the timing relationship between CLKA cycle and CLKB cycle. This parameter is guaranteed, but not tested.

8/ Writing data to the mail1 register when the B0-B35 outputs are active and MBB is high.

9/ Writing data to the mail2 register when the A0-A35 outputs are active and MBA is high.

Case outline Y (see notes 1, 2, 3 and 4)



Symbol	Inches		Millimeters		Symbol	Inches		Millimeters	
	Min	Max	Min	Max		Min	Max	Min	Max
A	0.110	0.150	2.79	3.81	HD/HE	1.460	1.540	37.08	39.12
b	0.008	0.014	0.20	0.36	e	0.025		0.635	
c	0.004	0.008	0.10	0.20	e1	0.800		20.32	
D/E	0.935	0.965	23.75	24.51	N	132			

Notes: 1. Although dimensions are in inches, the US government preferred system of measurement is the metric SI system. However, since this item was originally designed using inch-pound units of measurement, in the event of conflict between the two, the inch-pound units shall take precedence. Metric equivalents are for general information only.
2. Terminal one shall be identified by a mechanical index in the lead or body, or a mark on the top surface.
3. Terminal identification numbers need not appear on the package.

FIGURE 1. Case outline.

Device type	01						
Case outline	Y						
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	FS1	34	B23	67	A0	100	A23
2	$\overline{RST2}$	35	B22	68	A1	101	A24
3	MBB	36	B21	69	A2	102	A25
4	$\overline{MBF1}$	37	B20	70	V_{CC}	103	A26
5	V_{CC}	38	B19			104	A27
		39	B18	71	A3	105	A28
6	$\overline{AEB}$	40	GND	72	A4	106	A29
7	$\overline{AFB}$	41	B17	73	A5	107	GND
8	ORB	42	B16	74	GND	108	A30
9	IRB	43	V_{CC}	75	A6	109	A31
10	GND			76	A7	110	V_{CC}
11	$\overline{CSB}$	44	B15	77	A8		
12	W/RB	45	B14	78	A9	111	A32
13	ENB	46	B13	79	A10	112	A33
14	CLKB	47	B12	80	A11	113	A34
15	V_{CC}	48	GND	81	GND	114	A35
		49	NC	82	NC	115	NC
16	NC	50	NC	83	NC	116	NC
17	NC	51	NC	84	NC	117	NC
18	NC	52	B11	85	A12	118	GND
19	B35	53	B10	86	V_{CC}	119	CLKA
20	B34	54	B9			120	ENA
21	B33	55	B8	87	A13	121	W/RA
22	B32	56	B7	88	A14	122	$\overline{CSA}$
23	GND	57	V_{CC}	89	A15	123	IRA
24	B31			90	A16	124	ORA
25	B30	58	B6	91	A17	125	V_{CC}
26	B29	59	GND	92	GND	126	$\overline{AFA}$
27	B28	60	B5	93	A18	127	$\overline{AEA}$
28	B27	61	B4	94	A19	128	$\overline{MBF2}$
29	B26	62	B3	95	A20	129	MBA
30	V_{CC}	63	B2	96	A21	130	$\overline{RST1}$
		64	B1	97	V_{CC}	131	FS0
31	B25	65	B0			132	GND
32	B24	66	GND	98	A22		
33	GND			99	GND		

FIGURE 2. Terminal connections.

Flag Programming

FS1	FS0	$\overline{RST1}$	$\overline{RST2}$	X1 AND Y1 REGISTERS	X2 AND Y2 REGISTERS
H	H	↑	X	64	X
H	H	X	↑	X	64
H	L	↑	X	16	X
H	L	X	↑	X	16
L	H	↑	X	8	X
L	H	X	↑	X	8
L	L	↑	↑	Programmed from port A	Programmed from port A

NOTE: X1 register holds the offset for $\overline{AEB}$; Y1 register holds the offset for $\overline{AFA}$;
X2 register holds the offset for $\overline{AEA}$; Y2 register holds the offset for $\overline{AFB}$.

Port-A Enable Function

$\overline{CSA}$	W/$\overline{RA}$	ENA	MBA	CLKA	A0-A35 OUTPUTS	PORT FUNCTION
H	X	X	X	X	In high-impedance state	None
L	H	L	X	X	In high-impedance state	None
L	H	H	L	↑	In high-impedance state	FIFO1 write
L	H	H	H	↑	In high-impedance state	Mail1 write
L	L	L	L	X	Active, FIFO2 output register	None
L	L	H	L	↑	Active, FIFO2 output register	FIFO2 read
L	L	L	H	X	Active, mail2 register	None
L	L	H	H	↑	Active, mail2 register	Mail2 read (set $\overline{MBF2}$ high)

FIGURE 3. Truth tables.

Port-B Enable Function

$\overline{CSB}$	$\overline{W}$/RB	ENB	MBB	CLKB	B0-B35 OUTPUTS	PORT FUNCTION
H	X	X	X	X	In high-impedance state	None
L	L	L	X	X	In high-impedance state	None
L	L	H	L	↑	In high-impedance state	FIFO2 write
L	L	H	H	↑	In high-impedance state	Mail2 write
L	H	L	L	X	Active, FIFO1 output register	None
L	H	H	L	↑	Active, FIFO1 output register	FIFO1 read
L	H	L	H	X	Active, mail1 register	None
L	H	H	H	↑	Active, mail1 register	Mail1 read (set $\overline{MBF1}$ high)

FIFO1 and FIFO2 flag operation

NUMBER OF WORDS IN FIFO1 1/ 2/	SYNCHRONIZED TO CLKB		SYNCHRONIZED TO CLKA		NUMBER OF WORDS IN FIFO2 2/ 3/	SYNCHRONIZED TO CLKA		SYNCHRONIZED TO CLKB	
	ORB	$\overline{AEB}$	$\overline{AFA}$	IRA		ORA	$\overline{AEA}$	$\overline{AFB}$	IRB
0	L	L	H	H	0	L	L	H	H
1 to X1	H	L	H	H	1 to X2	H	L	H	H
(X1+1) to [512 - (Y1+1)]	H	H	H	H	(X2+1) to [512 - (Y2+1)]	H	H	H	H
(512-Y1) to 511	H	H	L	H	(512-Y2) to 511	H	H	L	H
512	H	H	L	L	512	H	H	L	L

1/ X1 is the almost-empty offset for FIFO1 used by $\overline{AEB}$. Y1 is the almost-full offset for FIFO1 used by $\overline{AFA}$ Both X1 and Y1 are selected during a reset of FIFO1 or programmed from port A.
2/ When a word loaded to an empty FIFO is shifted to the output register, its previous FIFO memory location is free.
3/ X2 is the almost-empty offset for FIFO2 used by $\overline{AEA}$. Y2 is the almost-full offset for FIFO2 used by $\overline{AFB}$. Both X2 and Y2 are selected during a reset of FIFO2 or programmed from port A.

FIGURE 3. Truth tables - continued.

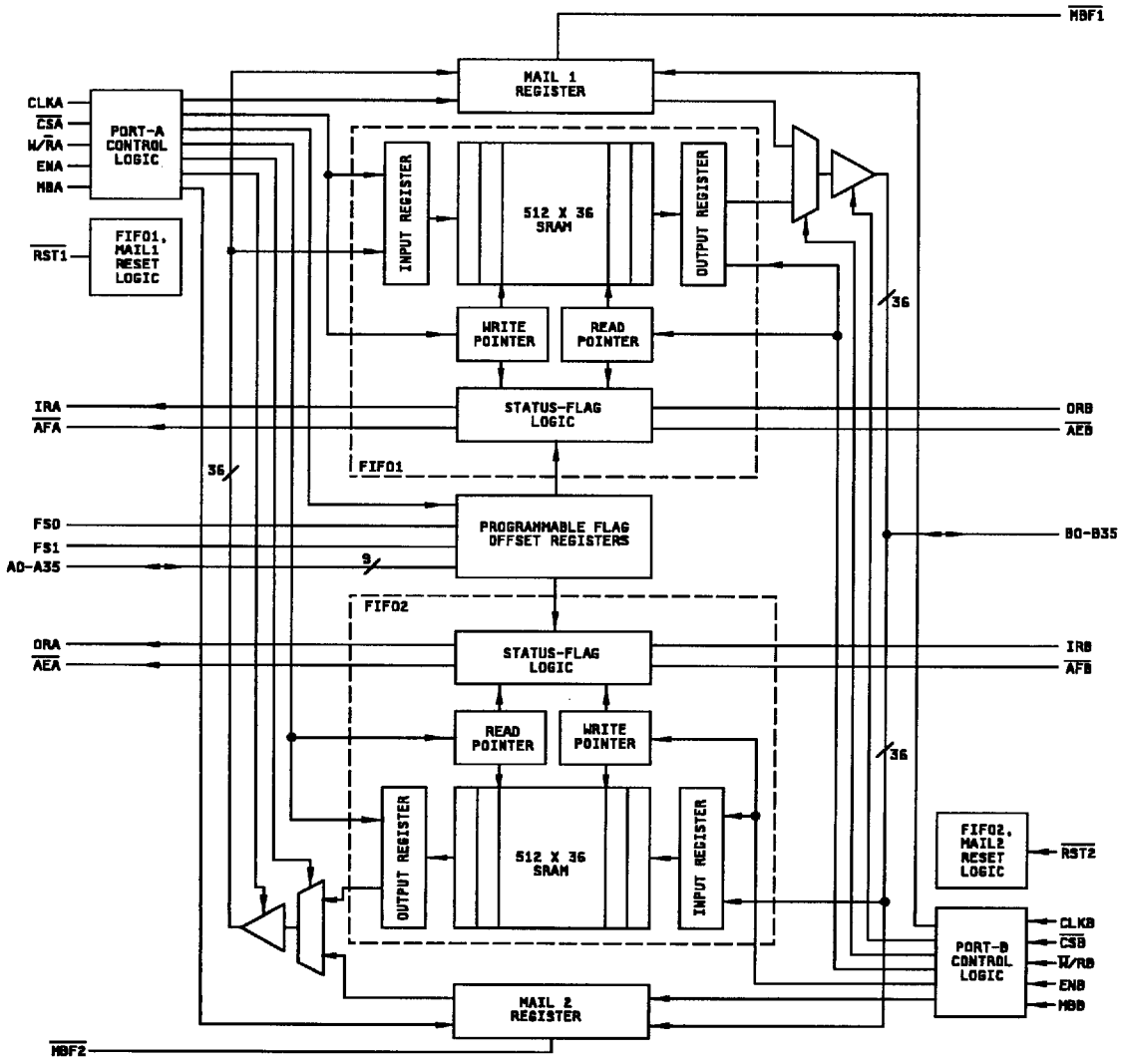
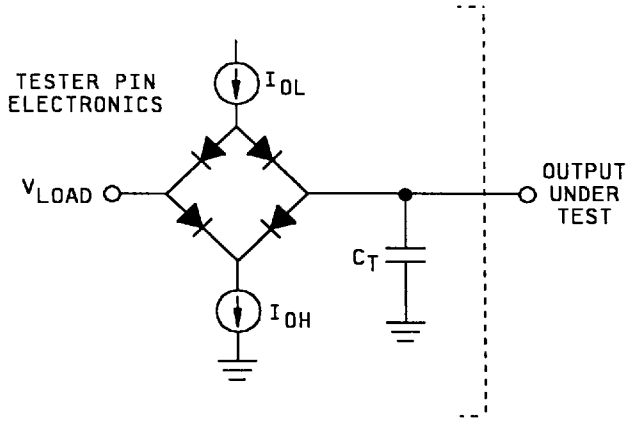
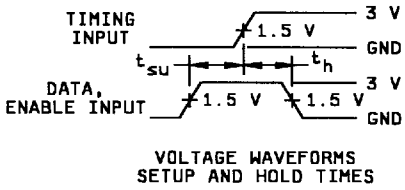


FIGURE 4. Block diagram.

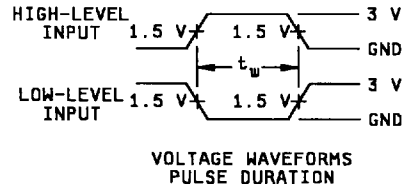
STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-95628
		REVISION LEVEL	SHEET 12



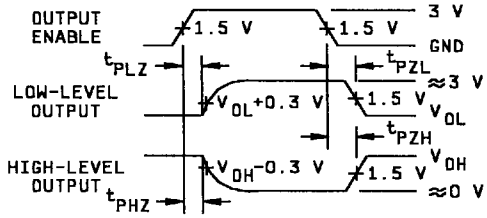
NOTE: I_{OL} = 8 mA (all outputs), I_{OH} = -4 mA (all outputs), and V_{LOAD} = 20 pF minimum load circuit capacitance.



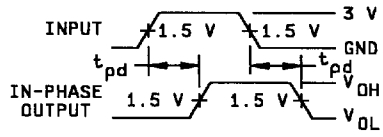
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



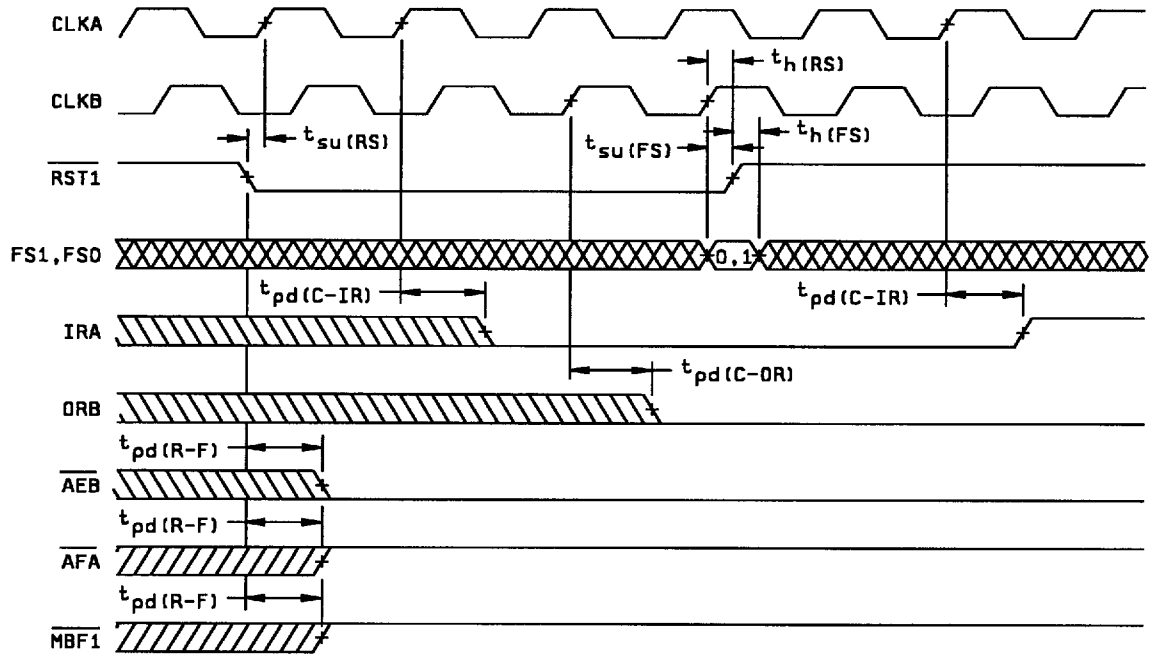
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

FIGURE 5. Test load circuit and voltage timing waveforms.

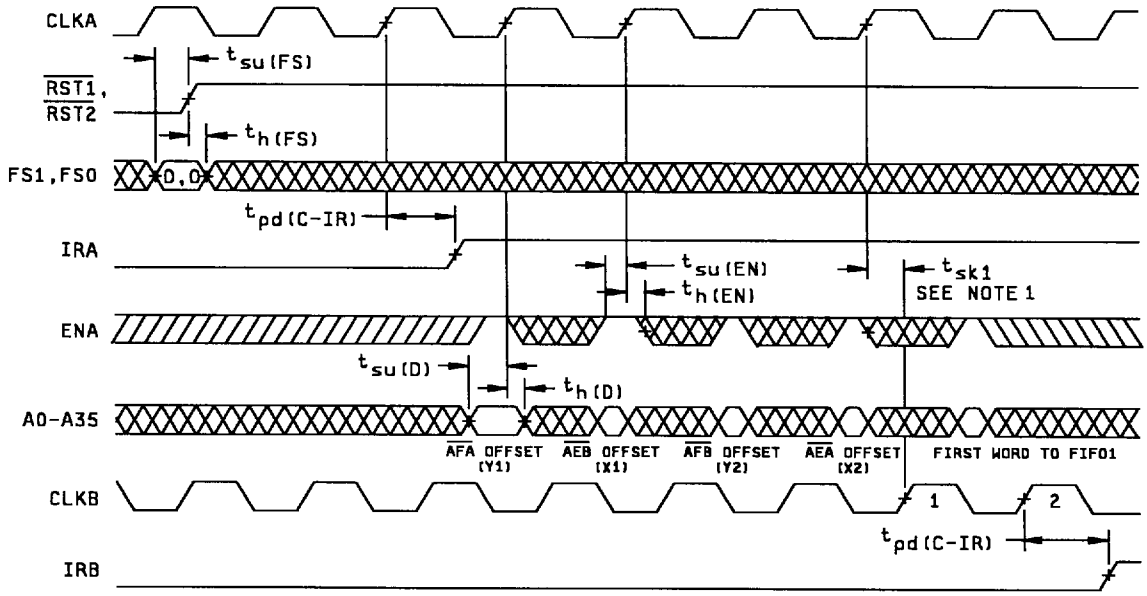
FIFO1 RESET LOADING X1 AND Y1 WITH A PRESET VALUE OF EIGHT



NOTE: FIFO2 is reset in the same manner to load X2 and Y2 with a preset value.

FIGURE 6. Timing waveforms - Continued.

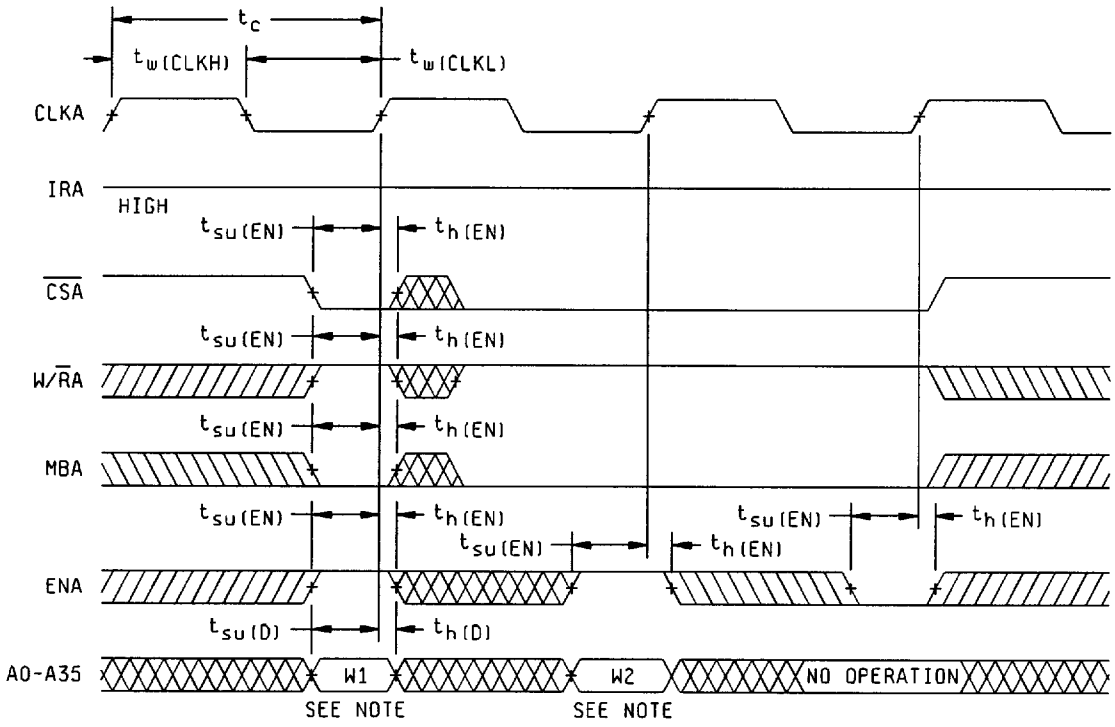
PROGRAMMING THE ALMOST FULL FLAG AND ALMOST-EMPTY FLAG OFFSET VALUES AFTER RESET



NOTES: 1. t_{sk1} is the minimum time between a rising CLKA edge and a rising CLKB edge for IRB to transition high in the next CLKB cycle. If the time between CLKA edge and rising CLKB edge is less than t_{sk1}, then IRB may transition high one cycle later than shown.
2. $\overline{CSA}$ = L, W/$\overline{RA}$ = H, MBA = L. It is not necessary to program offet register on consecutive clock cycles.

FIGURE 6. Timing waveforms - Continued.

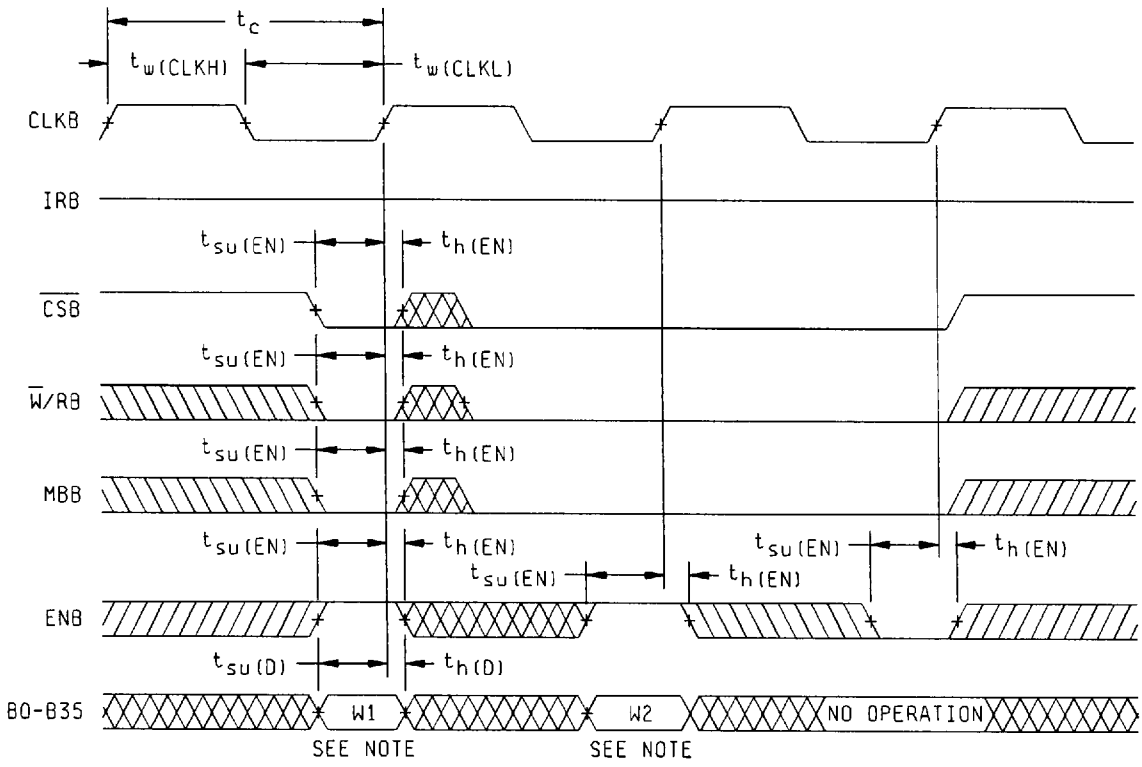
PORT-A WRITE CYCLE TIMING FOR FIFO1



NOTE: Written to FIFO1.

FIGURE 6. Timing waveforms - Continued.

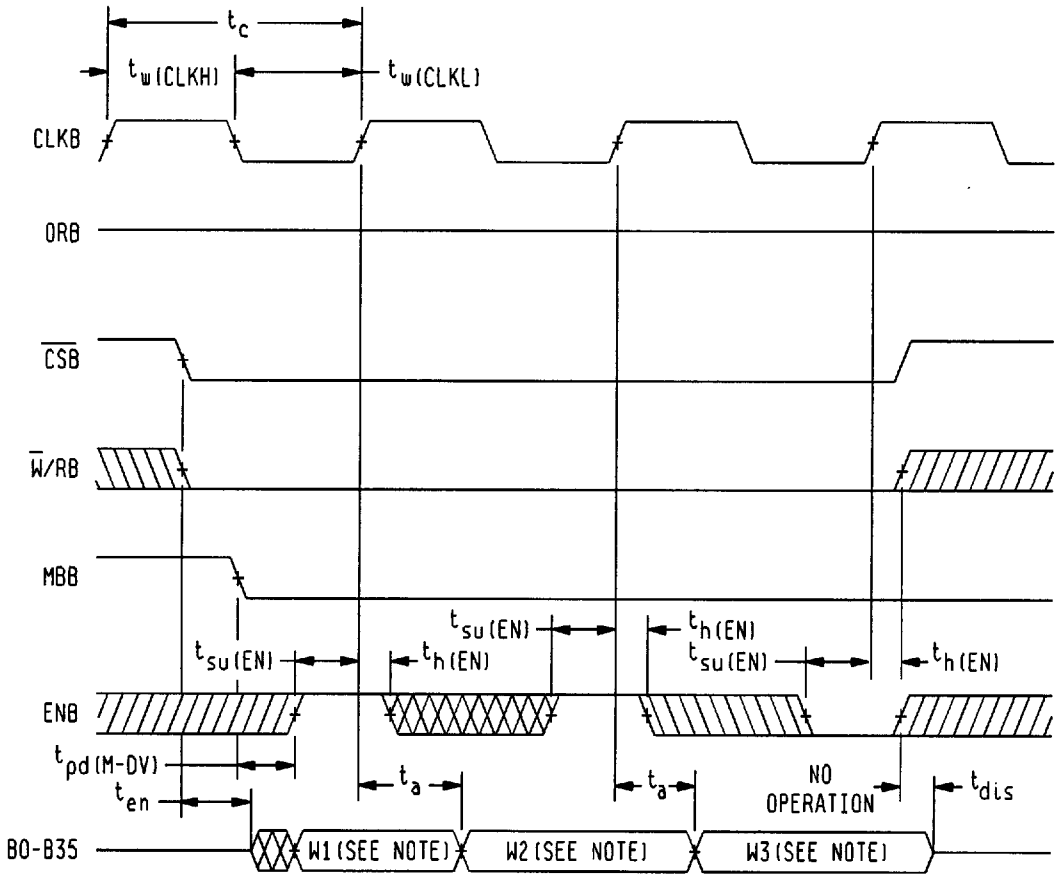
PORT-B WRITE CYCLE TIMING FOR FIFO2



NOTE: Written to FIFO2.

FIGURE 6. Timing waveforms - Continued.

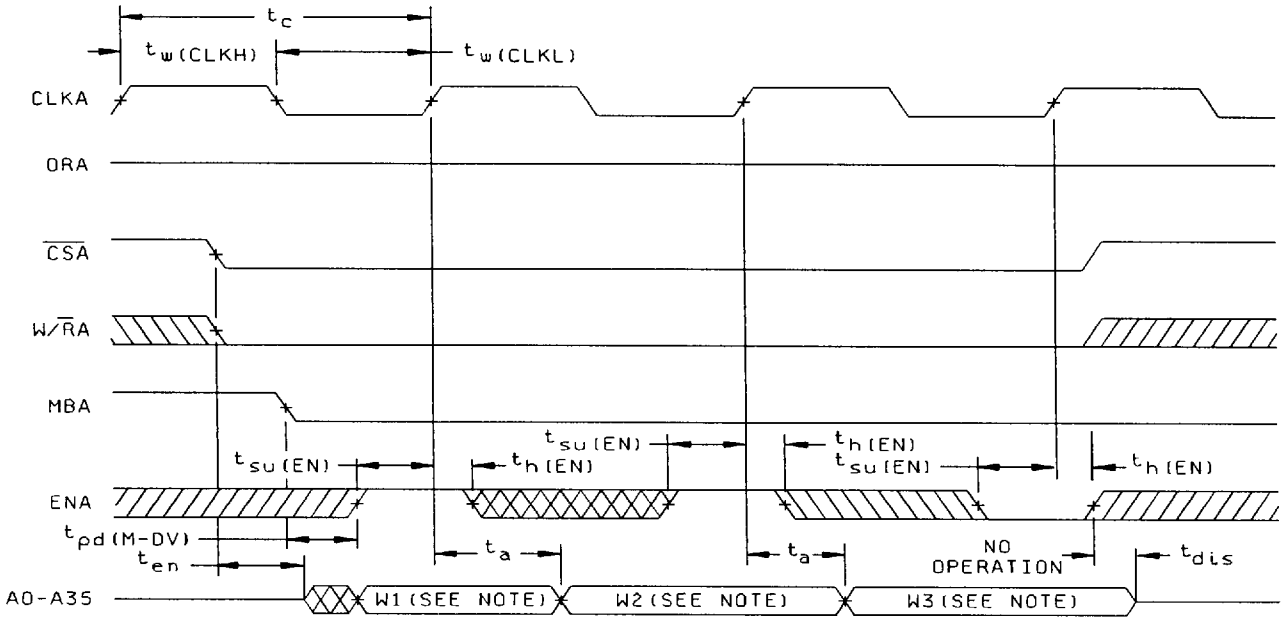
PORT-B READ CYCLE TIMING FOR FIFO1



NOTE: Read from FIFO1.

FIGURE 6. Timing waveforms - Continued.

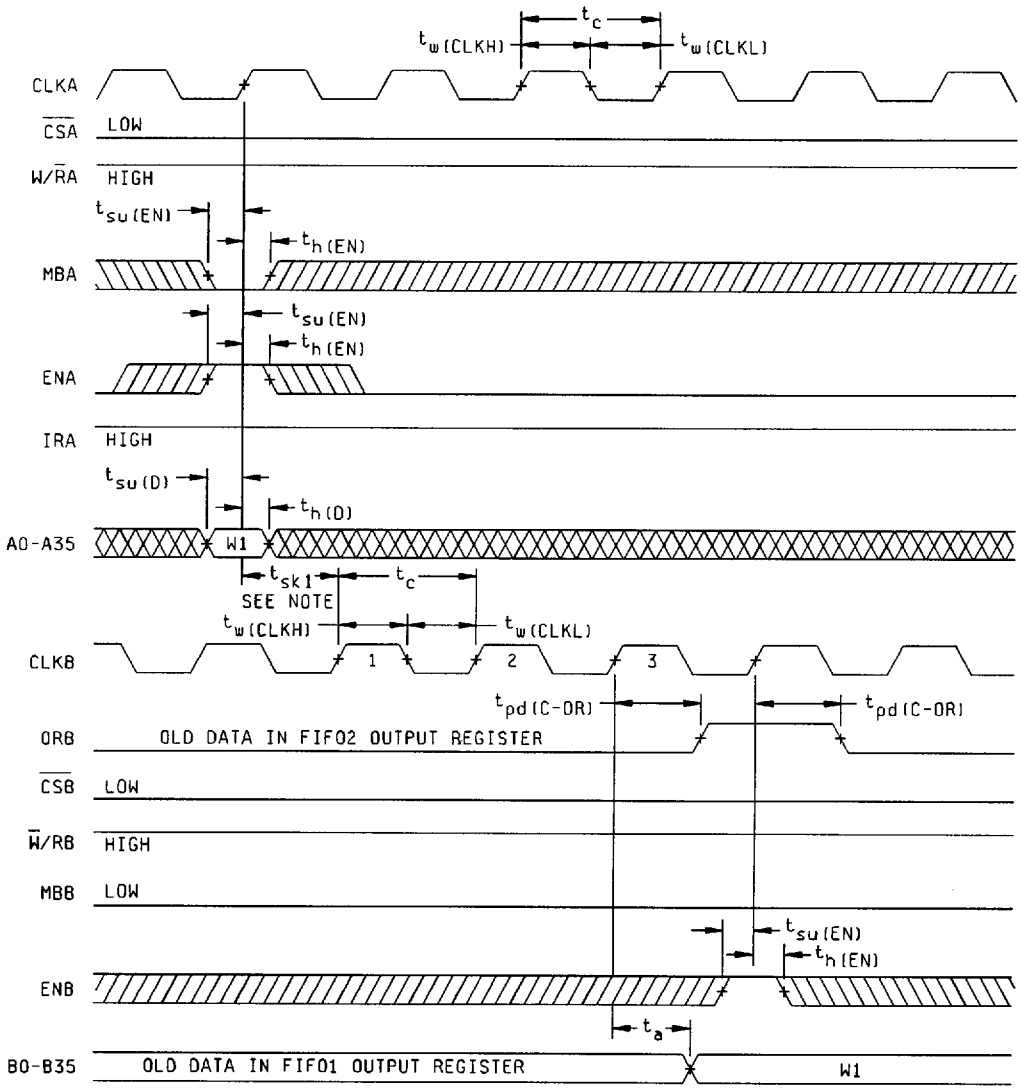
PORT-A READ CYCLE TIMING FOR FIFO2



NOTE: Read from FIFO2.

FIGURE 6. Timing waveforms - Continued.

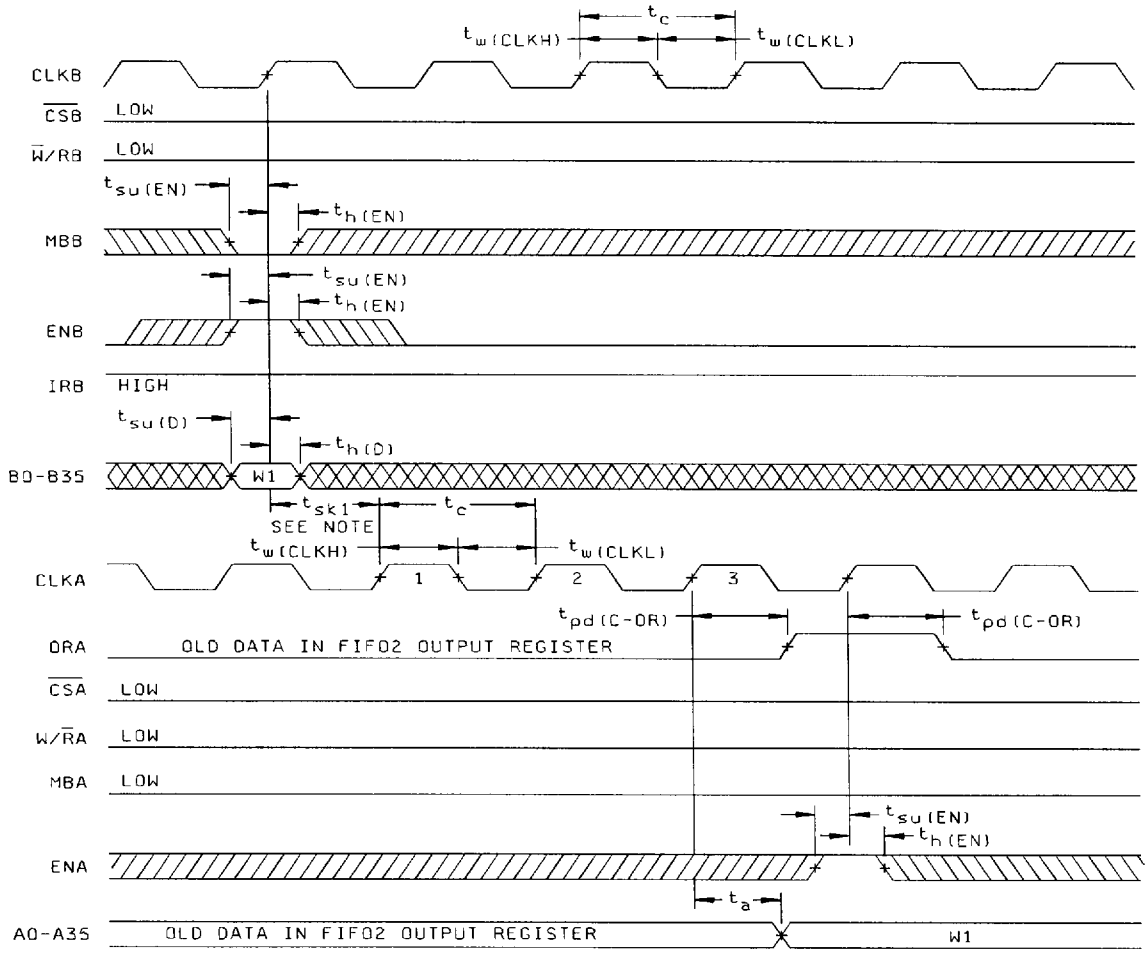
ORB FLAG TIMING AND FIRST DATA WORD FALLTHROUGH WHEN FIFO1 IS EMPTY



NOTE: t_{sk1} is the minimum time between a rising CLKA edge and a rising CLKB edge for ORB to transition high and to clock the next word to the FIFO1 output register in three CLKB cycles. If the time between the rising CLKA edge and rising CLKB edge is less than t_{sk1}, then the transition of ORB high and load of the first word to the output register may occur one CLKB cycle later than shown.

FIGURE 6. Timing waveforms - Continued.

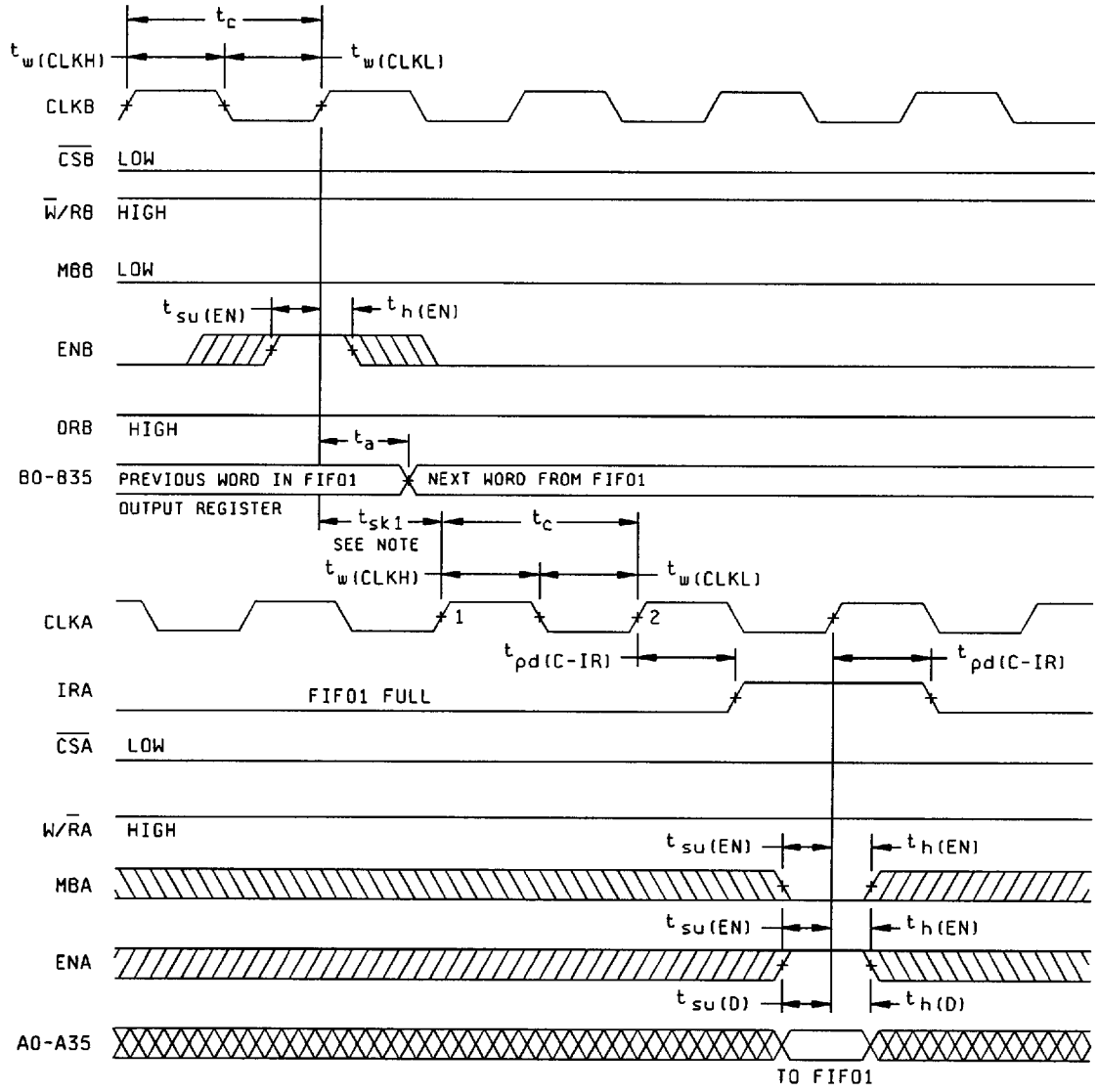
ORA FLAG TIMING AND FIRST-DATA-WORD FALLTHROUGH WHEN FIFO2 IS EMPTY



NOTE: t_{sk1} is the minimum time between a rising CLKB edge and a rising CLKA edge for ORA to transition high and to clock the next word to the FIFO2 output register in three CLKA cycles. If the time between the rising CLKB edge and rising CLKA edge is less than t_{sk1}, then the transition of ORA high and load of the first word to the output register may occur one CLKA cycle later than shown.

FIGURE 6. Timing waveforms - Continued.

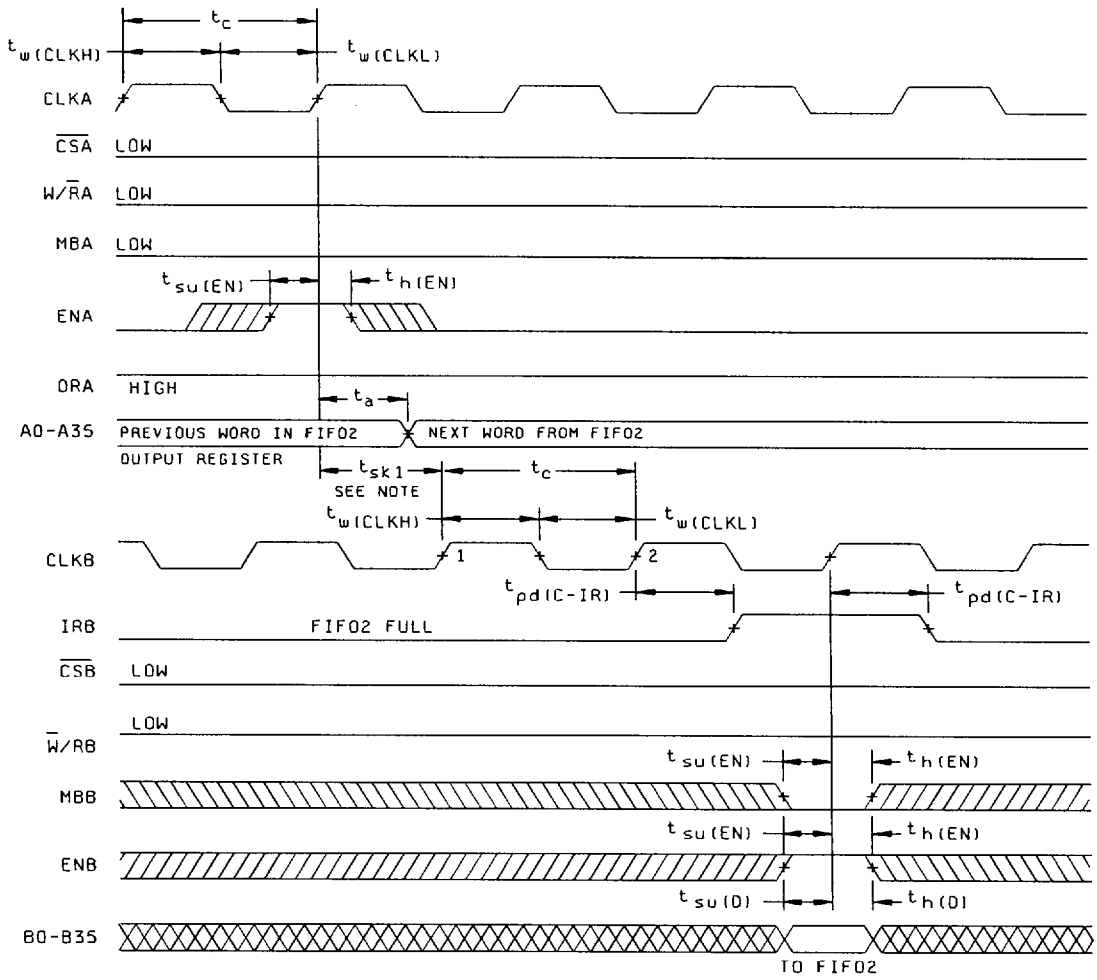
IRA FLAG TIMING AND FIRST AVAILABLE WRITE WHEN FIFO1 IS FULL



NOTE: t_{sk1} is the minimum time between a rising CLKB edge and a rising CLKA edge for IRA to transition high in the next CLKA cycle. If the time between the rising CLKB edge and rising CLKA edge is less than t_{sk1}, then IRA may transition high one CLKA cycle later than shown.

FIGURE 6. Timing waveforms - Continued.

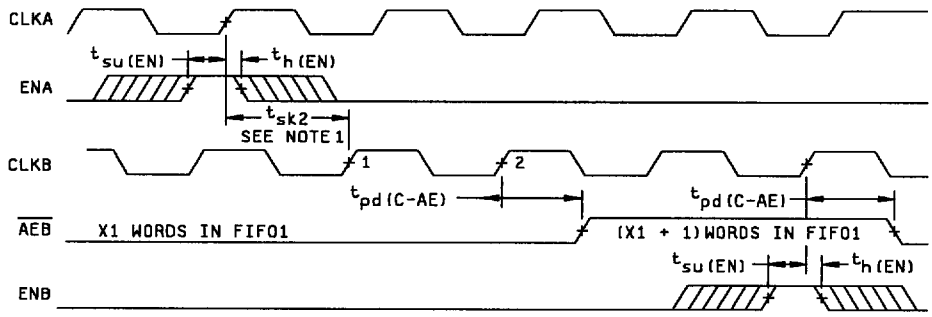
IRB FLAG TIMING AND FIRST AVAILABLE WRITE WHEN FIFO2 IS FULL



NOTE: t_{sk1} is the minimum time between a rising CLKA edge and a rising CLKB edge for IRB to transition high in the next CLKB cycle. If the time between the rising CLKA edge and the rising CLKB edge is less than t_{sk1}, then IRB may transition high one CLKB cycle later than shown.

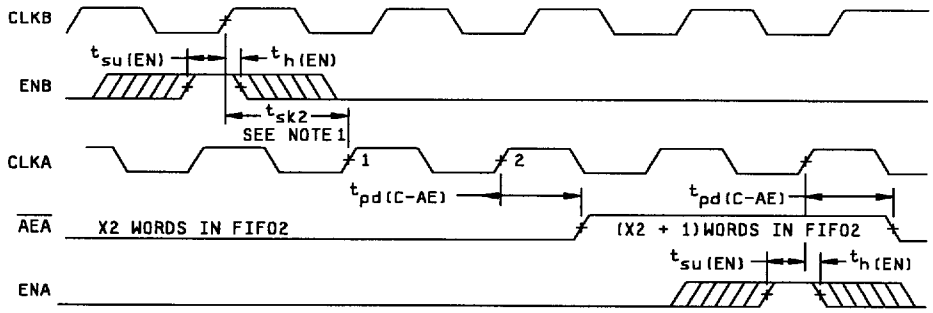
FIGURE 6. Timing waveforms - Continued.

TIMING FOR $\overline{AEB}$ WHEN FIFO1 IS ALMOST EMPTY



NOTES: 1. t_{sk2} is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{AEB}$ to transition high in the next CLKB cycle. If the time between CLKA edge and rising CLKB edge is less than t_{sk2}, then $\overline{AEB}$ may transition high one CLKB cycle later than shown.
2. FIFO1 write ($\overline{CSA}$ = L, W/$\overline{RA}$ = H, MBA = L), FIFO1 read ($\overline{CSB}$ = L, $\overline{W}$/RB = H, MBB = L). Data in the FIFO1 output register has been read from the FIFO.

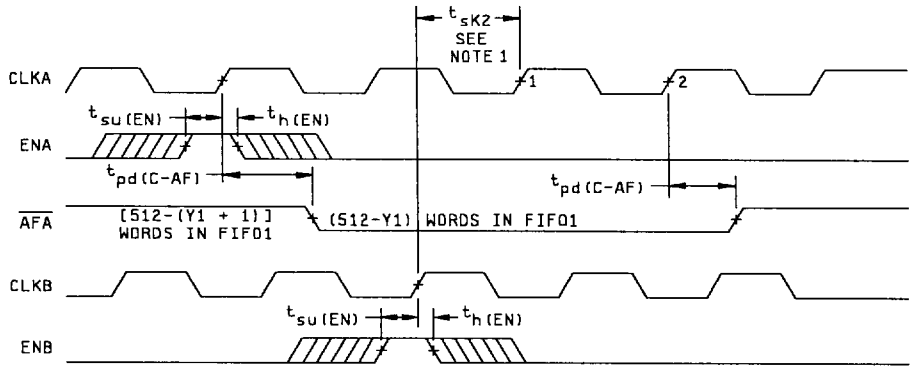
TIMING FOR $\overline{AEA}$ WHEN FIFO2 IS ALMOST EMPTY



NOTES: 1. t_{sk2} is the minimum time between a rising CLKB edge and a rising CLKA edge for $\overline{AEA}$ to transition high in the next CLKA cycle. If the time between CLKB edge and rising CLKA edge is less than t_{sk2}, then $\overline{AEA}$ may transition high one CLKA cycle later than shown.
2. FIFO2 write ($\overline{CSB}$ = L, $\overline{W}$/RB = L, MBB = L), FIFO2 read ($\overline{CSA}$ = L, W/$\overline{RA}$ = L, MBA = L). Data in the FIFO2 output register has been read from the FIFO.

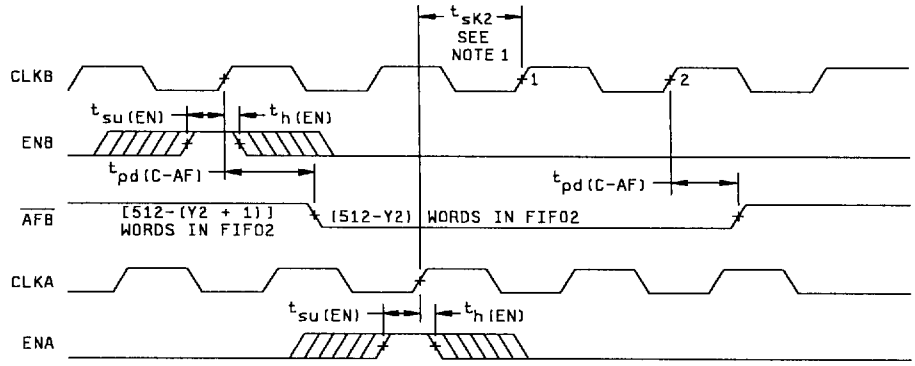
FIGURE 6. Timing waveforms - Continued.

TIMING FOR $\overline{AFA}$ WHEN FIFO1 IS ALMOST FULL



NOTES: 1. t_{sk2} is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{AFA}$ to transition high in the next CLKA cycle. If the time between CLKA edge and rising CLKB edge is less than t_{sk2}, then $\overline{AFA}$ may transition high one CLKB cycle later than shown.
2. FIFO1 write ($\overline{CSA}$ = L, W/$\overline{RA}$ = H, MBA = L), FIFO1 read ($\overline{CSB}$ = L, W/$\overline{RB}$ = H, MBB = L). Data in the FIFO1 output register has been read from the FIFO.

TIMING FOR $\overline{AFB}$ WHEN FIFO2 IS ALMOST FULL



NOTES: 1. t_{sk2} is the minimum time between a rising CLKB edge and a rising CLKA edge for $\overline{AFB}$ to transition high in the next CLKB cycle. If the time between CLKB edge and rising CLKA edge is less than t_{sk2}, then $\overline{AFB}$ may transition high one CLKA cycle later than shown.
2. FIFO2 write ($\overline{CSB}$ = L, W/$\overline{RB}$ = L, MBB = L), FIFO2 read ($\overline{CSA}$ = L, W/$\overline{RA}$ = L, MBA = L). Data in the FIFO2 output register has been read from the FIFO.

FIGURE 6. Timing waveforms - Continued.

TIMING FOR MAIL1 REGISTER AND $\overline{MBF1}$ FLAG

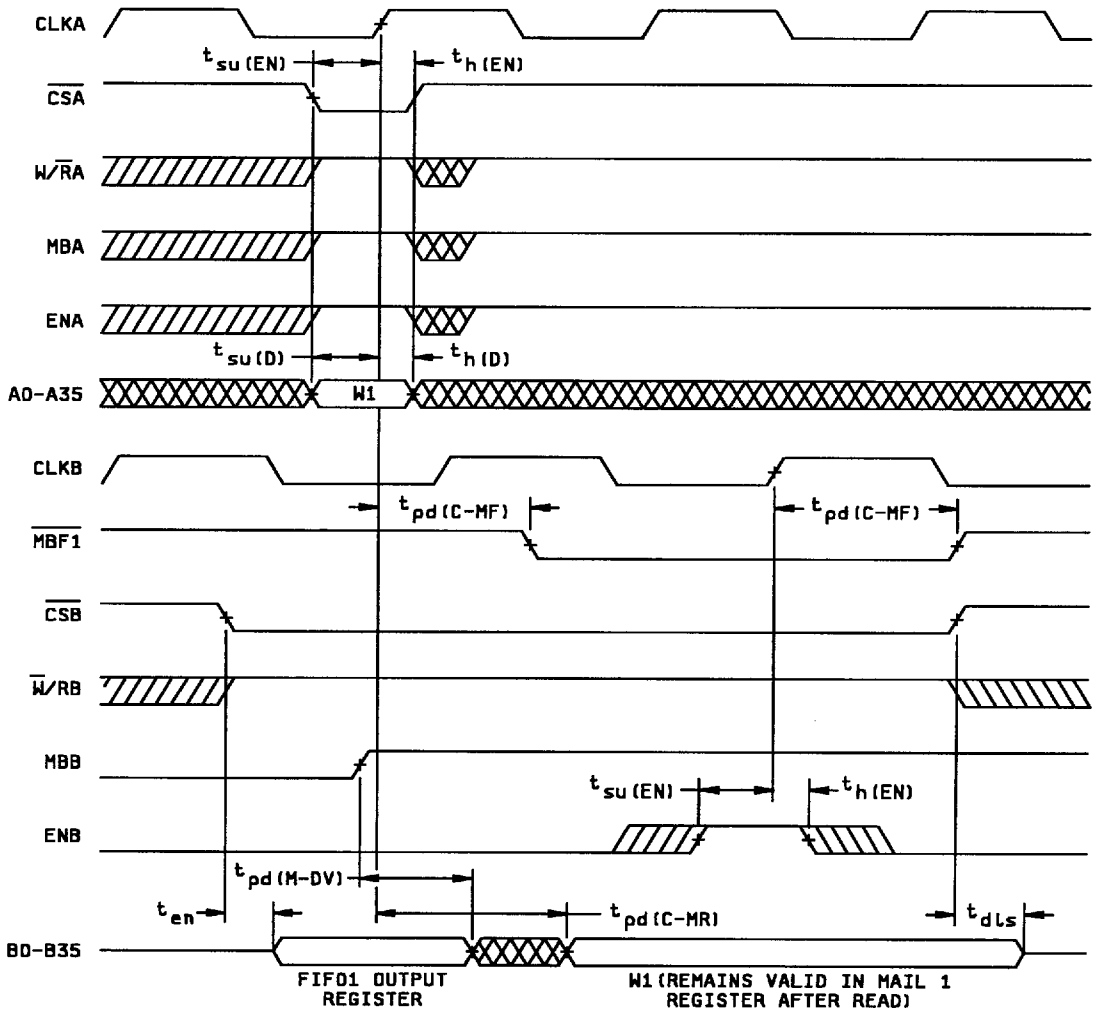


FIGURE 6. Timing waveforms - Continued.

TIMING FOR MAIL2 REGISTER AND $\overline{MBF2}$ FLAG

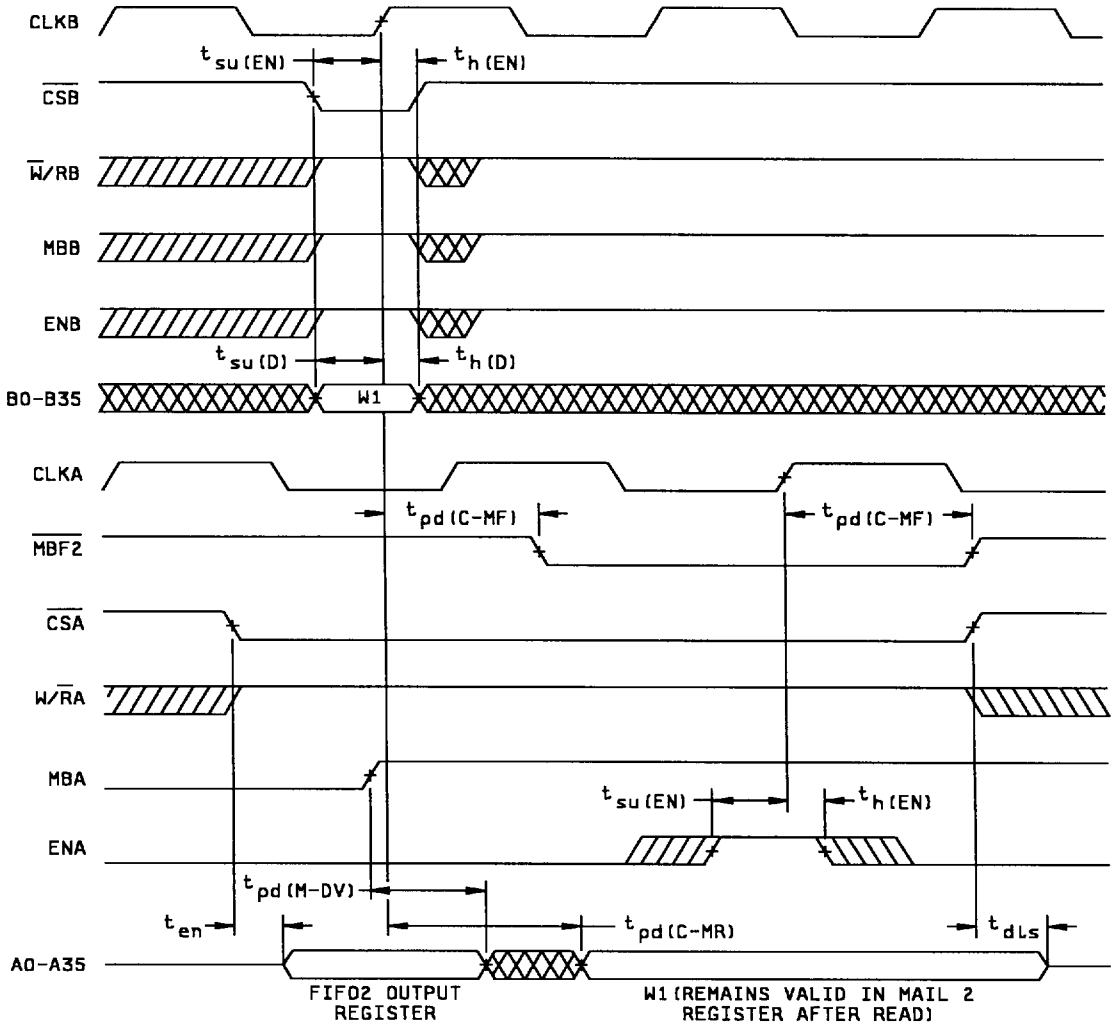


FIGURE 6. Timing waveforms - Continued.

Table IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/

Line no.	Test requirements	Subgroups (in accordance with MIL-STD-883, TM 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
		Device class M	Device class Q	Device class V
1	Interim electrical parameters (see 4.2)		1, 7, 9 or 1,2,8A,10	1, 7, 9 or 1,2,8A,10
2	Static burn-in I and II (method 1015)	Not required	Not required	Required
3	Same as line 1			1*, 7* Δ
4	Dynamic burn-in (method 1015)	Required	Required	Required
5	Same as line 1			1*, 7* Δ
6	Final electrical parameters (see 4.2)	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11
7	Group A test requirements (see 4.4)	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11
8	Group C end-point electrical parameters (see 4.4)	2, 3, 7, 8A, 8B	1, 2, 3, 7, 8A, 8B	1, 2, 3, 7, 8A, 8B, 9, 10, 11 Δ
9	Group D end-point electrical parameters (see 4.4)	2, 3, 7, 8A, 8B	2, 3, 7, 8A, 8B	2, 3, 7, 8A, 8B
10	Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9

1/ Blank spaces indicate tests are not applicable.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ Subgroups 7 and 8 functional tests shall verify the truth table.
4/ * indicates PDA applies to subgroup 1 and 7.
5/ ** see 4.4.1e.
6/ Δ indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the previous interim electrical parameters (see line 1).
7/ See 4.4.1d.

Table IIAB. Delta limits at +25° C.

Parameter 1/	Device types
	All
I_I	±10%
I_{OZH}, I_{OZL}	±10%

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 105 (see MIL-PRF-38535, appendix A).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Delete the sequence specified as initial (preburn-in) electrical parameters through interim (postburn-in) electrical parameters of method 5004 and substitute lines 1 through 6 of table IIA herein.

b. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(1) Dynamic burn-in for device class M (method 1015 of MIL-STD-883, test condition D; for circuit, see 4.2.1b herein).

c. Interim and final electrical parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-PRF-38535.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535 and the device manufacturer's QM plan. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-PRF-38535 permits alternate in-line control testing. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.

c. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

d. O/V (latch-up) tests shall be measured only for initial qualification and after any design or process changes which may affect the performance of the device. For device class M, procedures and circuits shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing activity or acquiring activity upon request. For device classes Q and V, the procedures and circuits shall be under the control of the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the preparing activity or acquiring activity upon request. Testing shall be on all pins, on five devices with zero failures. Latch-up test shall be considered destructive. Information contained in JEDEC Standard number 17 may be used for reference.

e. Subgroup 4 (C_{IN} and $C_{I/O}$ measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is 5 devices with no failures, and all input and output terminals tested.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB, in accordance with MIL-PRF-38535, and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

4.5 Delta measurements for device class V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIAB. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after burn-in perform final electrical parameter tests, subgroups 1, 7, and 9.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0525.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43216-5000, or telephone (614) 692-0674.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and as follows.

Pin name	I/O	Description
A0-A35	I/O	Port-A data. 36-bit bidirectional data port for side A.
$\overline{AEA}$	O	Port-A almost empty flag. Programmable flag synchronized to CLKA. It is low when the number of 36-bit words in FIFO2 is less than or equal to the value in the offset register, X2.
$\overline{AEB}$	O	Port-B almost empty flag. Programmable flag synchronized to CLKB. It is low when the number of 36-bit words in FIFO1 is less than or equal to the value in the offset register, X1.
$\overline{AFA}$	O	Port-A almost-full flag. Programmable flag synchronized to CLKA. It is low when the number of 36-bit locations in FIFO1 is less than or equal to the value in the offset register, Y1.
$\overline{AFB}$	O	Port-B almost-full flag. Programmable flag synchronized to CLKB. It is low when the number of 36-bit locations in FIFO2 is less than or equal to the value in the offset register, Y2.
B0-B35	I/O	Port-B data. 36-bit bidirectional data port for side B.
CLKA	I	Port-A clock. CLKA is a continuous clock that synchronizes all data transfers through port A and can be asynchronous or coincident to CLKB. IRA, ORA, $\overline{AFA}$, and $\overline{AEA}$, are synchronous to the low-to-high transition of CLKA.
CLKB	I	Port-B clock. CLKB is a continuous clock that synchronizes all data transfers through port B and can be asynchronous or coincident to CLKA. IRB, ORB, $\overline{AFB}$, and $\overline{AEB}$, are synchronous to the low-to-high transition of CLKB.
$\overline{CSA}$	I	Port-A chip select. $\overline{CSA}$ must be low to enable a low-to-high transition of CLKA to read or write data on port A. The A0-A35 outputs are in the high-impedance state when $\overline{CSA}$ is high.
$\overline{CSB}$	I	Port-B chip select. $\overline{CSB}$ must be low to enable a low-to-high transition of CLKB to read or write data on port B. The B0-B35 outputs are in the high-impedance state when $\overline{CSB}$ is high.
ENA	I	Port-A enable. ENA must be high to enable a low-to-high transition of CLKA to read or write data on port A.
ENB	I	Port-B enable. ENB must be high to enable a low-to-high transition of CLKB to read or write data on port B.
IRA	O	Input ready flag. IRA is synchronized to the low-to-high transition of CLKA. When IRA is low, FIFO1 is full and writes to its array are disabled. IRA is et low when FIFO1 is reset and is high on the second low-to-high tranition of CLKA after reset.
IRB	O	Input ready flag. IRB is synchronized to the low-to-high transition of CLKB. When IRB is low, FIFO2 is full and writes to its array are disabled. IRB is et low when FIFO2 is reset and is high on the second low-to-high tranition of CLKB after reset.
FS1,FS0	I	Flag offset selects. The low-to-high transition of a FIFO's reset input latches the values of FS0 and FS1. If either FS0 or FS1 is high when a reset input input goes high, one of three preset values is selected as the offset for the FIFO's almost-full and almost-empty flags. If both FIFO's are reeset simultaneously and both FS0 and FS1 are low when $\overline{RST1}$ and $\overline{RST2}$ go high, the first four writes to FIFO1 program the almost-full and almost-empty offsets for both FIFO's.
MBA	I	Port-A mailbox select. A high level on MBA chooses a mailbox register for a port-A read or write operation. When the A0-A35 outputs are active, a high level on MBA selects data from the mail2 register for output and low level selects FIFO2 output register data for output.
MBB	I	Port-B mailbox select. A high level on MBB chooses a mailbox register for a port-B read or write operation. When the B0-B35 outputs are active, a high level on MBB selects data from the mail1 register for output and low level selects FIFO1 output register data for output.
$\overline{MBF1}$	O	Mail1 register flag. $\overline{MBF1}$ is set low by the low-to-high transition of CLKA that writes data to the mail1 register. Writes to the mail1 register are inhibited while $\overline{MBF1}$ is low. $\overline{MBF1}$ is set high by a low-to-high transition of CLKB when a port-B read is selected and MBB is high. $\overline{MBF1}$ is set high when FIFO1 is reset.

Pin name	I/O	Description
$\overline{MBF2}$	O	Mail2 register flag. $\overline{MBF2}$ is set low by the low-to-high transition of CLKB that writes data to the mail2 register. Writes to the mail2 register are inhibited while $\overline{MBF2}$ is low. $\overline{MBF2}$ is set high by a low-to-high transition of CLKA when a port-A read is selected and MBA is high. $\overline{MBF2}$ is also set high when FIFO2 is reset.
ORA	O	Output-ready flag. ORA is synchronized to the low-to-high transition of CLKA. When ORA is low, FIFO2 is empty and reads from its memory are disabled. Ready data is present on the output register of FIFO2 when ORA is high. ORA is forced low when FIFO2 is reset and goes high on the third low-to-high transition of CLKA after a word is loaded to empty memory.
ORB	O	Output-ready flag. ORB is synchronized to the low-to-high transition of CLKB. When ORB is low, FIFO1 is empty and reads from its memory are disabled. Ready data is present on the output register of FIFO1 when ORB is high. ORB is forced low when FIFO1 is reset and goes high on the third low-to-high transition of CLKB after a word is loaded to empty memory.
$\overline{RST1}$	I	FIFO1 reset. To reset FIFO1, four low-to-high transitions of CLKA and four low-to-high transitions of CLKB must occur while $\overline{RST1}$ is low. The low-to-high transition of $\overline{RST1}$ latches the status of FS0 and FS1 for $\overline{AFA}$ and $\overline{AEB}$ offset selection. FIFO1 must be reset upon power-up before data is written to its RAM.
$\overline{RST2}$	I	FIFO2 reset. To reset FIFO2, four low-to-high transitions of CLKA and four low-to-high transitions of CLKB must occur while $\overline{RST2}$ is low. The low-to-high transition of $\overline{RST2}$ latches the status of FS0 and FS1 for $\overline{AFB}$ and $\overline{AEA}$ offset selection. FIFO2 must be reset upon power-up before data is written to its RAM.
W/$\overline{R}$A	I	Port-A write/read select. A high on W/$\overline{R}$A selects a write operation and a low selects a read operation on port A for a low-to-high transition of CLKA. The A0-A35 outputs are in the high-impedance state when W/$\overline{R}$A is high.
$\overline{W}$/RB	I	Port-B write/read select. A high on $\overline{W}$/RB selects a write operation and a low selects a read operation on port B for a low-to-high transition of CLKB. The B0-B35 outputs are in the high-impedance state when $\overline{W}$/RB is low.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN

DATE: 98-01-06

Approved sources of supply for SMD 5962-95628 are listed below for immediate acquisition only and shall be added to QML-38535 and MIL-HDBK-103 during the next revision. QML-38535 and MIL-HDBK-103 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revisions of QML-38535 and MIL-HDBK-103.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9562801QYA	01295	SNJ54ACT3632HFP

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for the part. If the desired lead finish is not listed, contact the Vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments Incorporated 13500 N. Central Expressway P.O. Box 655303 Dallas, TX 75265 Point of contact: I-20 at FM 1788 Midland, TX 79711-0448

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