1 M × 36-Bit Dynamic RAM Module — HYM 361020S-80/-10

Advanced Information

- 1 04 576 × 36-bit organization (alternative 2 097 153 × 18-bit)
- Fast access and cycle time
  80 ns access time
  160 ns cycle time (HYM 361020S-80)
  100 ns access time
  190 ns cycle time (HYM 361020S-10)
- Fast page mode capability with
  45 ns cycle time (HYM 361020S-80)
  55 ns cycle time (HYM 361020S-10
- Single + 5 V (± 10 %) supply
- Low power dissipation
  max. 5720 mW active (HYM 361020S-80)
  max. 5060 mW active (HYM 361020S-10)
  CMOS –166 mW standby
  TTL –132 mW standby
- $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$-only refresh, hidden refresh
- 12 Decoupling capacitors mounted on substrate
- All inputs, outputs and clocks fully TTL compatible
- Single in-Line Memory Module (L-SIM-72-1000)
  Utilizes eight 1 M × 4 DRAMs in 350 mil and four 1 M × 1 DRAM in 300 mil SOJ packages
- 1024 refresh cycles/16 ms

The HYM 361020S-80/-10 is a 36 Mbyte RAM module organized as 1048576 words by 36-bit in a 72-pin single in-line package comprising eight HYB 514400 DRAMs in 350 mil wide and four HYB 5 11000AJ in 300 mil wide SOJ packages together with twelve 0.2 µF ceramic decoupling capacitors on a PC board.

The HYM 361020S-80/-10 can also be used as a 2097152 words by 18-bits dynamic RAM module by means of connecting DQ0 and DQ18, DQ1 and DQ19, DQ2 and DQ20, ..., DQ17 and DQ35, respectively.

Each HYB 514400 and HYB 511000AJ is described in the data sheet and is fully electrical tested and processed according to Siemens standard quality procedure prior to module assembly. After assembly onto the board, a further set of electrical tests is performed.

The speed of the module can be detected by the use of four presence detect pins.

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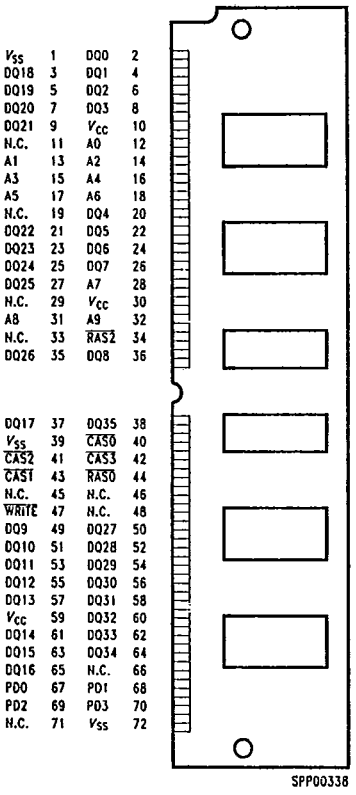
Ordering Information

Type	Ordering code	Package	Description
HYM 361020S-80	Q67100-Q558	L-SIM-72-1000-D	DRAM Module (access time 80 ns)
HYM 361020S-10	Q67100-Q559	L-SIM-72-1000-D	DRAM Module (access time 100 ns)

Pin Configuration



SPP00338

Pin Names

A0-A9	Address Inputs
DQ0-DQ35	Data Input/Output
CAS0-CAS3	Column Address Strobe
RAS0, RAS2	Row Address Strobe
WRITE	Read/Write Input
V_{CC}	Power (+ 5 V)
V_{SS}	Ground
PD	Presence Detect Pin
N.C.	No Connection

Presence Detect Pins

	HYM 361020S-80	HYM 361020S-10
PD0	V_{SS}	V_{SS}
PD1	V_{SS}	V_{SS}
PD2	N.C.	V_{SS}
PD3	V_{SS}	V_{SS}

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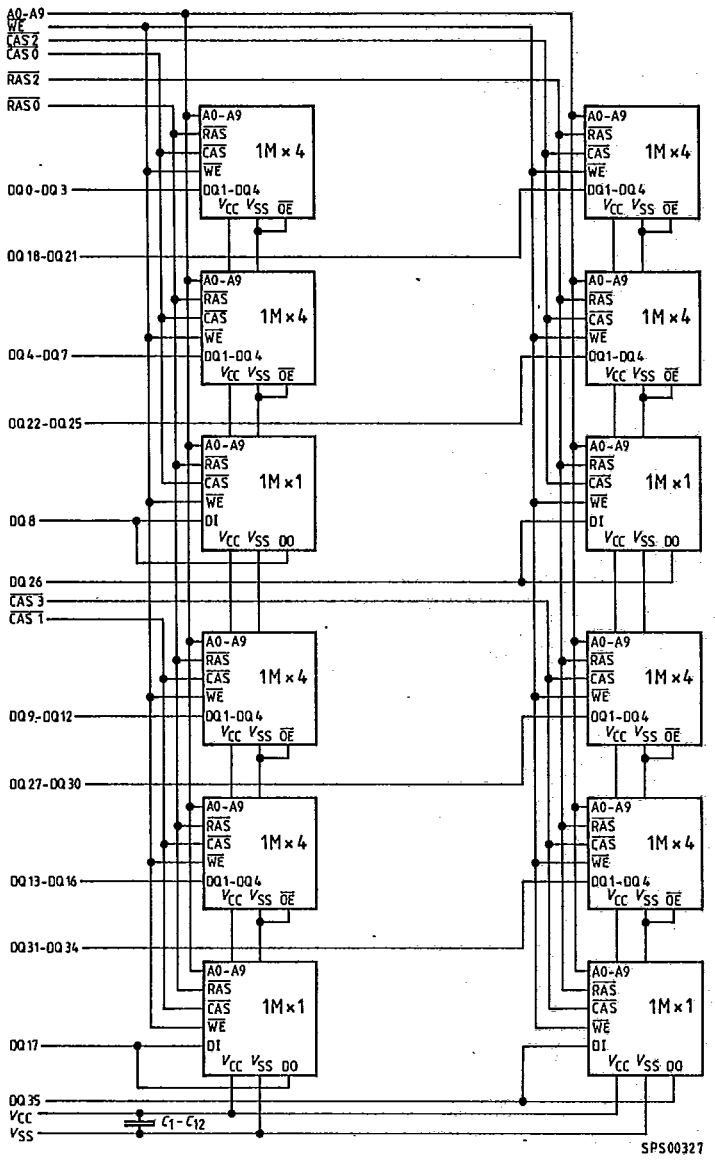
Block Diagram



Absolute Maximum Ratings

Operating temperature range ..... 0 to + 70 °C
Storage temperature range ..... – 55 to + 125 °C
Soldering temperature ..... 260 °C
Soldering time ..... 10 s
Input/output voltage ..... – 1 to + 7 V
Power supply voltage ..... – 1 to + 7 V
Power dissipation ..... 7.2 W
Data out current (short circuit) ..... 50 mA

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_A = 0 to 70 °C, V_{SS} = 0 V, V_{CC} = 5 V ± 10 %

Symbol	Parameter	Limit values		Unit	Test-condition
		min.	max.		
V_{IH}	Input high voltage	2.4	5.5	V	1)
V_{IL}	Input low voltage	– 1.0	0.8	V	–
V_{OH}	Output high voltage (I_{OUT} = – 5 mA)	2.4	–	V	–
V_{OL}	Output low voltage (I_{OUT} = 4.2 mA)	–	0.4	V	–
$I_{I(L)}$	Input leakage current (0 V ≤ V_{IN} ≤ 6.5 V, all other pins = 0 V)	– 50	50	µA	–
$I_{O(L)}$	Output leakage current (DO is disabled, 0 V ≤ V_{OUT} ≤ 5.5 V)	–10	10	mA	–
I_{CC1}	Average V_{CC} supply current: HYM 361020S-80 HYM 361020S-10 ($\overline{RAS}$, $\overline{CAS}$, address cycling: t_{RC} = t_{RC} min.)	– –	1040 920	mA mA	2) 3)
I_{CC2}	Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	–	24	mA	–
I_{CC3}	Average V_{CC} supply current, during $\overline{RAS}$ only refresh cycles: HYM 361020S-80 HYM 361020S-10 ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = t_{RC} min.)	– –	1040 920	mA mA	2) 3)
I_{CC4}	Average V_{CC} supply current, during fast page mode: HYM 361020S-80 HYM 361020S-10 ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ address cycling, t_{RC} = t_{RC} min.)	– –	760	mA mA	2) 3)
I_{CC5}	Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} - 0.2 V	–	12	mA	–
I_{CC6}	Average V_{CC} supply current, during $\overline{CAS}$-before-$\overline{RAS}$ refresh mode: HYM 361020S-80 HYM 361020S-10 ($\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC} = t_{RC} min.)	– –	1040 920	mA mA	–

Notes see page 217.

AC Characteristics [4] [5]

T_A = 0 to 70 °C, V_{CC} = 5 V ± 10 %, t_T = 5 ns

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Symbol	Parameter	Limit values				Unit
		HYM 361020S-80		HYM 361020S-10		
		min.	max.	min.	max.	
t_{RC}	Random read or write cycle time	160	–	190	–	ns
t_{PC}	Fast page mode cycle time	45	–	55	–	ns
t_{RAC}	Access time from $\overline{RAS}$ [6] [11]	–	80	–	100	ns
t_{CAC}	Access time from $\overline{CAS}$ [6] [11]	–	20	–	25	ns
t_{AA}	Access time from column address [6] [12]	–	40	–	50	ns
t_{CPA}	Access time from $\overline{CAS}$ precharge [6]	–	45	–	55	ns
t_{CLZ}	$\overline{CAS}$ to output in low-Z [6]	0	–	0	–	ns
t_{OFF}	Output buffer turn-off delay [7]	0	20	0	20	ns
t_T	Transition time (rise and fall) [5]	3	50	3	50	ns
t_{RP}	$\overline{RAS}$ precharge time	70	–	80	–	ns
t_{RAS}	$\overline{RAS}$ pulse width	80	10000	100	10000	ns
t_{RASP}	$\overline{RAS}$ pulse width (fast page mode)	80	200000	100	200000	ns
t_{RSH}	$\overline{RAS}$ hold time	20	–	25	–	ns
t_{CSH}	$\overline{CAS}$ hold time	80	–	100	–	ns
t_{CAS}	$\overline{CAS}$ pulse width	20	10000	25	10000	ns
t_{RCD}	$\overline{RAS}$ to CAS delay time [11]	20	60	25	75	ns
t_{RAD}	$\overline{RAS}$ to column address delay time [12]	15	40	20	50	ns
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ precharge time	5	–	10	–	ns
t_{CP}	$\overline{CAS}$ precharge time (fast page mode)	10	–	10	–	ns
t_{ASR}	Row address setup time	0	–	0	–	ns
t_{RAH}	Row address hold time	10	–	15	–	ns
t_{ASC}	Column address setup time	0	–	0	–	ns
t_{CAH}	Column address hold time	15	–	20	–	ns
t_{AR}	Column address hold time referenced to $\overline{RAS}$	60	–	75	–	ns
t_{RAL}	Column address to $\overline{RAS}$ lead time	40	–	50	–	ns
t_{RCS}	Read command setup time	0	–	0	–	ns

Notes see page 217.

AC Characteristics (cont'd) [4] [5]

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Symbol	Parameter	Limit values				Unit
		HYM 361020S-80		HYM 361020S-10		
		min.	max.	min.	max.	
t_{RCH}	Read command hold time [8]	0	–	0	–	ns
t_{RRH}	Read command hold time referenced to $\overline{RAS}$ [8]	0	–	0	–	ns
t_{WCH}	Write command hold time	15	–	20	–	ns
t_{WCR}	Write command hold time referenced to $\overline{RAS}$	60	–	75	–	ns
t_{WP}	Write command pulse width	15	–	20	–	ns
t_{RWL}	Write command to $\overline{RAS}$ lead time	15	–	25	–	ns
t_{CWL}	Write command to $\overline{CAS}$ lead time	15	–	25	–	ns
t_{DS}	Data setup time [9]	0	–	0	–	ns
t_{DH}	Data hold time [9]	15	–	20	–	ns
t_{DHR}	Data hold time referenced to $\overline{RAS}$	60	–	75	–	ns
t_{REF}	Refresh period	–	16	–	16	ns
t_{WCS}	Write command setup time [10]	0	–	0	–	ns
t_{CSR}	$\overline{CAS}$ setup time (CBR cycle)	5	–	10	–	ns
t_{CHR}	$\overline{CAS}$ hold time (CBR cycle)	15	–	20	–	ns
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ precharge time	0	–	0	–	ns
t_{CPN}	$\overline{CAS}$ precharge time	10	–	15	–	ns
t_{WRP}	Write to $\overline{RAS}$ precharge time [13]	10	–	10	–	ns
t_{WRH}	Write hold time referenced to $\overline{RAS}$ [13]	10	–	10	–	ns

Notes see page 217.

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Capacitance

T_A = 0 to 70 °C, V_{CC} = 5 V ± 10 %, f = 1 MHz

Symbol	Parameter	Limit values		Unit
		min.	max.	
C_{I1}	Input capacitance (A0 to A19, $\overline{WE}$)	–	85	pF
C_{I2}	I/O capacitance (DQ0-DQ7, DQ9-DQ16, DQ18-DQ25, DQ27-DQ34	–	20	pF
C_{I3}	I/O capacitance (DQ8, DQ17, DQ26, DQ35)	–	25	pF
C_{I4}	Input capacitance ($\overline{RAS0}$, $\overline{RAS2}$, $\overline{CAS0}$-$\overline{CAS3}$)	–	42	pF

Notes for pages 214 to 216

1) All voltages are referenced to V_{SS}.

2) I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.

3) I_{CC1} and I_{CC4} depend on output loading. Specified values are measured with the output open.

4) An initial pause of 500 µs is required after power-up followed by 8 $\overline{RAS}$ cycles of which at least one cycle has to be a refresh cycle before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles is required.

5) V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Transition times are also measured between V_{IH} and V_{IL}.

6) Measured with a load equivalent of 2 TTL loads and 100 pF.

7) t_{OFF} (max.) defines the time at which the output achieves the open-circuit conditions and is not referenced to output voltage levels.

8) Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

9) These parameters are referenced to the $\overline{CAS}$ leading edge.

10) t_{WCS} is not a restrictive operating parameter. This is included in the data sheet as electrical characteristics only. If t_{WCS} t_{WCS} (min.), the cycle is an early write cycle and data out pin will remain open (high impedance).

11) Operation within the t_{RCD} (max.) limit ensures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.

12) Operation within the t_{RAD} (max.) limit ensures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

13) For $\overline{CAS}$ before $\overline{RAS}$ cycles only.

Waveforms

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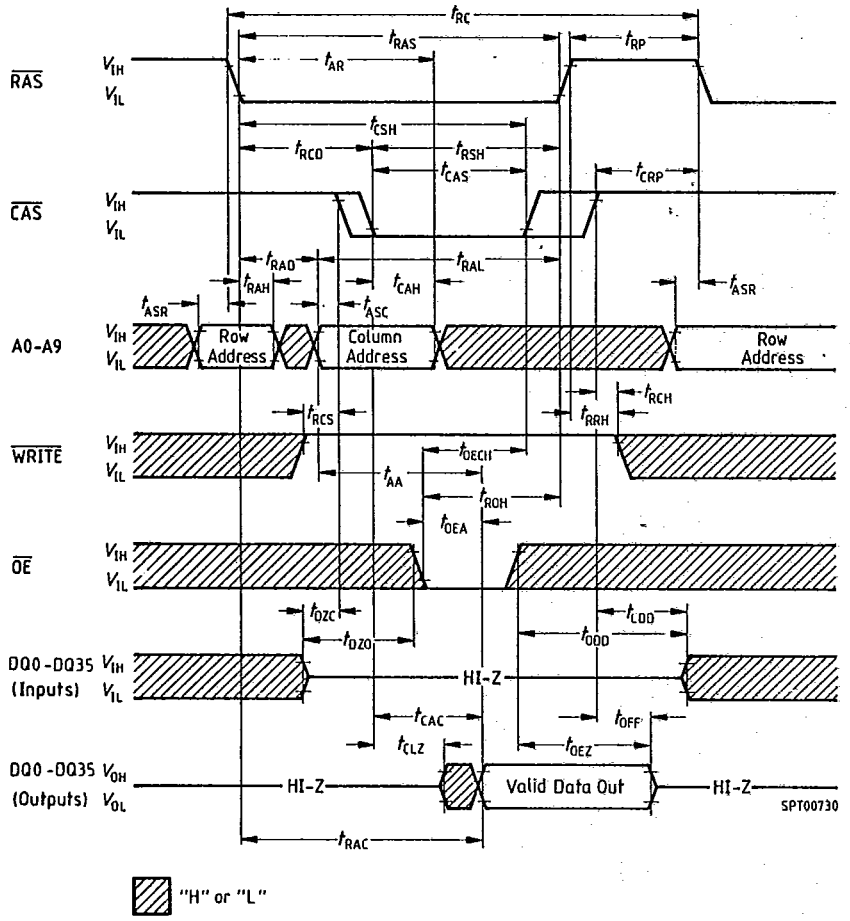
Read Cycle



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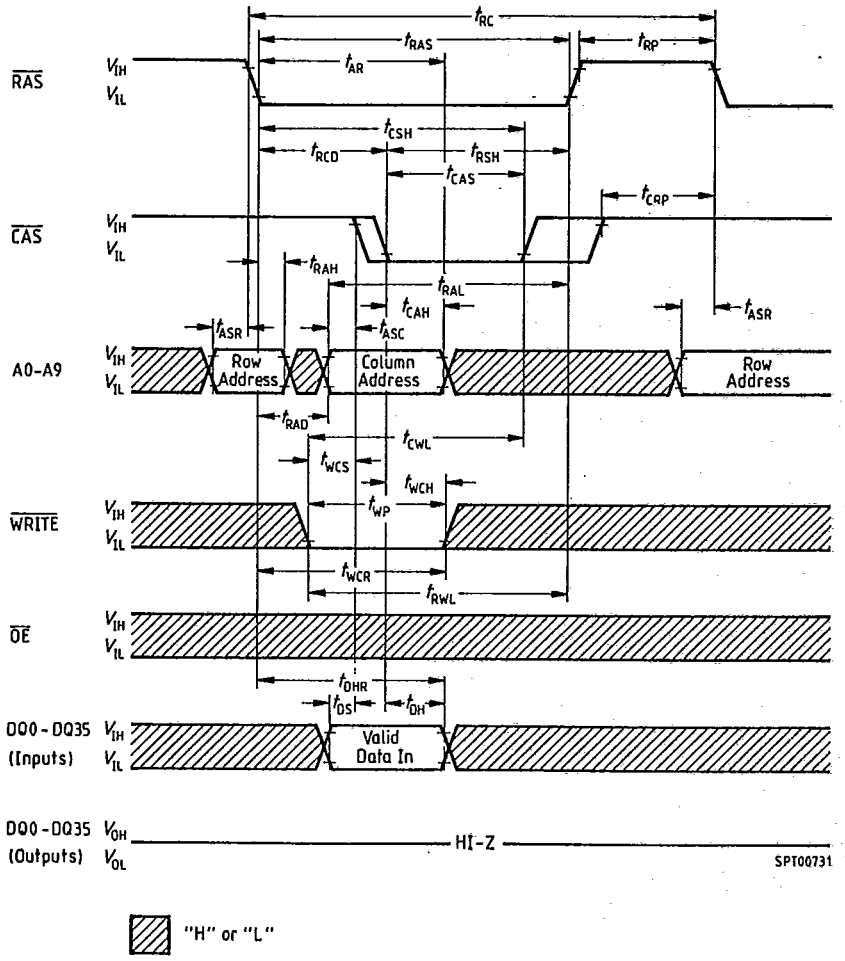
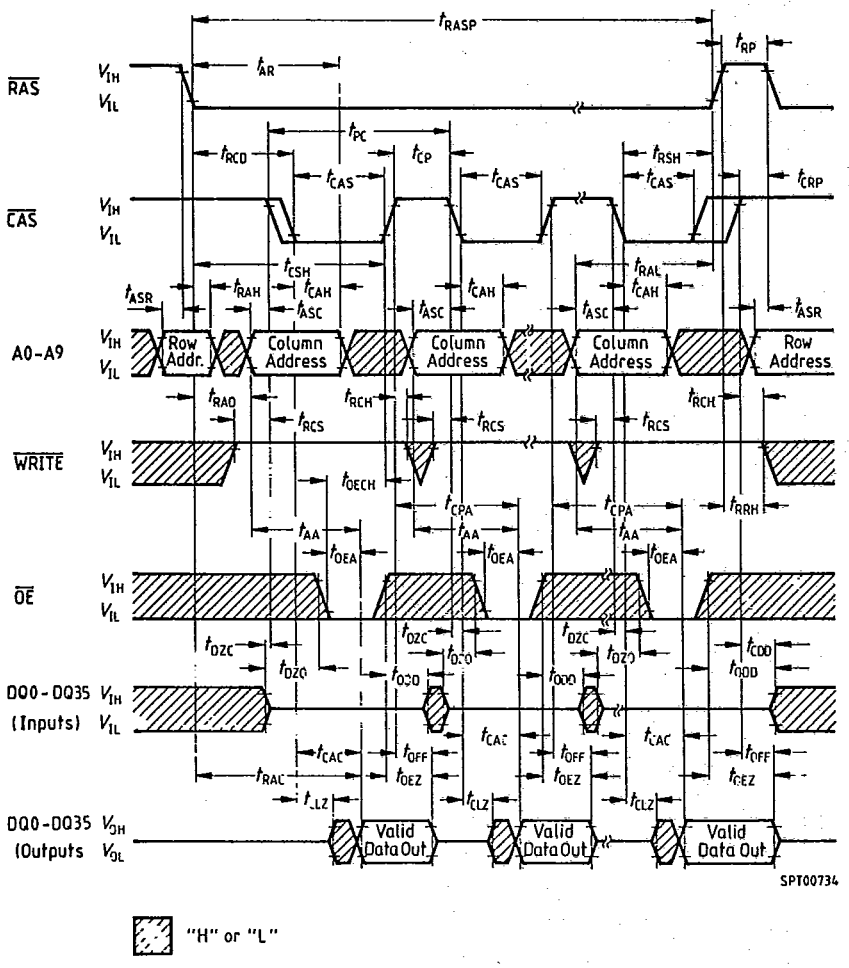
Write Cycle (early write)



Fast Page Mode Read Cycle



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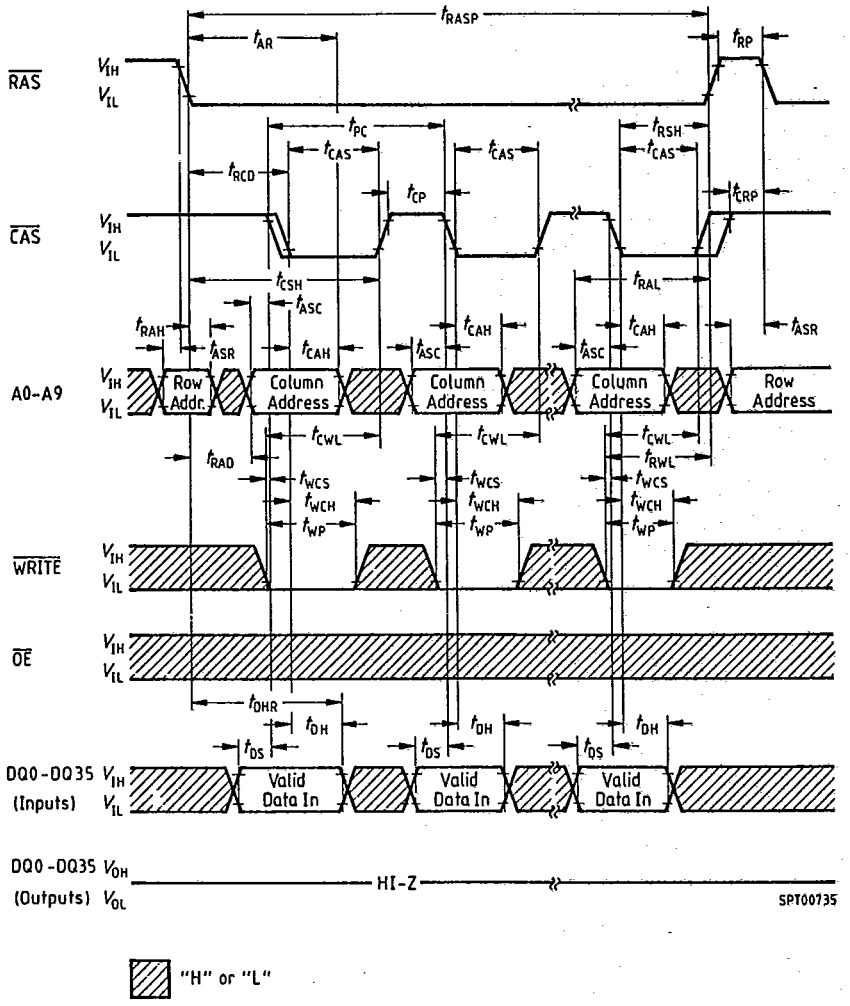
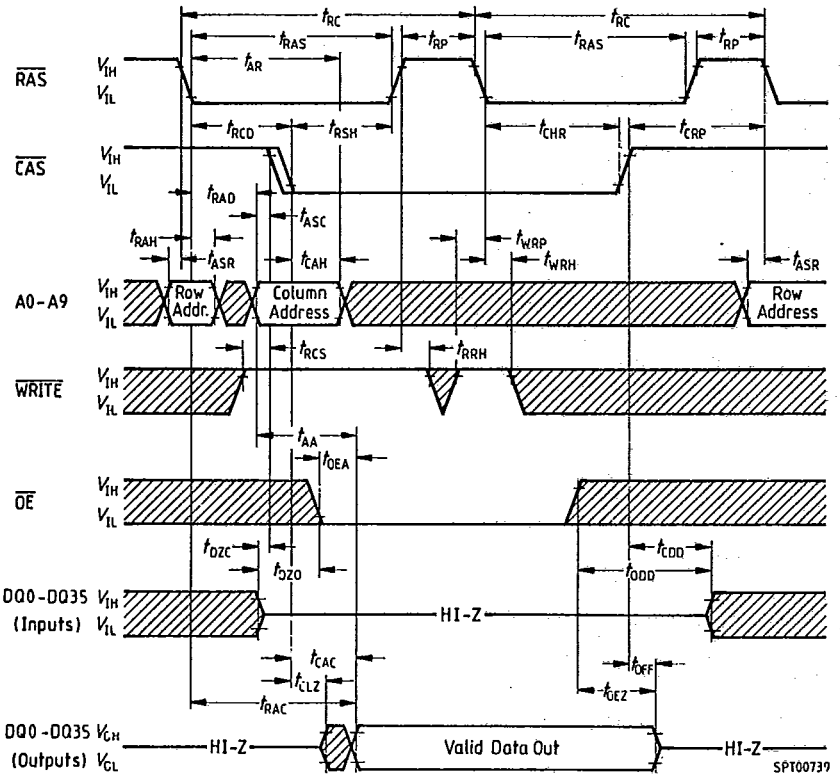
Fast Page Mode Write Cycle (early write)



Hidden Refresh Cycle (read)



"H" or "L"

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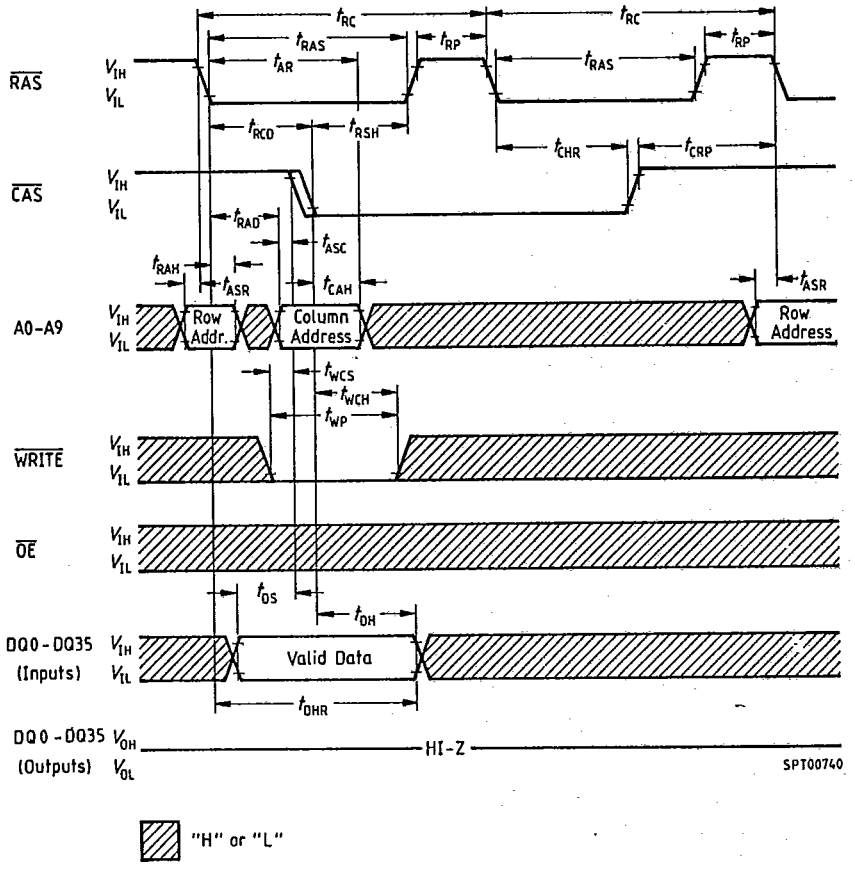
Hidden Refresh Cycle (early write)



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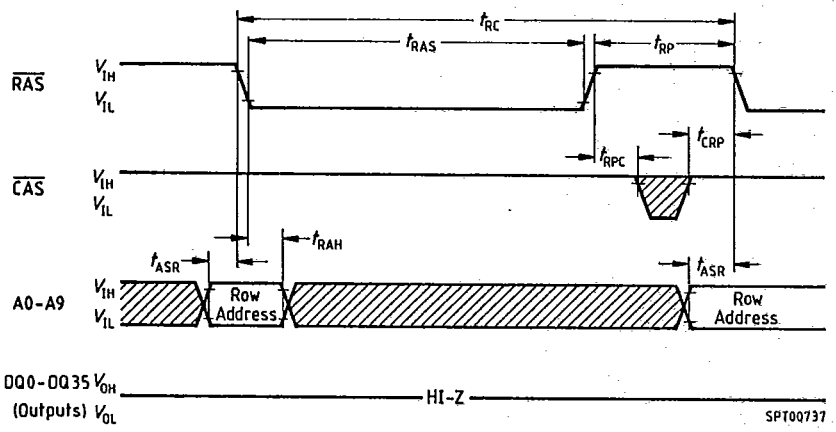
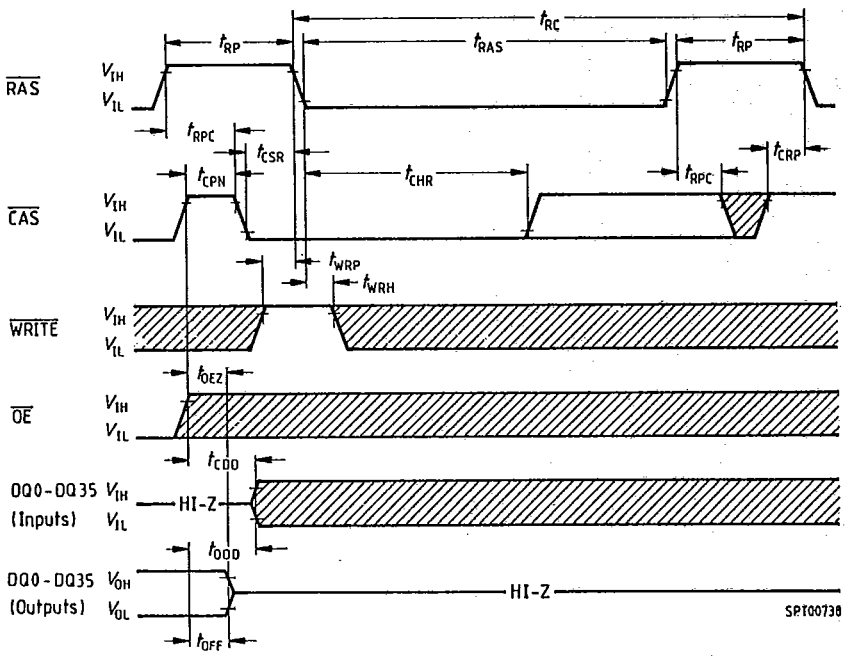
$\overline{\text{RAS}}$-Only Refresh Cycle



Note: $\overline{\text{WRITE}}$, $\overline{\text{OE}}$, I/O1-I/O4 (Inputs) = Don't Care

CAS-Before-RAS Refresh Cycle



"H" or "L"

Note: A0-A9 = Don't Care