

### General Description

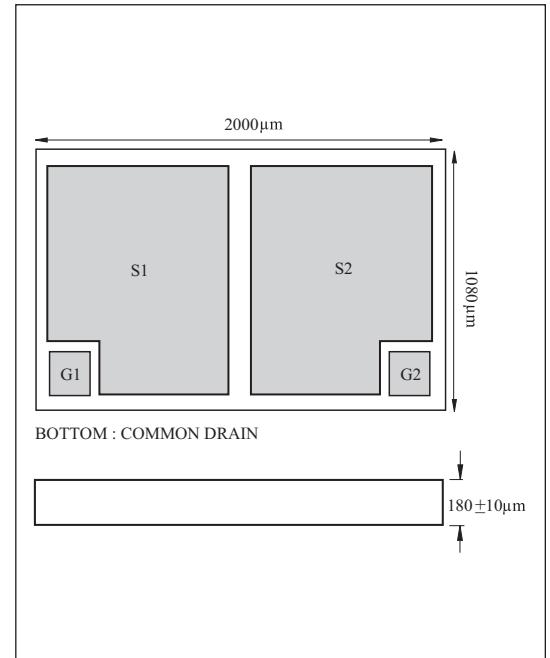
The K3519PQ-XH is a Dual N-channel MOSFET designed for use as a bi-directional load switch, facilitated by its common-drain configuration.

### FEATURES

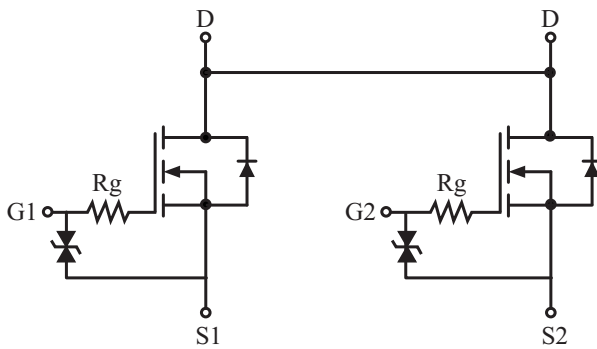
- Low on-state resistance  
 $R_{DS(ON)1} = 16m \text{ MAX } (V_{GS}=4.5V, I_S=1.0A)$   
 $R_{DS(ON)2} = 17m \text{ MAX } (V_{GS}=3.9V, I_S=1.0A)$   
 $R_{DS(ON)3} = 20m \text{ MAX } (V_{GS}=3.5V, I_S=1.0A)$

### MAXIMUM RATING (Ta=25 Unless otherwise noted)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Drain-Source Voltage	$V_{DSS}$	24	V
Gate-Source Voltage	$V_{GSS}$	$\pm 12$	V
Storage Temperature Range	$T_{stg}$	-55 150	



### Equivalent Circuit



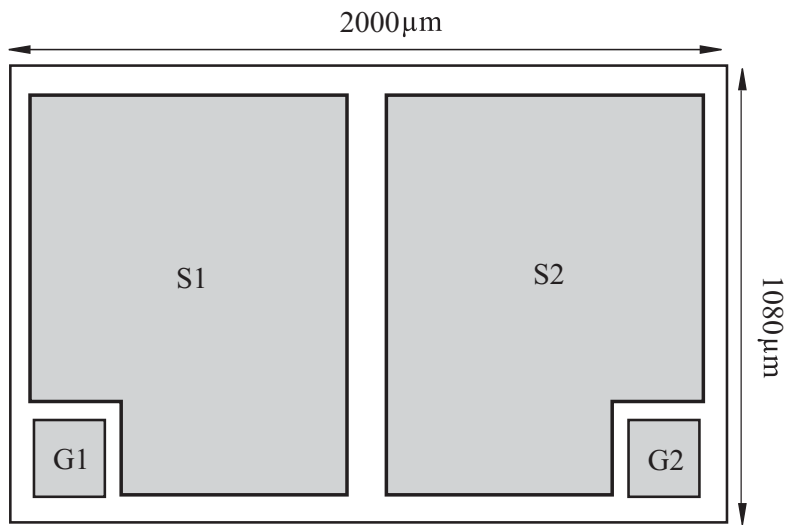
# K3519PQ-XH

## Electrical Characteristics (Ta=25 Unless otherwise noted)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Drain to Source Breakdown Voltage	$V_{(BR)DSS}$	$I_D = 250 \mu A, V_{GS} = 0V$	24	-	-	V
Gate to Source Breakdown Voltage	$V_{(BR)GSS}$	$I_G = \pm 100 \mu A, V_{DS} = 0V$	$\pm 12$	$\pm 14$	-	V
Drain Cut-off Current	$I_{DSS}$	$V_{DS} = 24V, V_{GS} = 0V$	-	-	1.0	$\mu A$
Gate to Source Leakage Current	$I_{GSS}$	$V_{GS} = \pm 12V, V_{DS} = 0V$	-	-	$\pm 10$	$\mu A$
Gate to Source Threshold Voltage	$V_{th}$	$V_{DS}=V_{GS}, I_D=250\mu A$	0.5	1.1	1.5	V
Drain to Source On Resistance	$R_{DS(on)}$	$V_{GS} = 4.5V, I_D = 1.0A$	-	12.0	16.0	m
		$V_{GS} = 3.9V, I_D = 1.0A$	-	13.0	17.0	m
		$V_{GS} = 3.5V, I_D = 1.0A$	-	14.5	20.0	m
Gate Resistance	$R_g$	$f=1MHz$	-	3.0	-	k
Input Capacitance	$C_{iss}$	$V_{DS} = 10V, V_{GS} = 0V, f=1MHz$	-	600	-	pF
Output Capacitance	$C_{oss}$		-	115	-	
Reverse Transfer Capacitance	$C_{rss}$		-	83	-	
Total Gate Charge	$Q_g$	$V_{DD}=10V, V_{GS}=3.9V, I_S=4.0A$	-	6.0	-	nC
Gate-Source Charge	$Q_{gs}$		-	0.8	-	
Gate-Drain Charge	$Q_{gd}$		-	2.5	-	
Source-Drain Forward Voltage	$V_{SD}$	$V_{GS} = 0V, I_S = 1.0A$	0.50	0.70	0.86	V

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## DIE INFORMATION



BOTTOM : COMMON DRAIN

CONTENTS	VALUE
Wafer size	8 inch notch type
Wafer thickness	180µm
Front Metal	A -4µm
Back Metal	Ti/Ni/Ag-1.4µm
Passivation Layer	Yes
Die Size (with scribe lane)	2000 × 1080µm <sup>2</sup>
Scribe lane width	60µm
Gate Pad Size	170 × 163µm <sup>2</sup>
Die edge to gate Pad	84µm
Die edge to Source Pad	70µm
Gross Die(per Wafer)	13,470ea