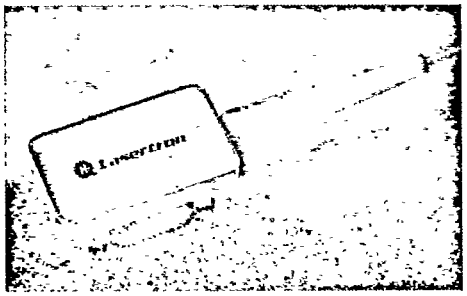
QDFH

High-Impedance Integrating pinFET Receiver



- *Telecom trunk and junction applications*
- *High-impedance integrating circuit configuration*
- *Data rates up to 1.0 Gb/s*
- *Industry-standard 14-pin DIL package*
- *Single-mode fiber*

Description

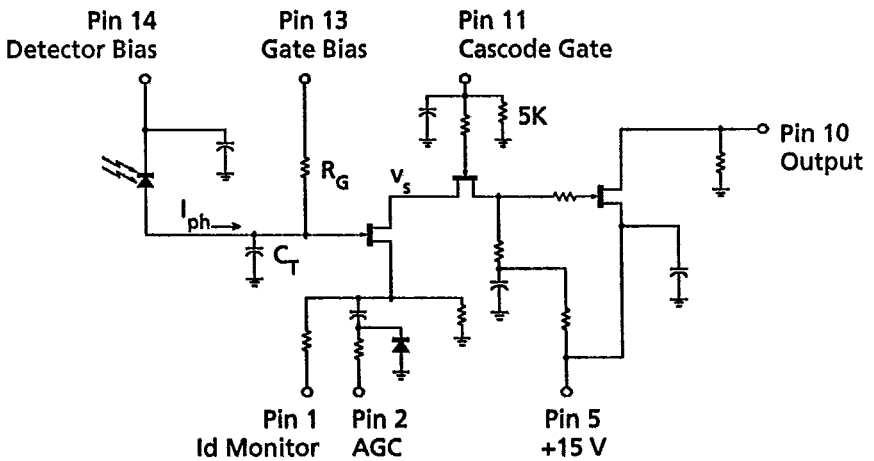
The QDFH pinFET features an integrating design for high sensitivity requirements at data rates up to 1.0 Gb/s. The QDFH design yields excellent noise performance not only at room temperature but also at elevated temperatures. The QDFH also incorporates a gain control feature which extends the optical dynamic range of the device by up to 4 dB as compared to conventional integrating pinFET designs.

Applications

Incident light on the pin photodiode, shown in Figure 1, produces a signal current I_{ph}, which flows through the gate resistor (R_G) at low frequencies or through the capacitor (C_T) at high frequencies. C_T is composed of the detector, FET and parasitic capacitances. Voltage is supplied to pin 13 to compensate for the voltage drop across R_G. This can be controlled by monitoring the voltage at pin 1 keeping that voltage constant. Because the FETs are made of GaAs, they have a high input impedance; C_T is the total capacitance of the FET input. The resulting voltage signal (V_s) is run through a cascode gain stage in which the amplified signal is output to pin 10. The combination of C_T and R_G results in an input pole usually at 1 MHz or less. This effect gives rise to the term integrating pinFET.

Figure 1

QDFH Integrating Design



All of the photocurrent must exit the pinFET through R_G if the FET is to be properly biased. The maximum value of the optical input depends on the value of the gate bias voltage (pin 13). The greater the gate bias voltage applied, the wider the dynamic range of the pinFET. For example, if we apply a voltage of -15 V to R_G (300K Ohms) a current of 50 µA is produced, corresponding to a maximum optical input power of -12 dBm. Decreasing the value of R_G would allow a greater amount of photocurrent to exit. However, the amount of Johnson noise present in the QDFH would increase, impairing the sensitivity.

While this circuit might not be ideal for every application, pertinent details for QDFH implementation are indicated. The QDFH consumes 360 mW of electrical power at minimum gain and 490 mW at maximum gain. Careful attention to heat dissipation is required for optimal performance, especially at elevated ambient temperature.

To use the pinFET to the full extent of the amplifier bandwidth, the output must be equalized. The equalizer can be nothing more than a simple differentiator, but its exact configuration depends on the application for which the QDFH is being used. An important consideration in the design of the equalizer is determining the frequency at which the equalizer no longer differentiates the output. Assume for this discussion that the equalizer is a simple differentiator composed of a capacitor, C_{eq}, and a resistor to ground, typically 50 Ohms. The effective transimpedance of this configuration is given by:

$$Z_{eff} = \frac{V_{out}}{I_{in}} = \frac{AC_{eq}\,R_{out}}{C_t}$$

A: Amplifier Gain
R_{out}: Output Impedance
C_t: Internal (~1pF) Capacitance

Clearly, to maximize the output signal of the pinFET we would like to make C_{eq} as large as possible. Given that the output impedance of the emitter-follower is 50 Ohms, the corner frequency for the differentiator is given by $F_{eq} = 1/(2\pi x 50 x C_{eq})$. If C_{eq} is too large, the output of the pinFET is not equalized over the full band pass of the amplifier. Keep in mind that the integrated response of the pinFET is falling at 6 dB/octave. Even though F_{eq} might be in excess of the pole in A(f), it is not increasing at a rate of 6 dB/octave. This effect is more exaggerated as the pole frequency approaches F_{eq}. Thus there is always a bandwidth penalty associated with the equalization.

As an example, if the 3 dB bandwidth of A(f) is at 700 MHz and the equalizer is designed such that F_{eq} = 1400 MHz, we will observe a net 600 MHz 3 dB frequency response due to this effect. Thus the exact equalizer configuration depends on the specific application and must account for the tradeoff between bandwidth and effective transimpedance. A starting point for determining C_{eq} is to calculate the first pole frequency cutoff for C_{eq} described by:

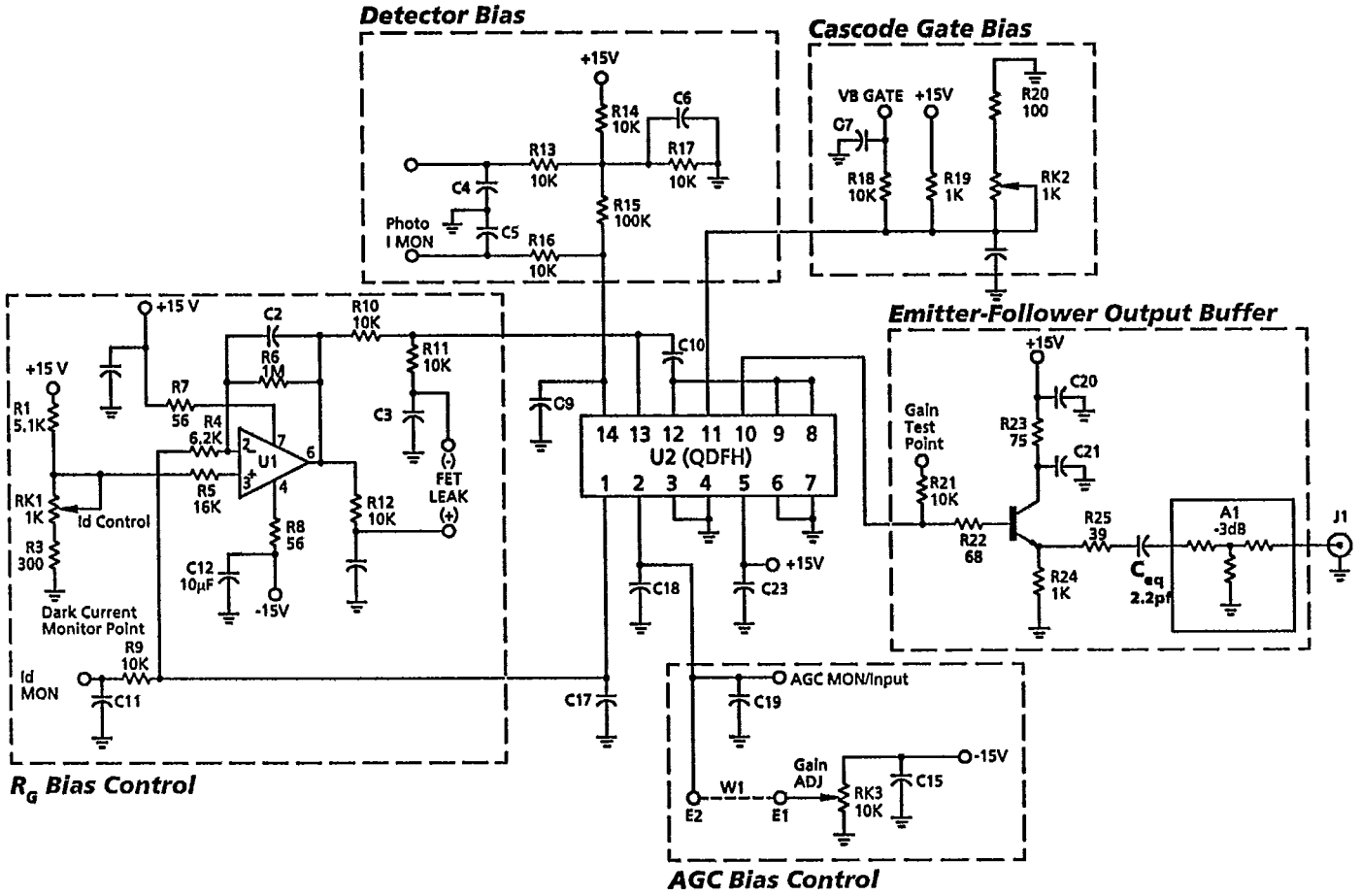
$$C_{eq} = (\text{Data Rate} \times 2\pi \times 50)^{-1}$$

The integrating circuit design of the QDFH imposes restrictions on the allowable data patterns. Well balanced line codes are necessary in order to avoid the 'integrating' characteristics of the pinFET from overloading the circuit. Such restrictions are not imposed by transimpedance pinFET designs.

An electrical gain reduction of 8 dB can be achieved by applying an external electrical signal, thus significantly extending the dynamic range of the preamplifier. For some applications, dynamic range limitations may be set by the requirement for linear operation of the preamplifier. There are also dynamic range limitations imposed by the requirement that the input FET be properly biased over a range of input photocurrents. The external circuitry biasing the pinFET is used to maintain the input FET at the correct bias point by adjusting the current flowing out of R_G through control of its external bias at pin 13.

QDFH
(continued)

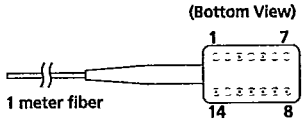
QDFH Implementation Circuit



Notes

- Capacitors are 0.1 µF unless noted.
- RK1 is adjusted for 1.20 VDC on pin 1 with a pinFET in the test fixture.
- RK3 is adjusted for 2.0 VDC on pin 10 with a pinFET in the test fixture.

Pin Connections



1 Input FET current
2 AGC
3 Case Ground
4 NC
5 +15 V
6 Case Ground
7 Case Ground
8 Case Ground
9 Case Ground
10 Output
11 Cascode gate bias
12 Case Ground
13 Gate resistor bias
14 Detector bias (+8 V)

Specifications

Noise filter bandwidth (MHz)			475
Sensitivity (dBm, Avg.): Min.			-36
Typ.			-37
Typ. transimpedance (K Ohm)			1700
Max. input (dBm, Avg., with AGC)			-12
Common Specifications	**Min**	**Typ**	**Max**
Sensitivity change 25 to 65°C (dB)		1.5	
Detector dark current (nA)		8	20
Detector capacitance -5 V bias (pF)		0.15	0.2
Load impedance (Ohms, before equalizer)		1000	
Output voltage at Pmax (V)		7.0	
Measured output impedance (Ohms)			30
Responsivity 1300 nm and -5 V bias (A/W)	0.75	0.85	
Responsivity change (25 to 65°C)		0.1	0.5
Power consumption with implementation circuitry:			
+15 V supply (mW)		780	
-15 V supply (mW)		230	
Power consumption without implementation circuitry:			
+15 V supply (mW)		390	
-15 V supply (mW)		20	
Operating temperature range (°C)	-20		70
Storage temperature range (°C)	-20		85

Absolute Maximum Ratings

Fiber coupled power (mW)	5
Reverse photocurrent (mA)	5
Reverse bias voltage (V)	15
Forward current (mA)	2
Lead soldering temperature (°C)	260
Lead soldering duration (sec)	10
Fiber yield strength (N, min)	10
Fiber bend radius (mm, min)	35

Ordering Information

	Suffix			
Base Model	**No Connector**	**FC/PC**	**Biconic**	**ST**
QDFH-9003	-002	-050	-051	-052

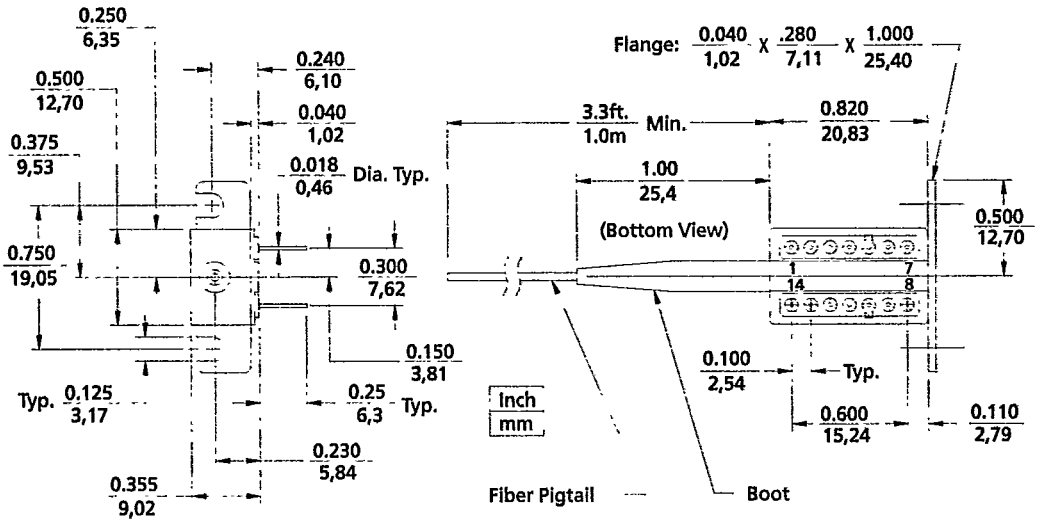
Package Specifications

T-91-20

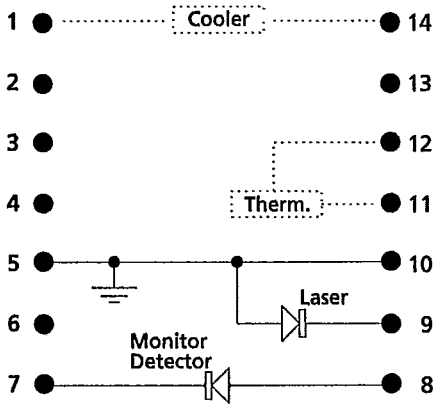
Lasertron uses a variety of industry-standard packages to house its products. The dimensions indicated here are common to all like packages; however, pin connections may differ between product families. Product-specific pin connections are provided in the individual data sheets in the Product Information section of this Product Guide.

Source Packages

14-pin DIL "Longhorn" (Lasers, LEDs)



LONGHORN SCHEMATIC

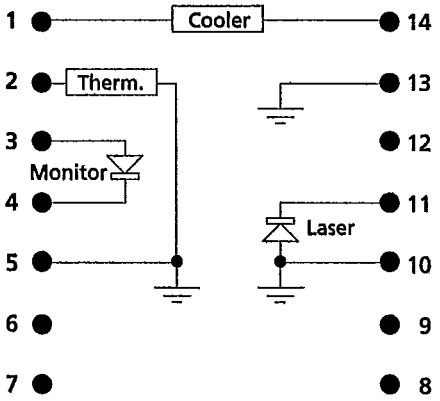


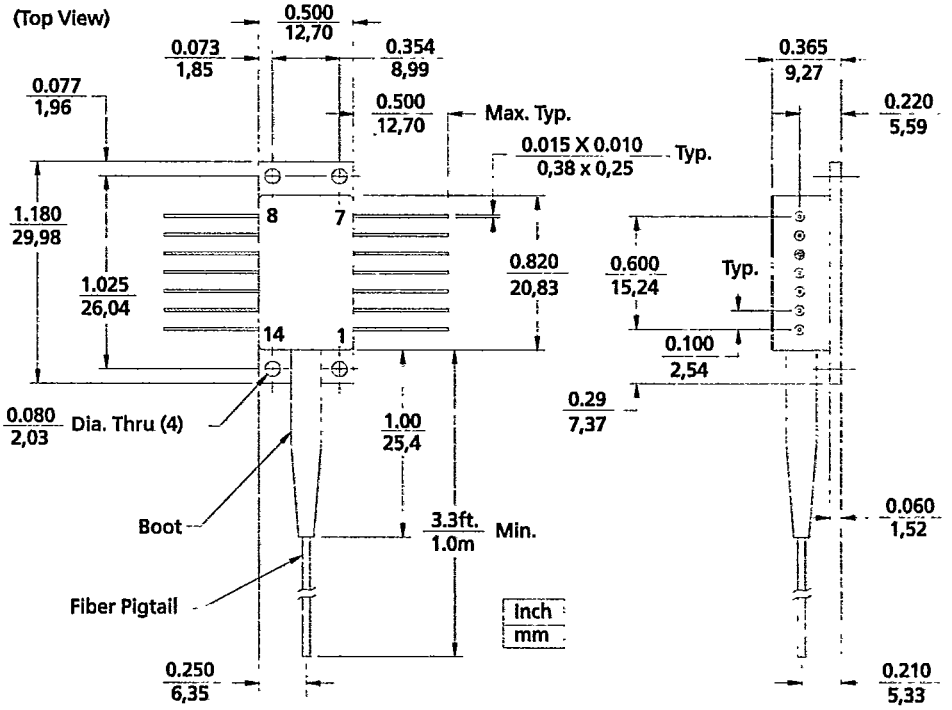
Note: Cooler and thermistor are not included in all modules.

Source Packages *(continued)*

14-pin "Butterfly"

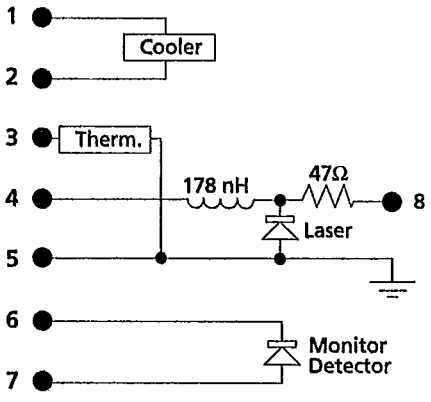
BUTTERFLY SCHEMATIC

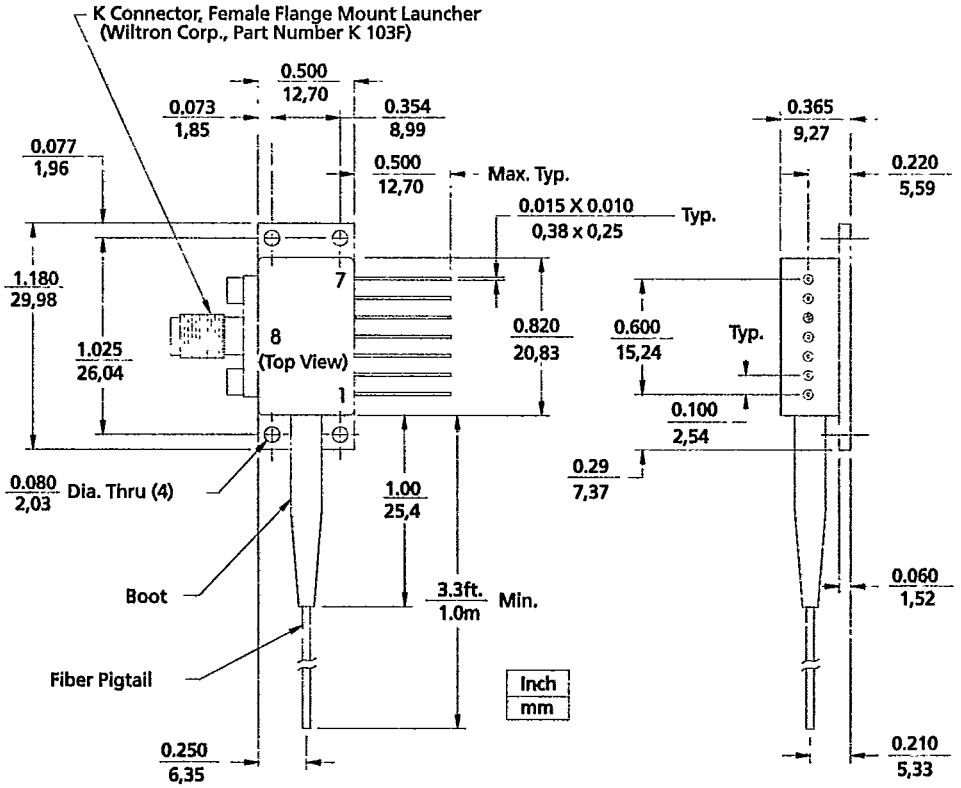




Microwave Laser

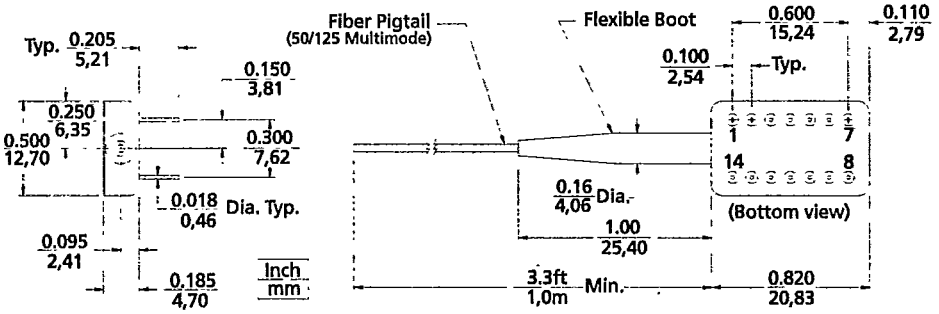
MICROWAVE LASER SCHEMATIC



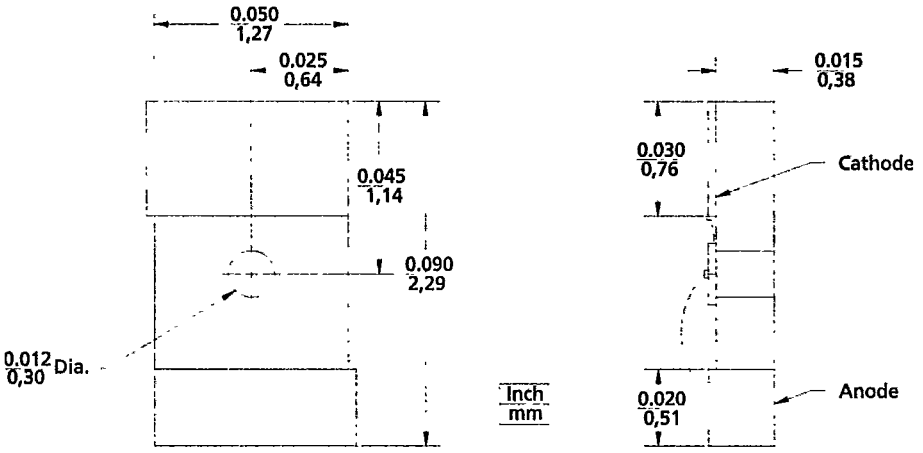


Detector Packages

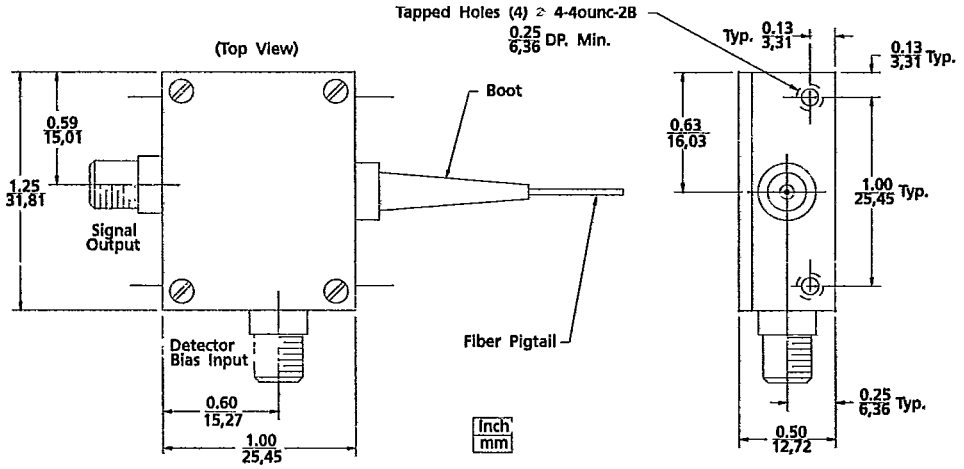
14-pin DIL PIN/pinFET



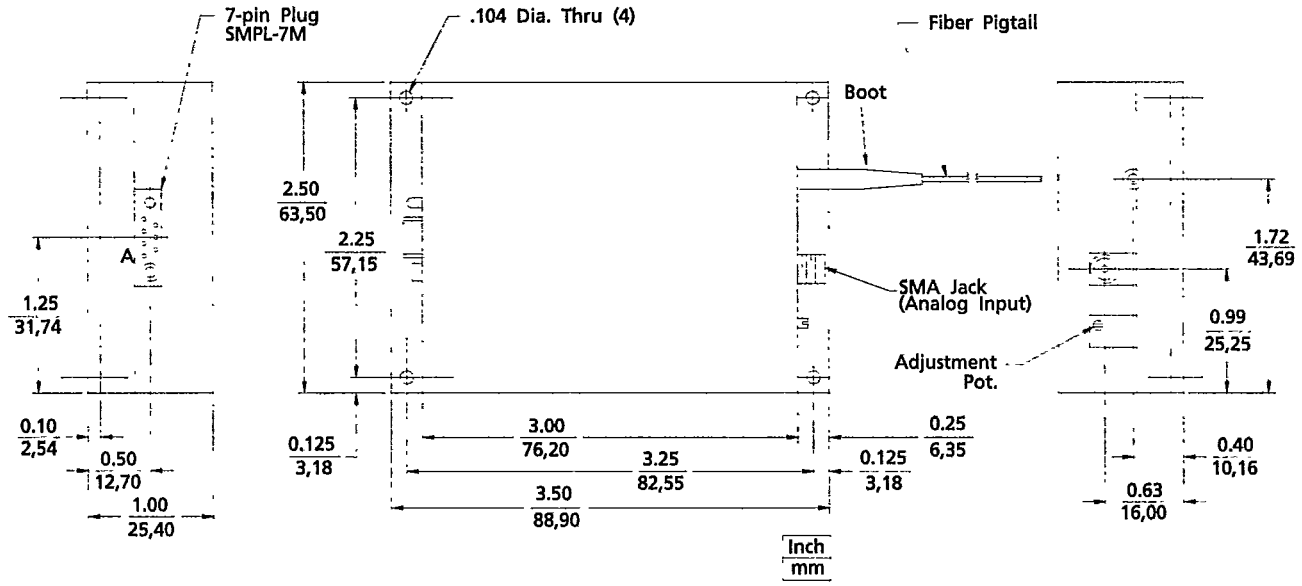
QDE035, QDE075



QDEMW1, QDEMW3 Microwave Detector



QTX Transmitter



QLXSMW Microwave Transmitter