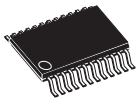
STPIC44L02

4 CHANNEL SERIA AND PARALLEL LOW SIDE PRE-FET DRIVER

- 4-CHANNEL SERIAL-IN PARALLEL-IN LOW SIDE PRE-FET DRIVER
- DEVICE ARE CASCADABLE
- INTERNAL 55V INDUCTIVE LOAD CLAMP AND VGS PROTECTION CLAMP FOR EXTERNAL POWER FETS
- INDEPENDENT SHORTED-LOAD AND SHORT-TO-BATTERY FAULT DETECTION ON ALL GATE TERMINALS
- INDEPENDENT OFF-STATE OPEN-LOAD FAULT SENSE
- OVER-BATTERY-VOLTAGE LOCKOUT PROTECTION AND FAULT REPORTING
- UNDER-BATTERY VOLTAGE LOCKOUT PROTECTION
- ASYNCRONOUS OPEN-GATE FAULT FLAG
- DEVICE OUTPUT CAN BE WIRE ORED WITH MULTIPLE DEVICES
- FAULT STATUS RETURNED THROUGH SERIAL OUTPUT TERMINAL
- INTERNAL GLOBAL POWER-ON RESET OF DEVICE AND EXTERNAL RESET TERMINAL
- HIGH IMPEDANCE CMOS COMPATIBLE INPUTS WITH HYSTERESIS
- TRANSITION THE GATE OUTPUT TO A LOW DUTY CYCLE PWM MODE
- WHEN A SHORTED LOAD FAULT OCCURS



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DESCRIPTION

The STPIC44L02 is low-side predriver that provides serial and parallel input interfaces to control four external FET power switches.

They are mainly designed to provide low-frequency switching, inductive load applications such as solenoids and relays. Fault stauts is available in a serial-data format. Each driver channel has independent off-state open-load detection and on-state shorted load short to battery detection.

The STPIC44L02 offer a battery over voltage and undervoltage detection and shutdown. If a fault occurs while using the STPIC44L02, the channel transitions into a low duty cycle, pulse width modulated (PWM) signal as long as the fault is present.

These devices provide control of output channles through a serial input interface or a parallel input interface. A command to enable the output from either interface enables the respective channles gate output to the external FET. The serial interface is recommended when the number of signals between the control device and the predriver must be minimized and the speed of operation is not critical. In applcations where the predriver must respond very quickly or asyncrhronously, the parallel input interface is recommended.

For serial operation, the control device must transition $\overline{CS}$ from high to low to activate the serial input interface. When this occurs, SDO, is enabled, fault data is latched into the serial interface, and the fault flag is refreshed. Data is clocked into the serial registers on low to high transitions of SCLK through SDI. Each string of data must consist of at least four bits of data. In applications where multiple devices are cascated together, the string of data must consist of four bits for each device. A high data bit turns the respective output channel on and a low data bit turn it off. Fault data for the device is clocked out of SDO as serial input data is clocked into the device. Fault data consists of fault flags for shorted load and open load flags (bits 0-3) for each of the four output channels. Fault register bits are set or cleared asynchronously to reflect the current state of the hardware. A fault must be present when $\overline{CS}$ is transitioned from high to low to be captured and reported in the serial fault data. New faults cannot be captured in the serial register when $\overline{CS}$ is low. $\overline{CS}$ must be transitioned high after all of the serial data has been clocked into the devie. A lo to high transition of $\overline{CS}$

transfers the last four bits of serial data to the output buffer puts SDO in a high impedance state and clears and reenables the fault register. The STPIC44L02 was designed to allow the serial input interfaces of multiple devices to be cascated together to simplify the serial interface of the controller. Serial input data flows through the device and is transferred out SDO following the fault data in cascaded configurations.

For parallel operation, data is transferred directly from the parallel input interface IN0-IN3 to the respective GATE(0-3) output asynchronously. SCLK or $\overline{CS}$ is not required for parallel control. A 1 on the parallel intput turns the respective channel on, where a 0 turns it off. Note that either the serial input interface or the parallel input interface can enable a channel. Under parallel operation, fault data must still be collected through the serial data interface.

The predriver monitor the drain voltage for each channel to detect shorted load or open load fault conditions, in the on and off state respectively.

These devices offer the option of using an internaly generated fault reference voltage or an externally supplied fault reference voltage through V_{COMP} for fault detection. The internal fault reference is selected by connecting V_{COMPEN} to GND and the external reference is selected by connecting V_{COMPEN} to V_{CC}. The drain voltage is compared to the fault reference when the channel is turned on the detect shorted load conditions and when the channel is off to detect open load conditions. If a fault occurs, the channel transitions into a low duty cycle, pulse width modulated (PWM) signal as long as the fault is present. Shorted load fault conditions must be present for at least the shorted load deglicth time, $t_{(STBDG)}$, to be flagged as a fault. A fault flag is sent to the control device as well as the serial fault register bits. More detail on fault detection operation is presented in the device operation section of this data sheet.

The device provide protection from over battery voltage and under battery voltage conditions irrespecive of the state of the output channels. When the battery voltage is greater than the overvoltage threshold or less than the undervotlage threshold, all channels are disabled and a fault flag is generated. Battery voltage faults are not reported in the serail fault data. The outputs return to normal operation once the battery voltage fault has been corrected. When an over battery/under battery voltage condition occurs, the device reports the battery fault, but disables fault reporting for open and shorted load conditions. Fault reporting for open and shorted load conditions are reenables after the battery fault condition has been corrected.

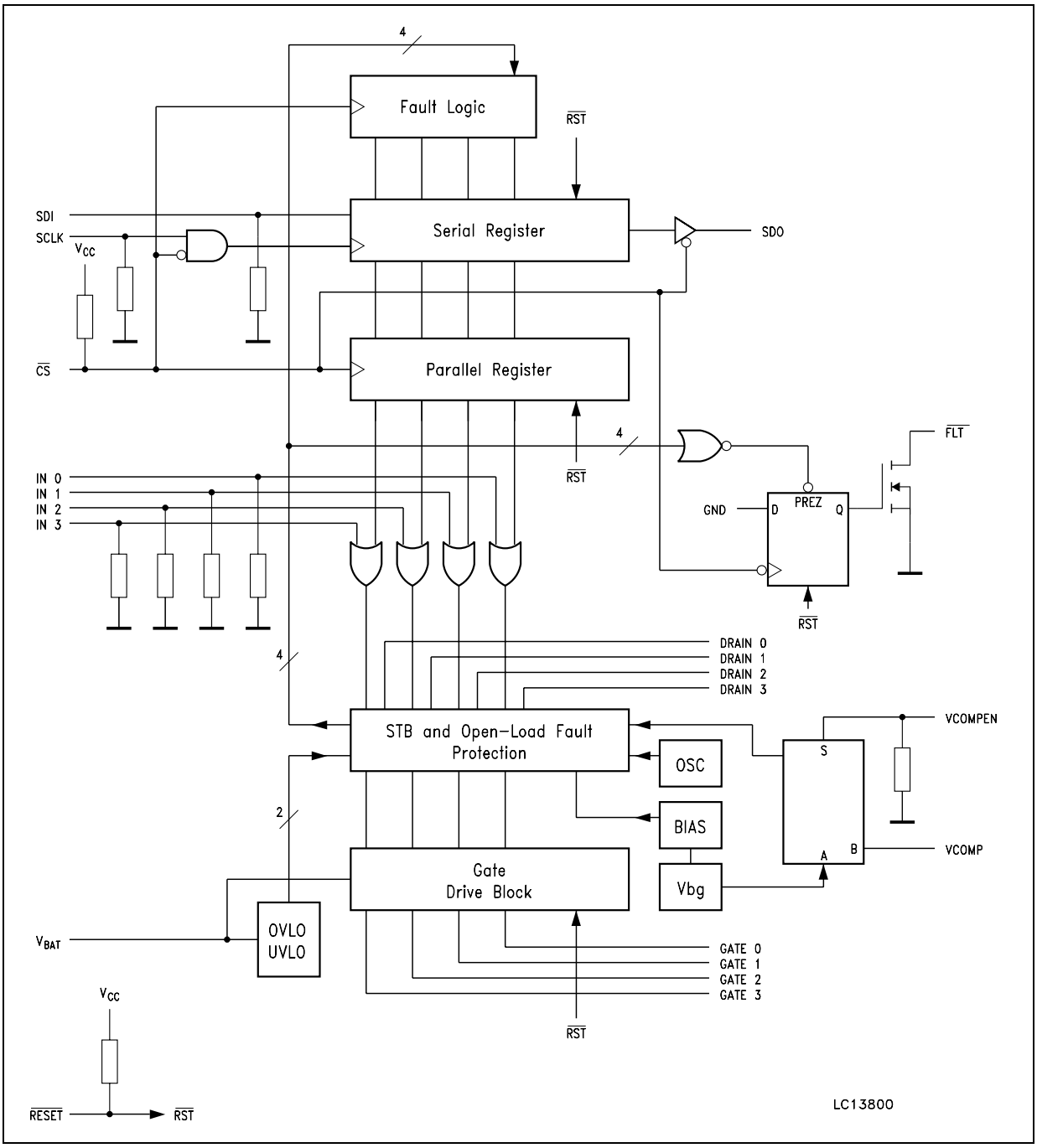
This device provide inductive transient protection on all channels. The drain voltage is clamped to protect the FET. The clamp voltage is defined by the sum of V_{CC} and turnon voltage of the external FET. The predriver also provides a gate to source voltage (V_{GS}) clamp to protect the gate source terminals of the power FET from exceeding their rated voltages. An external ective low $\overline{RESET}$ is provided to clear all register and flags in the device. GATE(0-3) outputs are disabled after RESET has been pulled low.

The device provide pulldown resistors on all inputs except $\overline{CS}$ and $\overline{RESET}$. A pullup resistor is used on $\overline{CS}$ and $\overline{RESET}$.

ORDERING CODES

Type	Package	Comments
STPIC44L02PTR	SSOP24 (Tape & Reel)	1350 parts per reel

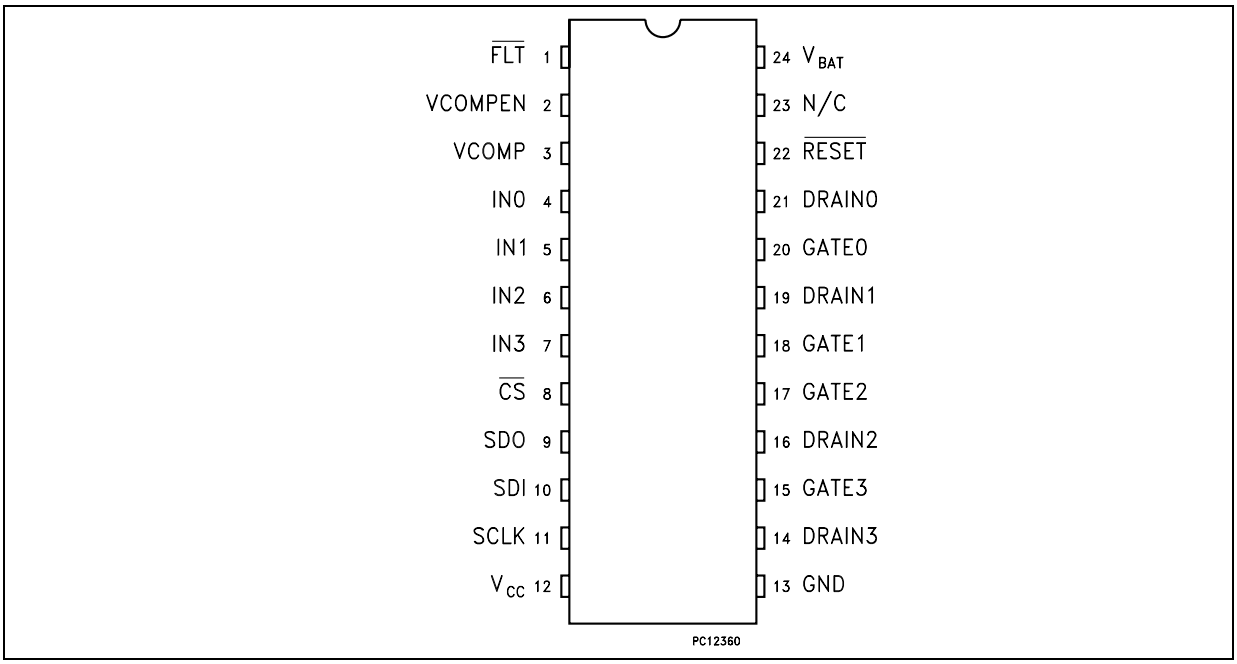
Figure 1 : Schematic Diagram



PIN DESCRIPTION

PIN No	SYMBOL	I/O	NAME AND FUNCTION
1	$\overline{FLT}$	I	Fault Flag. FLT is a logic level open-drain output that provides a real time fault flag for shorted-load, open-load, over-battery voltage, under-battery voltage faults. The device can be ORed with FLT terminals on other devices for interrupt handling. FLT requires an external pullup resistor.
2	VCOMPEN	I	Fault reference voltage select. VCOMPEN selecs the internally generated fault reference voltage (0) or an external fault reference (1) to be used in the shorted and open load fault detection circuitry.
3	VCOMP	I	Fault reference voltage. VCOMP provides an external fault reference voltage for the shorted-load and open oad fault detection circuitry.
4 5 6 7	IN0 IN1 IN2 IN3	I	Parallel gate driver. IN0 trough In3 are real-time controls for the gate predrive circuitry. They are CMOS compatible with hysteresis.
8	$\overline{CS}$	I	Chip select. A high to low transition on $\overline{CS}$ enables SDO, latches fault data into the serial interface, and refreshes FLT. When CS is high, the fault register can change fault status. On the falling edge of $\overline{CS}$, fault data is latched into the serial output register and transferred using SDO and SCLK. On a low to high transition of $\overline{CS}$, serial data is latched in to the output control register.
9	SDO	O	Serial data output. SDO is a 3-state output that transfers fault data to the controlling device. It also passes serial input data to the next stage for cascaded operation. SDO is taken to a high-impedance state when $\overline{CS}$ is in a high state.
10	SDI	I	Serial data input. Output control datat is clocked into the serial register through SDI. A 1 on SDI commands a particular gate output on and a 0 turns it off.
11	SCLK	I	Serial clock. SCLK clocks the shift register. Serial data is clocked into SDI and serial fault data is clocked out of SDO on the falling edge of the serial clock.
12	V_{CC}	I	Logic Supply Voltage
13	GND	I	Ground
14 16 19 21	DRAIN0 DRAIN1 DRAIN2 DRAIN3	I	FET drai inputs. DRAIN0 through DRAIN3 are used for both open load and short circuit fault detection at the drain of the external FETs. They are also used for inductive transient protection.
15 17 18 20	GATE0 GATE1 GATE2 GATE3	O	Gate drive output. GATE0 through GATE3 outputs are derived from the V_{BAT} supply voltage. Intenal clamps prevent voltages on these nodes from exceeding the VGS rating of most FETs.
22	$\overline{RESET}$	I	Reset. A high-to low transition of $\overline{RESET}$ clears all registers and flags. Gate outputs turn off and the $\overline{FLT}$ flag is cleared.
23	NC		Not Connected
24	V_{BAT}	I	Battery Supply Voltage

Figure 2 : Pin Configuration



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Logic Supply Voltage (See Note 1)	-0.3 to 7	V
V_{BAT}	Battery Supply Voltage	-0.3 to 60	V
V_I	Logic Input Voltage Range	-0.3 to 7	V
V_O	Output Voltage (SDO and $\overline{FLT}$)	-0.3 to 7	V
V_O	Output Voltage	-0.3 to 15	V
V_I	Logic Input Voltage Range	-0.3 to 7	V
V_{DS}	Drain to Source Voltage	-0.3 to 60	V
T_C	Operating Case Temperature Range	-40 to +125	°C
T_J	Maximum Junction Temperature	150	°C
T_{stg}	Storage Temperature Range	-40 to +150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

Note 1: All voltage value are with respect to GND

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Min.	Max.	Unit
V_{CC}	Logic Supply Voltage	4.5	5	5.5	V
V_{BAT}	Battery Supply Voltage	8		24	V
V_{IH}	High Level Input Voltage	$0.85V_{CC}$		V_{CC}	V
V_{IL}	Low Level Input Voltage	0		$0.15V_{CC}$	V
t_s	Set-up Time, SDI High Before SCLK ↑	10			ns
t_h	Hold Time, SDI High After SCLK ↑	10			ns
T_C	Operating Case Temperature	-40		125	°C

ELECTRICAL CHARACTERISTICS OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE (unless otherwise specified.)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
I_{BAT}	Supply Current	All Outputs OFF,	V_{BAT} = 12V	50	150	250	µA
I_{CC}	Supply Current	All Outputs OFF,	V_{BAT} = 5.5V	0.5	1.5	3	mA
$V_{(ovsd)}$	Over Battery Voltage Shutdown	Gate Disabled	(see figure 21)	32	34	36	V
$V_{hys(ov)}$	Over Battery Voltage Reset Hysteresys			0.1	0.3	0.5	V
$V_{(uvsd)}$	Under Battery Voltage Shutdown	Gate Disabled	(see figure 20)	4.1	4.8	5.4	V
$V_{hys(uv)}$	Under Battery Voltage Reset Hysteresys			50	150	300	mV
V_G	Gate Drive Voltage	V_{BAT} = 8 to 24V	I_O = 100µA	7		13.5	V
		V_{BAT} = 5.5 to 8V	I_O = 100µA	5		8	V
$I_{O(H)}$	Maximum Current Output For Drive Terminal Pull-Up	V_O = GND		0.5	1.8	2.5	mA
$I_{O(L)}$	Maximum Current Output For Drive Terminal Pull-Down	V_O = 7V		0.5	1.2	2.5	mA
$V_{(stb)}$	Short to Battery, Shorted Load, Open Load Detection Voltage	V_{COMPEN} = L		1.1	1.25	1.4	V
$V_{hys(stb)}$	Short to Battery Hysteresys				30		mV
$V_{D(open)}$	Open Load OFF State Detection Voltage Threshold	V_{COMPEN} = L		1.1	1.25	1.4	V
$V_{hys(open)}$	Open Load Hysteresys				60		mV
$I_{I(open)}$	Open Load Off State Detection Current	V_{DRAIN} = V_{REF} = 1.25V		30	60	80	µA
		V_{DRAIN} = 24V	(see figure 24)		250		µA
$I_{I(PU)}$	Input Pull-up Current	V_{CC} = 5V	V_I = 0		10		µA
$I_{I(PD)}$	Input Pull-down Current	V_{CC} = 5V	V_I = 5V		10		µA
V_{hys}	Input Voltage Hysteresys	V_{CC} = 5V		0.6	0.85	1.1	V
$V_{O(SH)}$	High Level Serial Output Voltage	I_O = 1mA		0.8V_{CC}			V
$V_{O(SL)}$	Low Level Serial Output Voltage	I_O = 1mA			0.1	0.4	V
$I_{OZ(SD)}$	3-State Current Serial Data Output	V_{CC} = 0 to 5.5V		-10	1	10	µA
$V_{O(CFLT)}$	Fault Interrupt Output Voltage	I_O = 1mA			0.1	0.5	V
$V_{I(COMP)}$	Fault External Reference Voltage	V_{COMPEN} = H		1		3	V
V_C	Output Clamp Voltage	dc < 1%	t_W = 100µs	47	55	63	V

SWITCHING CHARACTERISTICS (V_{CC}=5V, V_{BAT}=5V, T_C= 25°C, unless otherwise specified.)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{(STBFM)}$	Short to Battery, Shorted Load, Open Load Fault Mask Time	(see figures 16, 17)		60		µs
$t_{(STBDG)}$	Short to Battery, Shorted Load, Deglitch Time	(see figures 16, 17)		12		µs
t_{PLH}	Propagation Turn-On Dealy Time, $\overline{CS}$ or IN0-IN3 to Gate0-Gate3	$C_{(gate)}$ = 400pF		3.5		µs
t_{PHL}	Propagation Turn-Off Dealy Time, $\overline{CS}$ or IN0-IN3 to Gate0-Gate3	$C_{(gate)}$ = 400pF		4		µs
t_{r1}	Rise Time, Gate0-Gate3	$C_{(gate)}$ = 400pF		1.5		µs
t_{f1}	Fall Time, Gate0-Gate3	$C_{(gate)}$ = 400pF		2		µs
$f_{(SCLK)}$	Serial Clock Frequency				10	MHz
$t_{rf(SB)}$	Refresh Time Short to Battery	(see figure 16)		10		ms
$t_{W)}$	Refresh pulse width Short to Battery	(see figure 16)		68		µs
t_{su1}	Setup Time $\overline{CS}\downarrow$ to SCLK $\downarrow$	(see note 1) (see figure 4)		10		ns
t_{pd1}	Propagation Delay Time $\overline{CS}$ to SDO Valid	R_L = 10KΩ C_L = 200pF (see figure 6)		40		ns
t_{pd2}	Propagation Delay Time SCLK to SDO Valid			20		ns
t_{pd3}	Propagation Delay Time CS to SDO 3-State	R_L = 10KΩ C_L = 50pF (see figure 6)		2		µs
t_{r2}	Rise Time, SDO 3-State to SDO Valid	R_L = 10KΩ to GND C_L = 200pF Over Battery Fault (see figure 7)		30		ns
t_{f2}	Fall Time, SDO 3-State to SDO Valid	R_L = 10KΩ to GND C_L = 200pF No Fault (see figure 8)		20		ns
t_{r3}	Rise Time, FLT	R_L = 10KΩ C_L = 50pF (see figure 9)		1.2		µs
t_{f3}	Rise Time, FLT	R_L = 10KΩ C_L = 50pF (see figure 9)		15		ns

Note 1: The t_{d1} is refered to the falling edge of the first clock after the $\overline{CS}$ falls down

Figure 3 : Switching Time

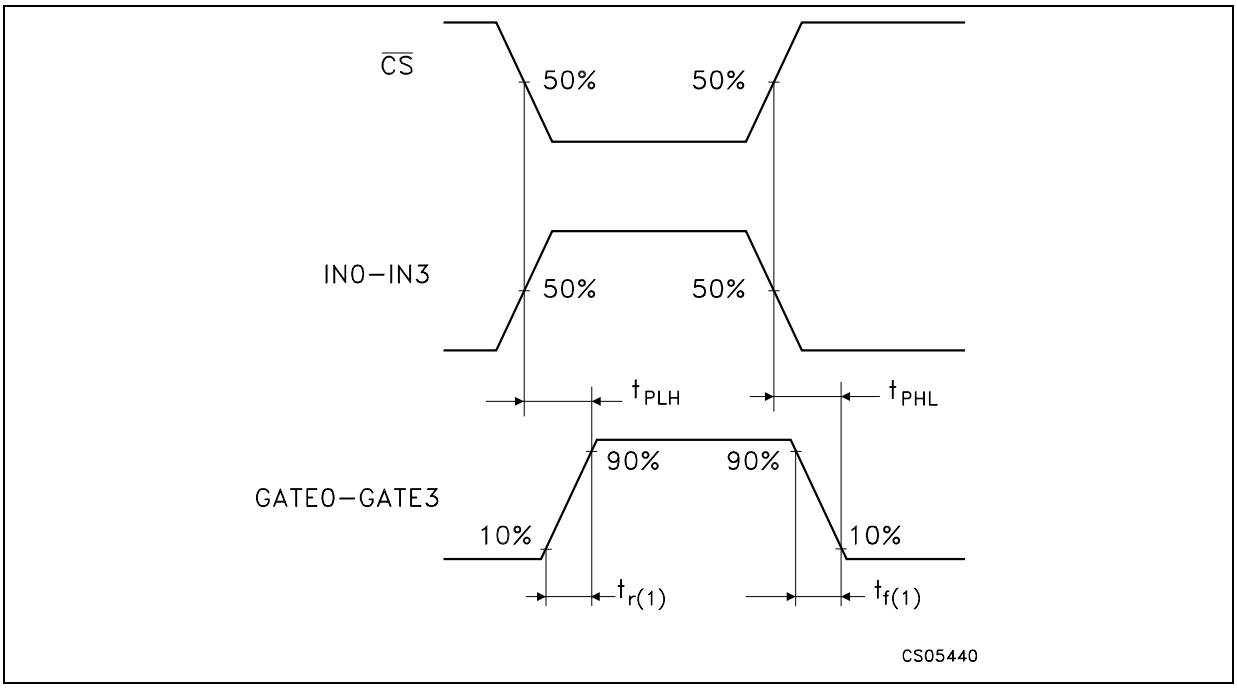


Figure 4 : Setup Time $\overline{CS}$ ↓ to SCLK ↓

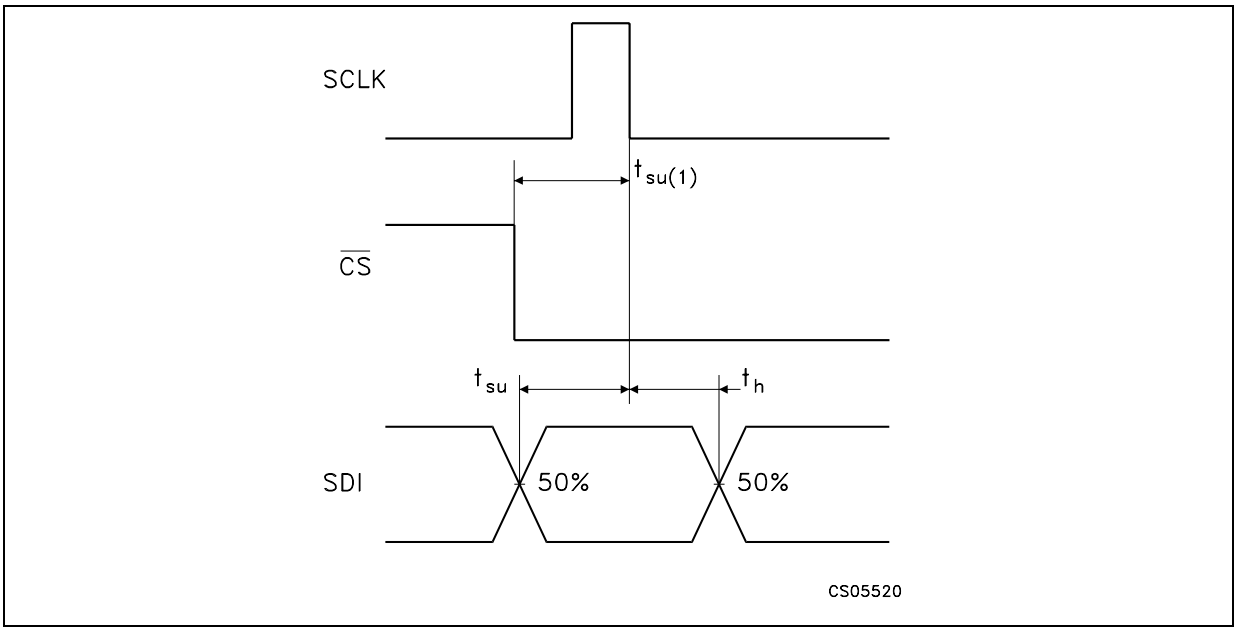


Figure 5 : Propagation Delay Time

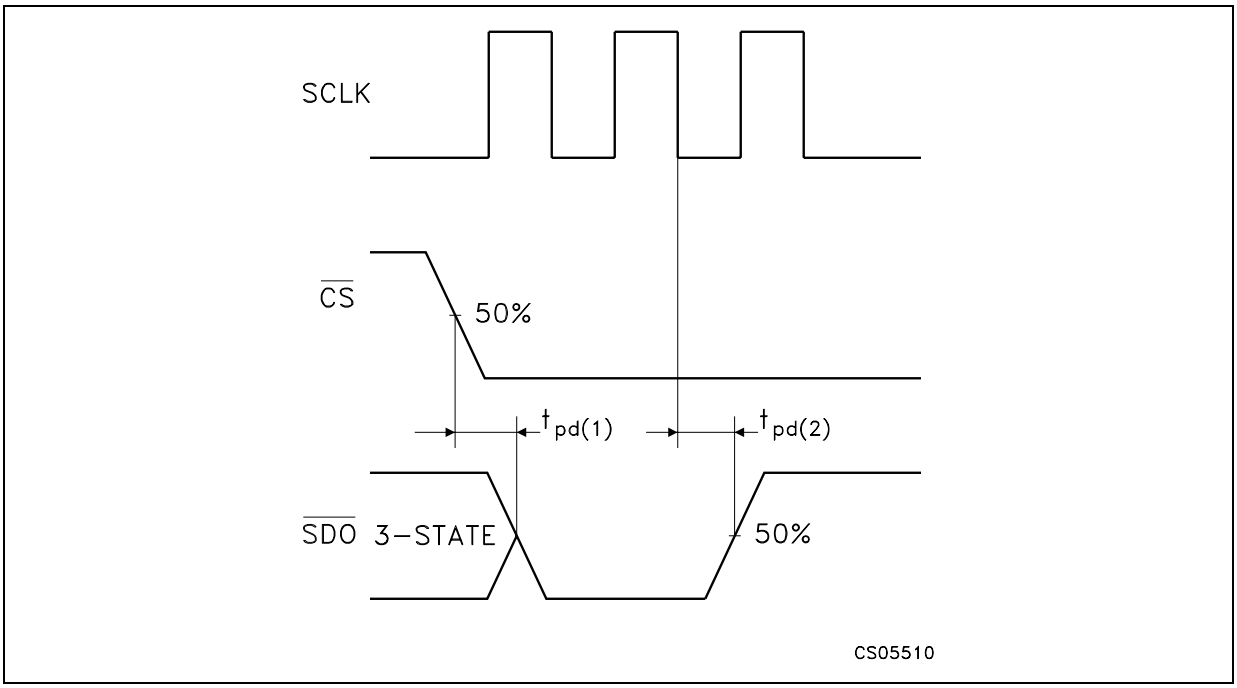


Figure 6 : Propagation Delay Time

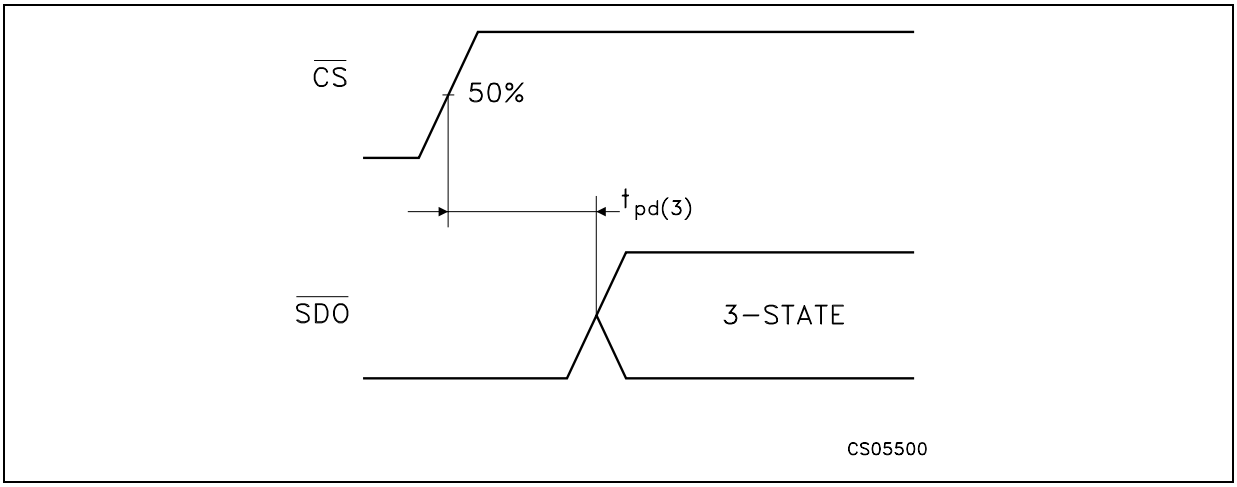


Figure 7 : SDO Switching Time

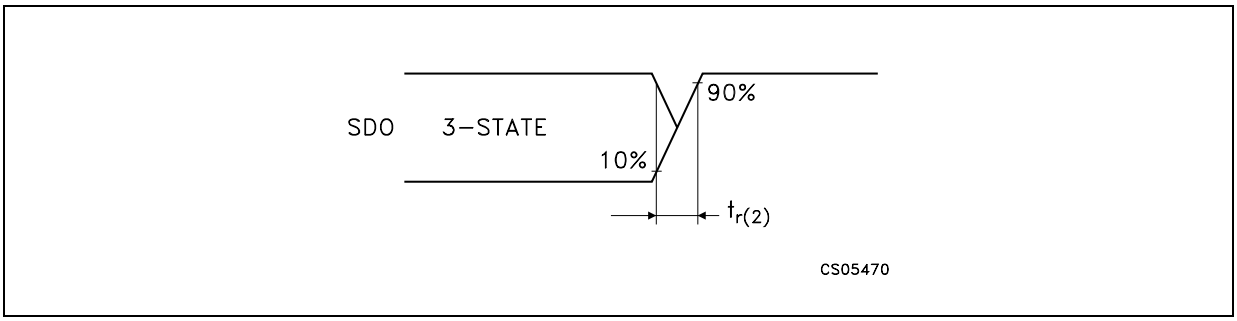


Figure 8 : SDO Switching Time

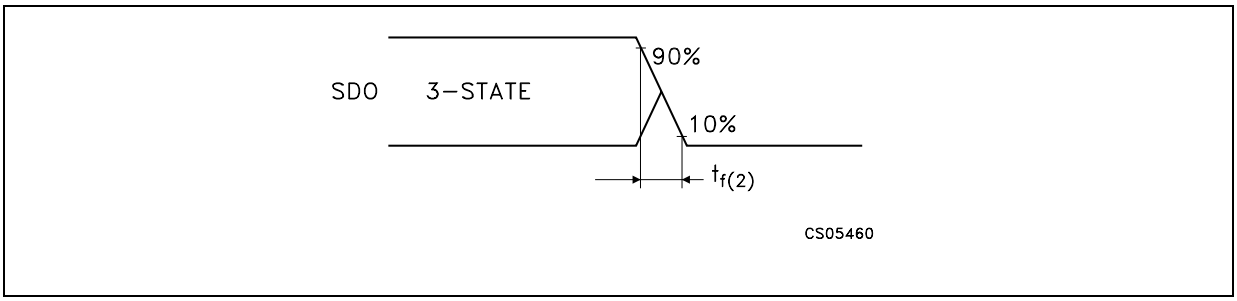
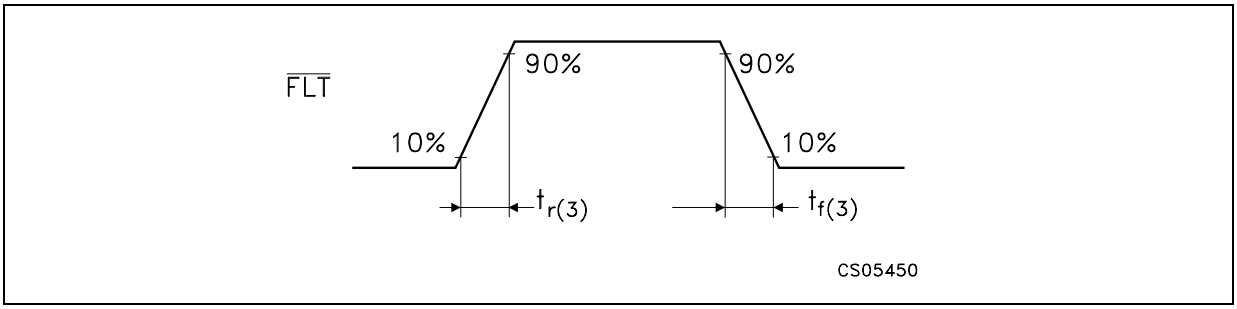


Figure 9 : $\overline{FLT}$ Switching Time



PRINCIPLES OF OPERATION

SERIAL DATA OPERATION

The STPIC44L02 offers serial input interface to the microcontroller to transfer control data to the predriver and fault data back to the controller. The serial input interface consists of:

SCLK - Serial Clock

$\overline{CS}$ - Chip Select

SDI - Serial Data Input

SDO - SeriaL Data Output

Serial data is shifted into the least significant bit (LSB) of the SDI shift register on the rising edge of the first SCLK after $\overline{CS}$ has transitioned from 1 to 0. The $\overline{CS}$ must be transitioned from 1 to 0 before the falling edge of the first clock (see note 1).

Four clock cycles must occur before $\overline{CS}$ transitions high for proper control of the outputs. Less than four clock cycles result in fault data being latched into the output control buffer.

Eight bits data can be shifted into the device, but the first 4 bits shifted out are always the fault data and the last 4 bits shifted in are alwys the output control data. A low-to-high transition on $\overline{CS}$ latches the contents of the serial shift register into the output control register. A logic 0 input to SDI turns the corresponding parallel output off and a logic 1 input turns the output on (see figure 10). Data is shifted out of SDO on the falling edge of SCLK. The MSB of fault data is available after $\overline{CS}$ is transitioned low. The remaining 3 bits of fault data are shifted out in the following three clock cycles. Fault data is latched into the serial resister when $\overline{CS}$ is transitioned low. A fault must be present on the high to low transition of $\overline{CS}$ to be captured by the device. The $\overline{CS}$ input must be transtioned to a high state after the last bit of serial data has been clocked into the device. the rising edge of $\overline{CS}$ inhibit SDI, put SDO into a high impedance state, latches the 4 bits of serial data into the output control register, and clear and reenable the serial fault registers (see figure 11). When a shorted load condition occurs, the device automatically retries the output and the fault clears after the fault condition has been corrected.

Figure 10 : Serial Programming Example

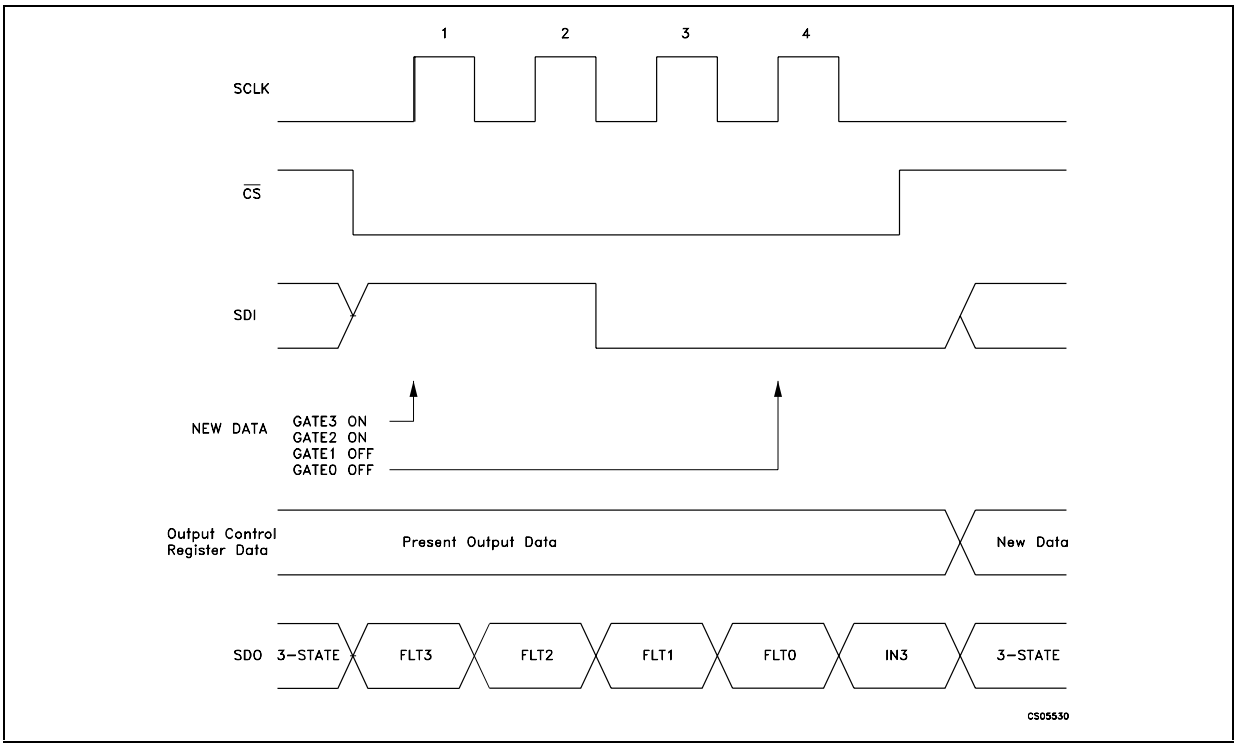


Figure 11 : 8-Bit Serial Programming Example (single device)

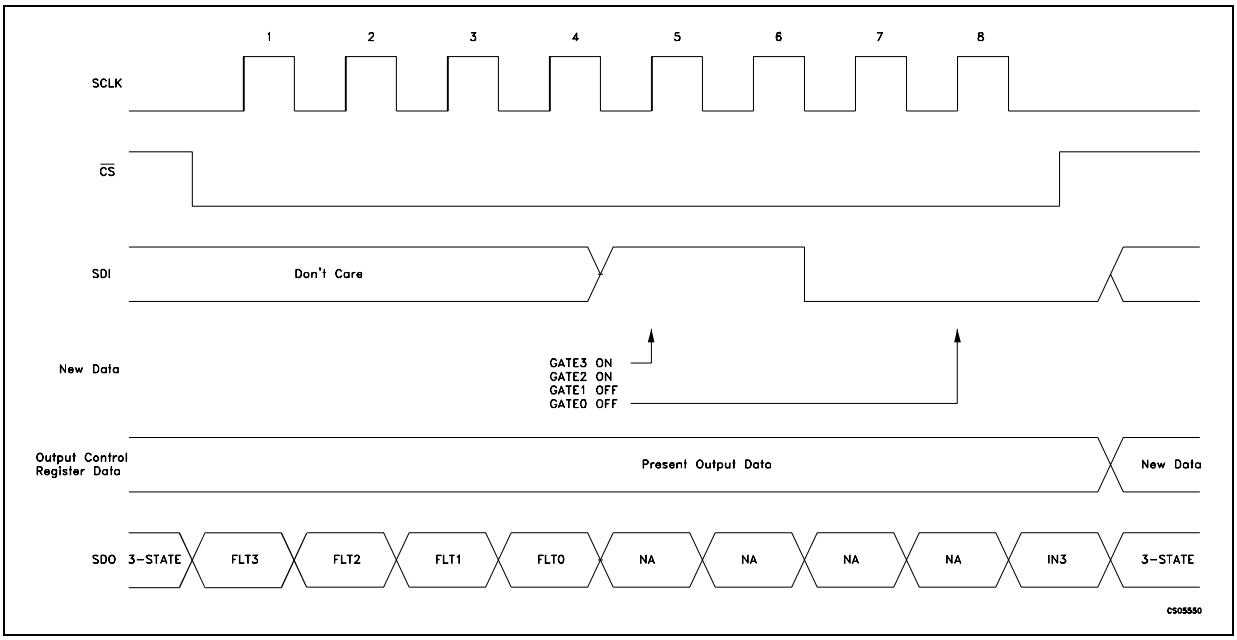


Figure 12 : 8-Bit Serial Programming Example (two predrivers cascated)

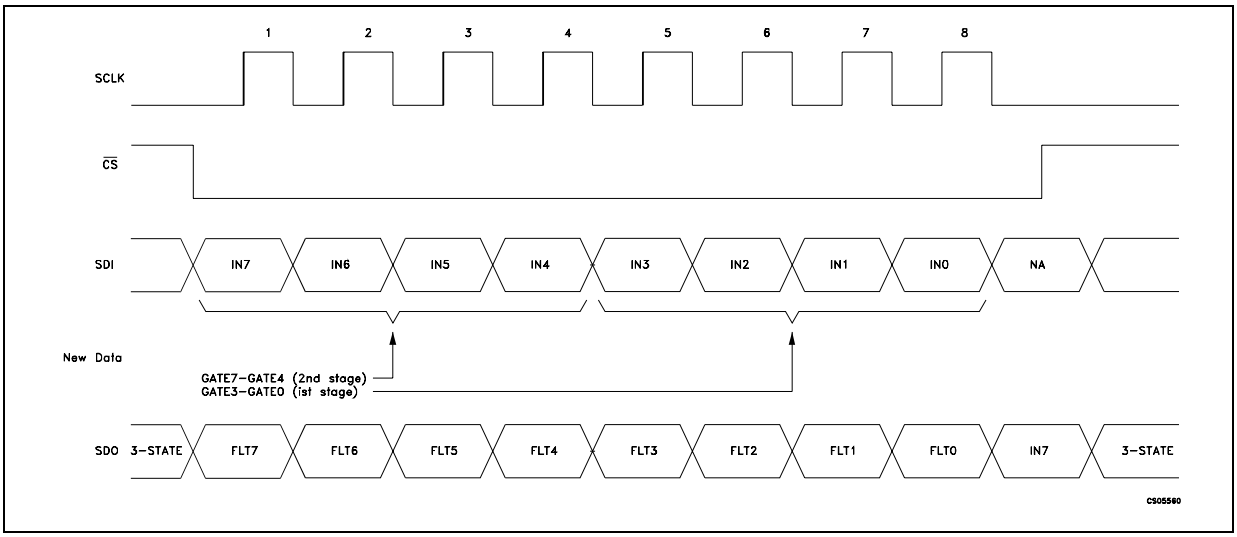
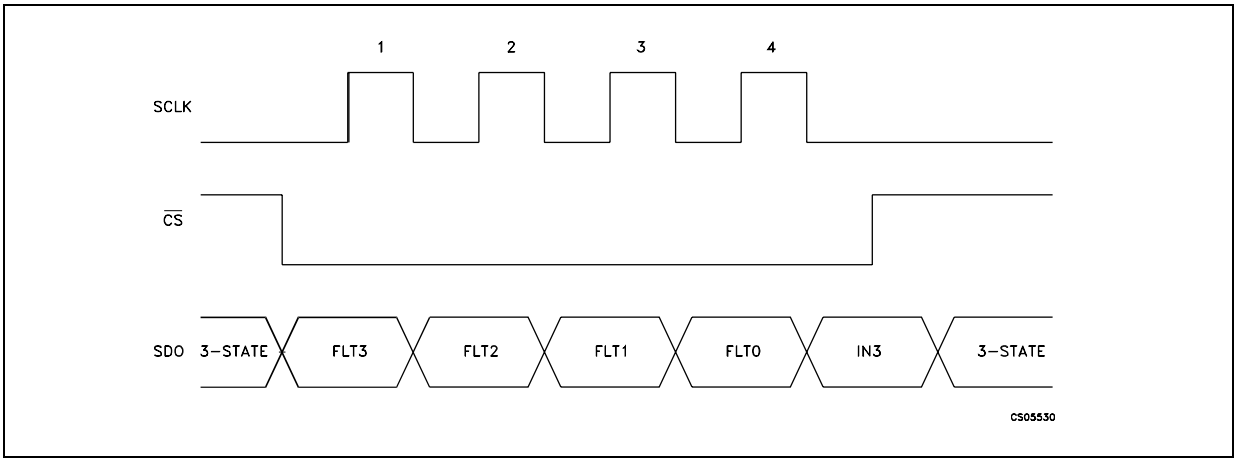


Figure 13 : Fault Reading Example



PARALLE INPUT DATA OPERATION

In addition to the serial interface the STPIC44L02 also provides a parallel interface to the microcontroller. The output turns on when either the parallel or the serial interface commands it to turn on. The parallel data terminals are real time control inputs for the outputs drivers. SCLK and CS are not required to transfer parallel input data to the output buffer. Fault data must be read over the serial data bus as described in the serial data operation section of this data sheet (see figure 13). The parallel input must be transitioned low and then high to clear and reenable a gate output after it has been disabled due to a shorted load fault condition.

CHIPSET PERFORMANCE UNDER FFAULT CONDITIONS

The STPIC44L02 and power FET arrays are designed for normal operation over a battery voltage range of 8V to 24V with load fault detection from 4.8V to 34V. It offer onboard fault detection to handle a variety of faults that may occur within a system. The circuits primary function is to prevent damage to the load and the power FETs in the event that a fault occurs.

Note that unused DRAIN0-DRAIN3 inputs must be connected to V_{BAT} through a pullup resistor to prevent false reporting of open load fault conditions. The circuitry detects the fault, shut off the output to the FET and reports the fault to the microcontroller. The primary faults under consideration are:

1) Shorted Load

2) Open Load

3) over battery voltage shutdown

4) Under battery voltage shutdown.

SHORTED LOAD FAULT CONDITION

The STPIC44L02 monitor the drain voltage of each channel to detect shorted load conditions. The onboard deglitch timer starts running when the gate output to the power FET transitions from the off state to the on state. The timer provides a 60µs deglitch time, $t_{(STBFM)}$, to allow the drain voltage to stabilize after the power FET has been turned on (see figure 16 and 17).
The deglitch delay time is only enabled for the first 60µs after the FET has been turned on. After the deglitch delay time, the drain voltage is checked to verify that it is less than the fault reference voltage. When it is greater than the reference voltage for at least the short to battery deglitch time, $t_{(STBDG)}$ FLT flags the microcontroller that a fault condition exists and gate output is automatically shut off until the error condition has been corrected.
An overheating condition on the FET occurs when the controller continually tries to reenable the output under shorted load fault conditions. When a shorted load fault is detected, the gate output is transitioned into a low duty cycle PWM signal to protect the FET from overheating. The PWM rate is defined as t(SB) and the pulse width is defined ad tW. The gate output remains in this state until the fault has been corrected or until the controller disables the gate output.
The microcontroller can read the serial port on the predriver to isolate which channel reported the fault condition.
Fault bits 0-3 distinguish faults for each of the output channels. When a shorted load occurs the STPIC44L02 automatically retries the output and the fault cleras after the fault condition has been corrected. Figure 16 illustrates operation after a gate output has been turned on. The gate to the power FET is turned on and the deglitch timer starts running, Under normal opertaion T1 turn on and the drain operates below the reference point set at U1. The output of U1 is low and a fault condition is not flagged.

Figure 14 : Open Load Test Circuit

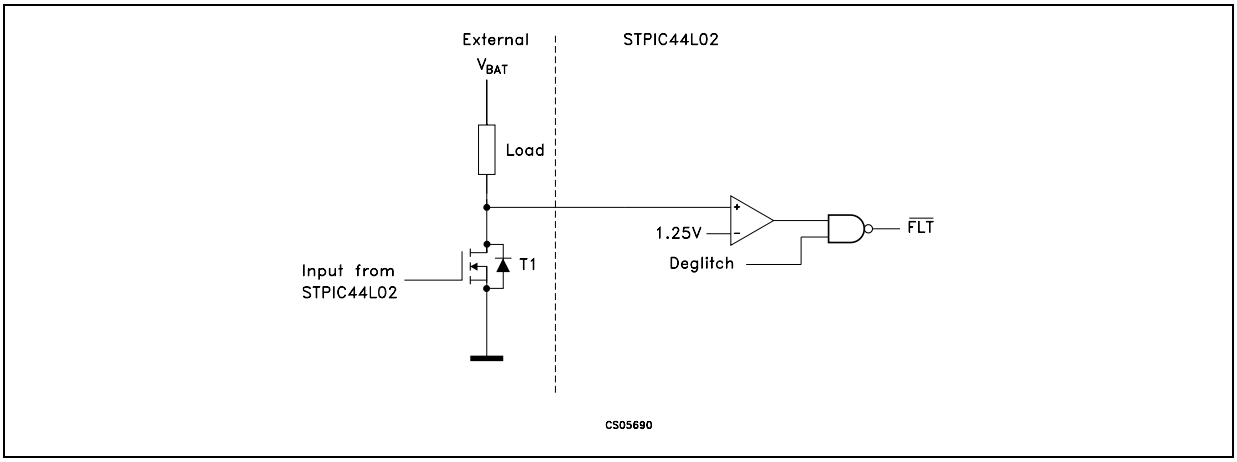


Figure 15 : Normal Operation

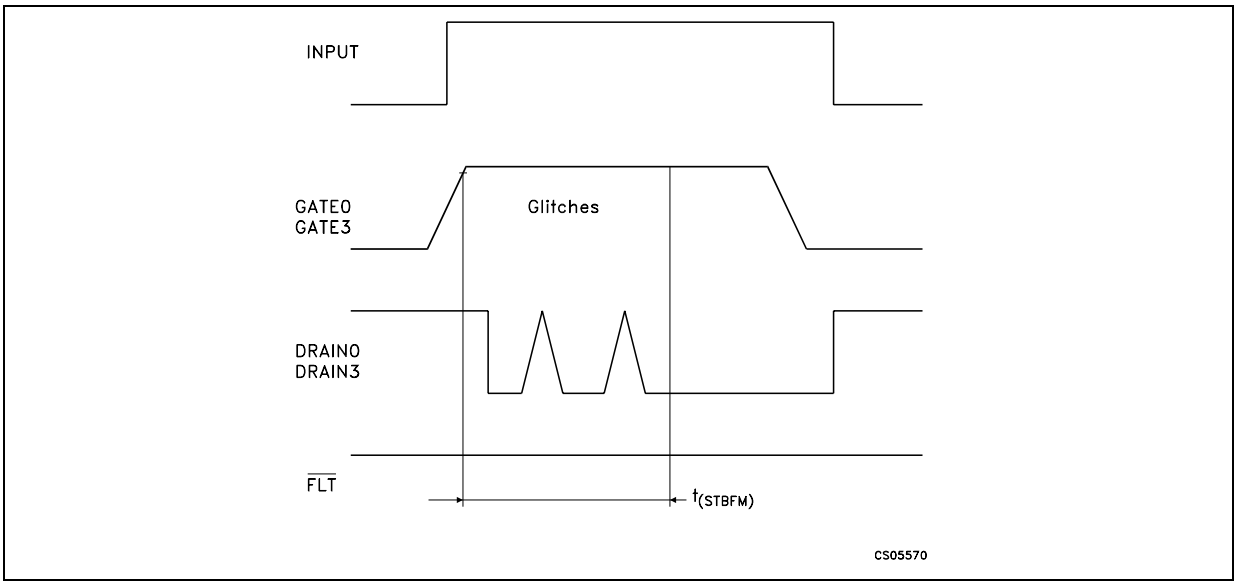
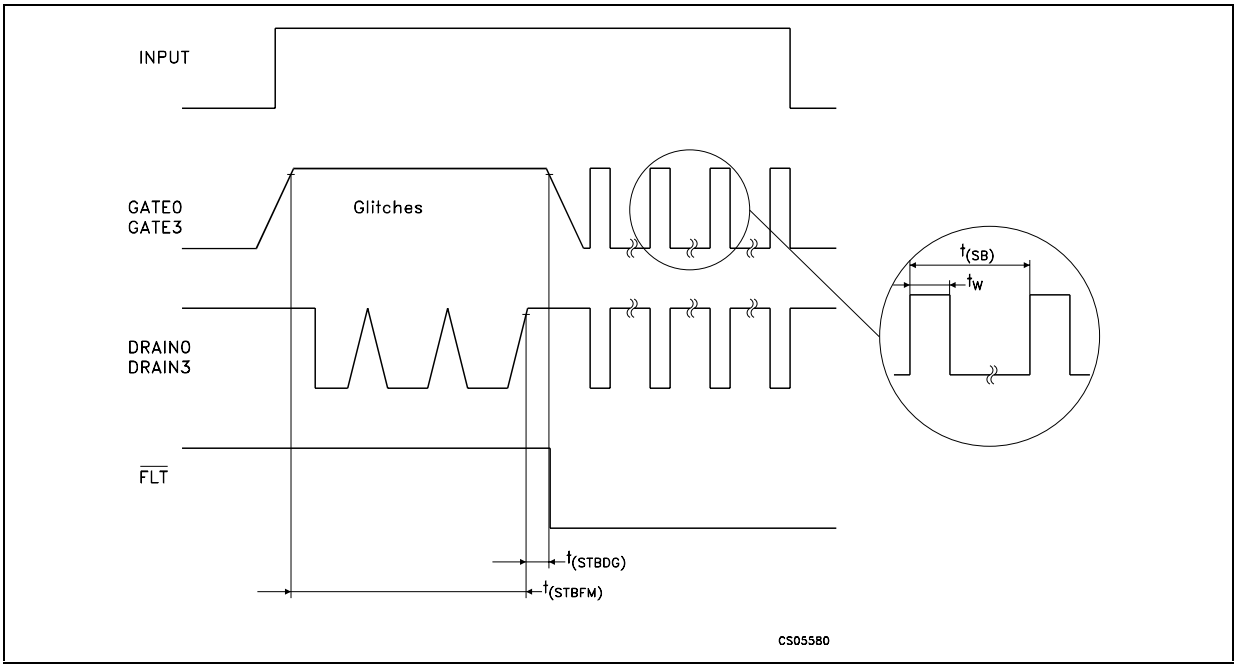


Figure 16 : Shorted Load Condition (Deglitch Time)



OPEN LOAD

The STPiC44L02, monitor the drain of each power FET for open circuit conditions that may exist. The 60µA current source is provided to monitor open load fault conditions. Open-load faults are only detected when the power FET is turned off. When load impedance is open or substantially high, the 60mA current source has adequate drive to pull the drain of T1 below the fault reference threshold on the detection circuit. Unused DRAIN0-DRAIN3 inputs must be connected to V_{BAT} through a pull-up resistor to prevent false reporting of open-load fault conditions. The on-board deglitch timer starts running when the STPiC44L02, gate output to the power FET transitions to the off state. The timer provides a 60ms deglitch time, $T_{(STBFM)}$ to allow the drain voltage to stabilize after the powerFET has been turned off. The deglitch time is only enabled for the first 60ms after the FET has been turned off. After

the deglitch delay time, the drain is checked to verify that it is greater than the fault reference voltage. When it is less than the reference voltage, a fault is flagged to the microcontroller through FLAT that an open-load fault condition exists. The microcontroller can then read the serial port on the STPiC44L02 to isolate which channel reported the fault condition. Fault bits 0-3 distinguish faults for each of the output channels. Figures 18 and 19 illustrate the operation of the open-load detection circuit. This feature provides useful information to the microcontroller to isolate system failures and warn the operator that a problem exists. Examples of such applications would be a warning that a light bulb filament may be open, solenoid coils may be open, etc.

Figure 17 : Open Load Short Ciruit test Circuitry

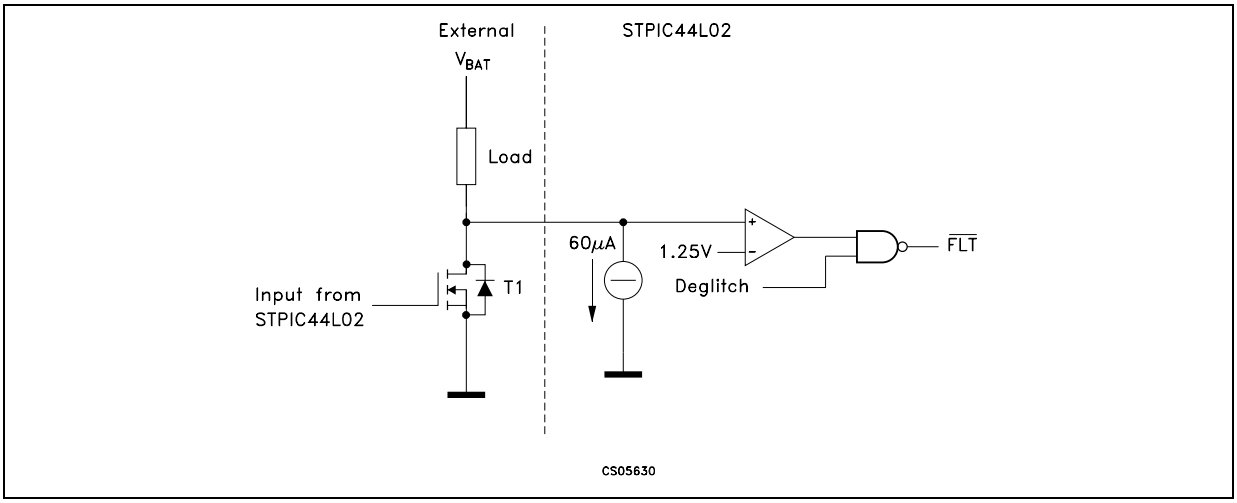


Figure 18 : Normal Condition Driving Load

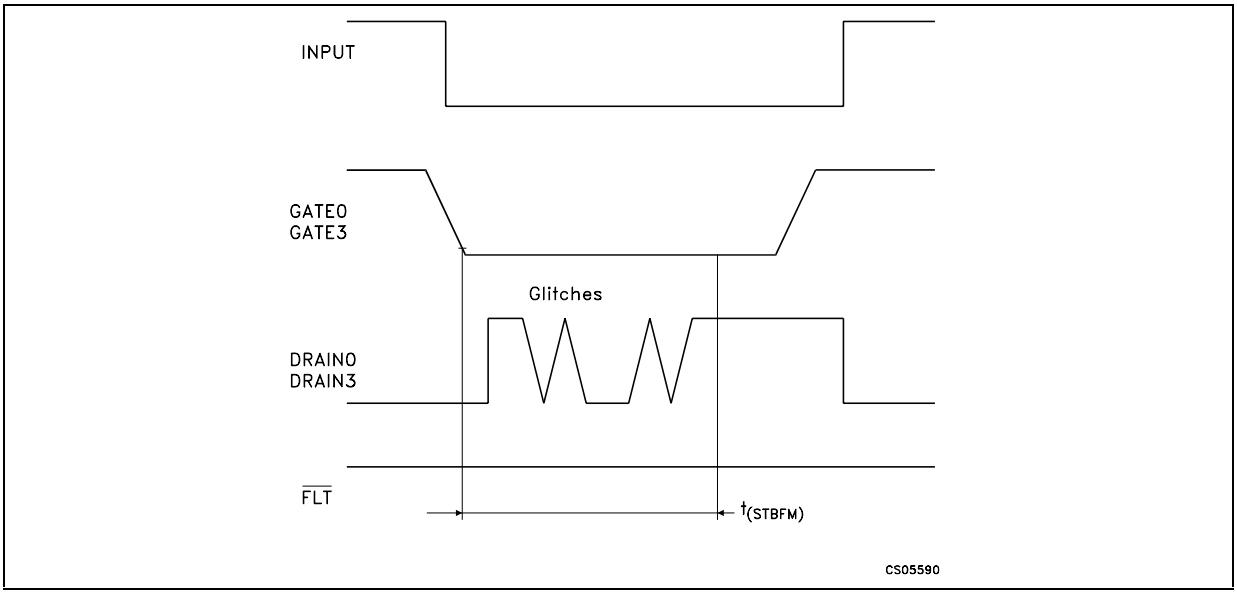
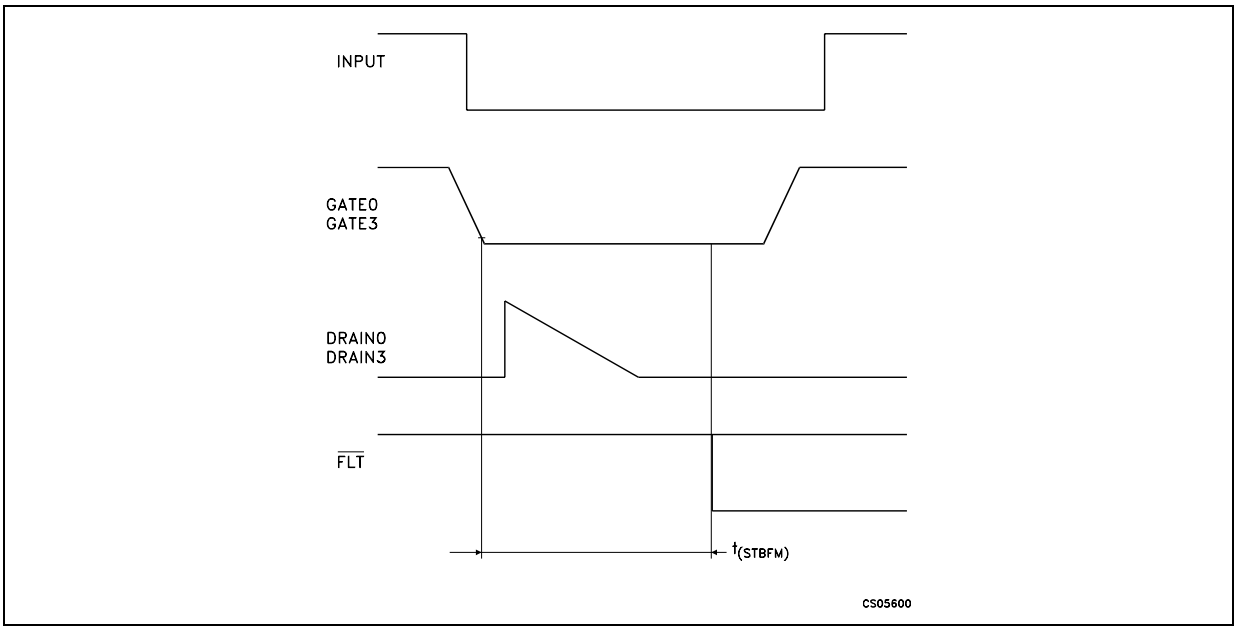


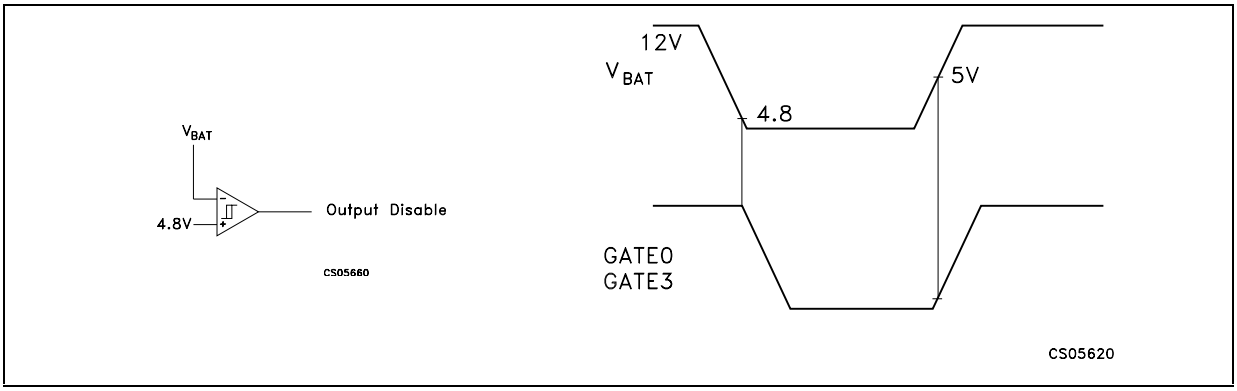
Figure 19 : Open Load ConditionTime



OVER-BATTERY-VOLTAGE SHUTDOWN

The STPIC44L02, monitor the battery voltage to prevent the power FETs turning on in the event that the battery voltage is too high. This condition may occur due to voltage transients resulting from a loose battery connection. The TPIC44L02 turns the power FET off when the battery voltage is above 34V to prevent possible damage to the load and the FET. GATE(0-3) output goes back to normal operation after the overvoltage condition has been corrected. An over-battery-voltage fault is flagged to the controller through $\overline{FLT}$. The over-battery-voltage fault is not reported in the serial fault word. When an over voltage condition occurs, the device reports the battery fault, but disables fault reporting for open and shorted-load conditions. Fault reporting for open and shorted-load conditions are re-enabled after the battery fault condition has been corrected. When the fault condition is removed before the $\overline{CS}$ signal transitions low, the fault condition is not captured in the serial fault register. The fault flag resets on a high-to-low transition of $\overline{CS}$ provided no other faults ere present in the device. Figure 21 illustrates the operation of the over-battery voltage detection circuit.

Figure 20 : Under Battery Shutdown

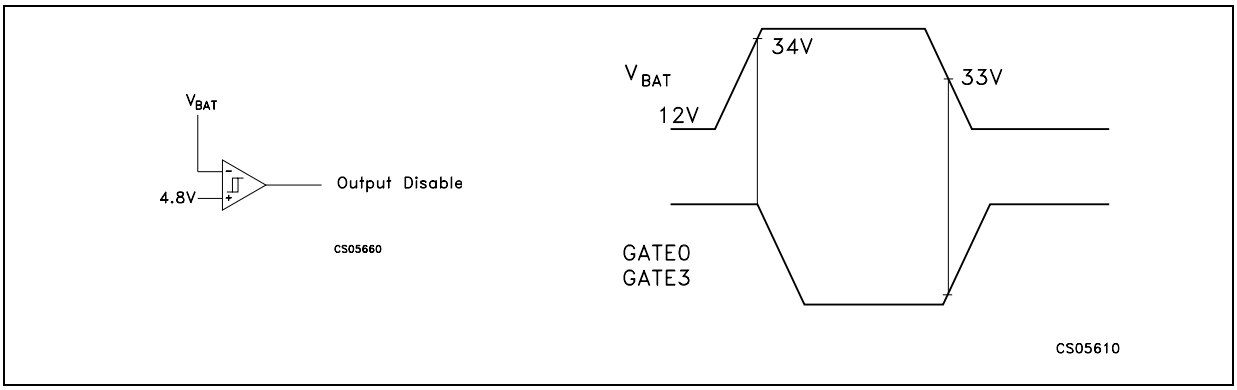


UNDER-BATTERY-VOLTAGE SHUTDOWN

The STPIC44L02 monitor the battery voltage to prevent the power FETs from being turned on in the event that the battery voltage is too low. When the battery voltage is below 4.8V, then GATE0-GATE3 may not provide sufficient gate voltage to the power FETs to minimize the on-resistance that could result in a thermal stress on the FET. The output goes back to normal operation after the under voltage condition has

been corrected. An under-battery-voltage fault is flagged to the controller through FLT. The under-battery voltage fault is not reported in the serial fault word. When an under-battery-voltage condition occurs, the device reports the battery fault but disables fault reporting for open and shorted load conditions. When the fault condition is removed before the $\overline{CS}$ signal transitions low, the fault condition is not captured in the serial fault register. The fault flag resets on a high-to-low transition of $\overline{CS}$ provided no other faults are present in the device. Figure 21 illustrates the operation of the under voltage detection circuit.

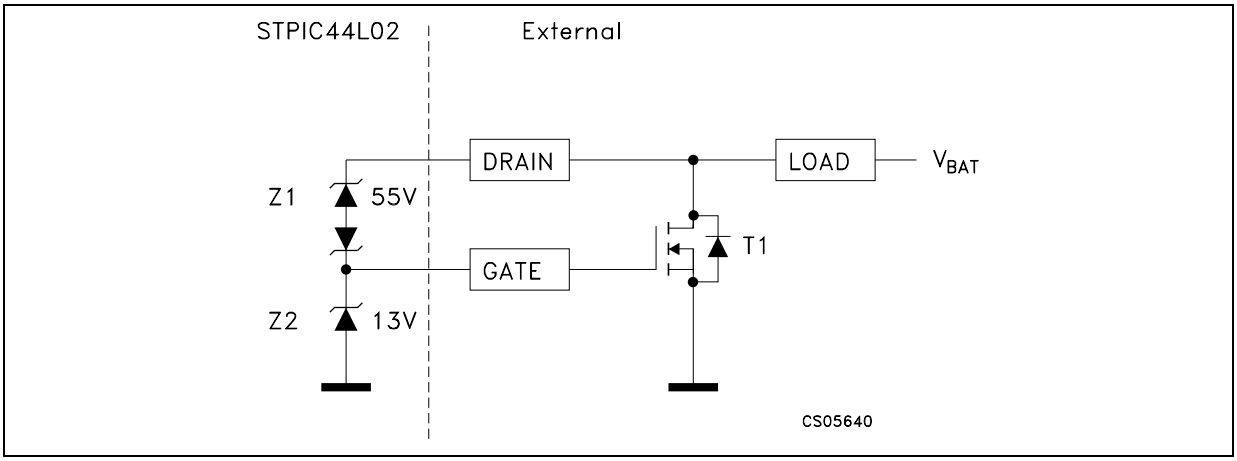
Figure 21 : Over Battery Shutdown



INDUCTIVE VOLTAGE TRANSIENTS

A typical application for the pre driver/power FET circuit is to switch inductive loads. When an inductive load is switched off, a large voltage spike can occur. These spikes can exceed the maximum V_{DS} rating for the external FET and damage the device when the proper protection is not in place. The FET can be protected from these transients through a variety of methods using external components.
The STPIC44L02 offers that protection in the form of a zener diode stack connected between the DRAIN input and GATE output (see figure 22). Zener diode Z1 turns the FET on to dissipate the transient energy. GATE diode Z2 is provided to prevent the gate voltage from exceeding 13V during normal operation and transient protection.

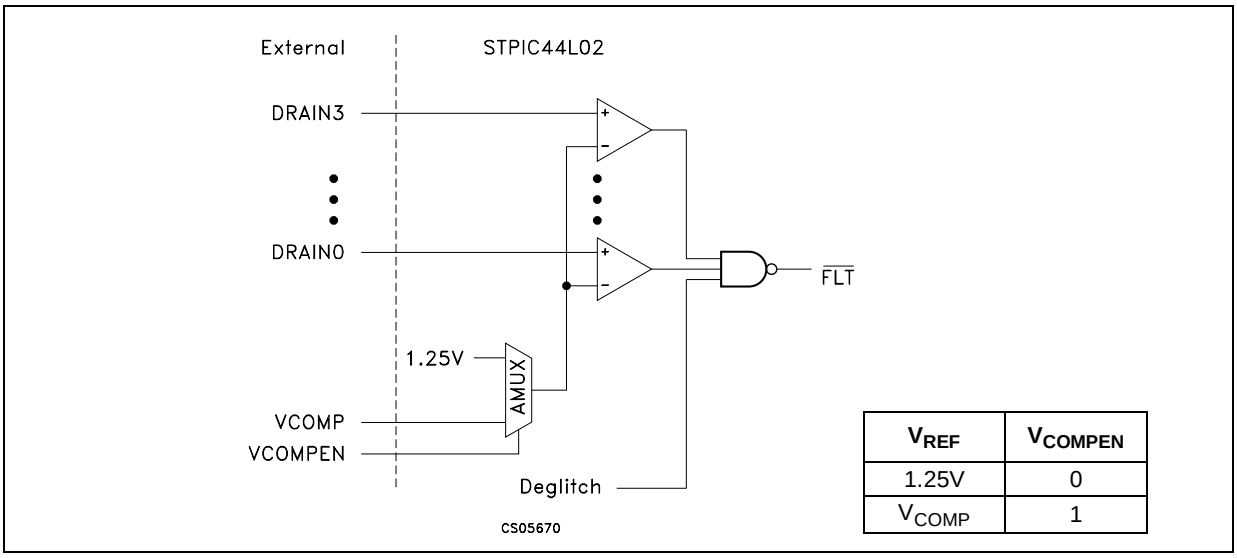
Figure 22 : Switching Time



EXTERNAL FAULT REFERENCE INPUT
The STPIC44L02 compare each channel drain voltage to a fault reference to detect shorted-load and open-load conditions. The user has the option of using the internal generated 1.25V fault reference or providing an external reference voltage through V_{COMP}. The internal reference is selected by connecting V_{COMPEN} to GND and V_{COMP} is selected by connecting V_{COMPEN} to V_{CC} (see Figure 23). Proper layout techniques should be used in the grounding network for the V_{COMP} circuit on the STPIC44L02. The ground for the

predriver and V_{COMP} network should be connected to a Kelvin ground if available; otherwise, they should make single-point contact back to the power ground of the FET array. Improper grounding techniques can result in inaccuracies in detecting faults.

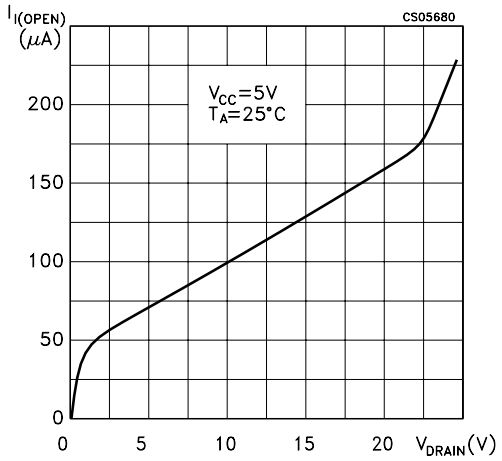
Figure 23 : External Reference Selection



V_{REF}	V_{COMPEN}
1.25V	0
V_{COMP}	1

TYPICAL PERFORMANCE CHARACTERISTICS (unless otherwise specified T_j = 25°C)

Figure 24 : Open Load Off State Detection Current



SSOP24 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			2			0.079
A1			0.25			0.010
A2	1.51		2.00	0.059		0.079
b	0.25	0.30	0.35	0.010	0.012	0.014
c	0.10		0.35	0.004		0.014
D	8.35		9.35	0.329		0.368
E	7.6		8.7	0.246	0.252	0.256
E1	5.02	6.10	6.22	0.198	0.240	0.245
e		0.65 BSC			0.0256 BSC	
K	0°		10°	0°		10°
L	0.25	0.50	0.80	0.010	0.020	0.031