VITESSE
SEMICONDUCTOR CORPORATION

Data Sheet
FX Family

High Performance
FX Family Gate Arrays

Features

- 20,000-350,000 Raw Gates, Channelless Array Architecture
- Sea-of-Gates Architecture and Four Layer Metal for High Density
- Array Performance
  - Typical gate delay: 97 ps @ 0.19 mW *(unbuffered 2-in NOR, F.O. = 1, 0.17 mm wire)*
  - Typical gate delay: 95 ps @ 0.59 mW *(buffered 2-in NOR, F.O. = 3, 0.51 mm wire)*
- ECL, PECL, and TTL Signal Levels
- MIL-STD-883 Screening Available
- 0.6µ H-GaAs III MESFET Process
- Optional Fixed Clock Distribution Scheme to Minimize Clock Skew
- Multiple Buffering Options for Optimal Speed-Power Solution
- Commercial, Industrial and Military Temperature Ranges

Introduction

The FX family offers the integration level of BiCMOS gate arrays with speed performance exceeding that of ECL devices. Implemented using Vitesse's proprietary H-GaAs III process, the FX family of gate arrays is the first to combine ultra high integration with leading edge performance.

The H-GaAs III process represents the third generation of the H-GaAs technology developed by Vitesse to manufacture high yielding, LSI and VLSI digital GaAs circuits. This process features a 0.6 µm self-aligned gate MESFET and four levels of metal interconnect. The basic logic structure for the FX family is a 2-input NOR gate implemented using direct coupled FET logic (DCFL). Millions of hours of life testing have proven the reliability of the H-GaAs process technology and the DCFL logic structure.

The FX array family incorporates a channelless array architecture which allows metal routing on the first layer to be placed directly over unused cells. This approach avoids the need for pre-defined channels between columns of macros and therefore allows much greater density and flexibility than channelled gate array architectures. Due to an advanced four layer metal process, typical maximum array utilizations can be as high as 67% of the total available gates.

Capable of operating at over 1 GHz, the FX family arrays have been designed to provide the best speed - power performance of any gate array technology. The speed of leading edge ECL technology is achieved at a fraction of ECL's power. In addition, because of the frequency independent power consumption of H-GaAs technology, power dissipation levels comparable to, or lower than, similar density BiCMOS arrays can be achieved at frequencies above 50 MHz (see Vitesse Application Note 10, "Power Dissipation: BiCMOS vs. GaAs"). This power savings can add up to substantial cost savings to users in terms of overall cooling requirements.

The FX family includes support for the creation of custom masterslices. Functions such as SRAMs, multiport register files, and others can be merged with FX arrays resulting in unique architectures and optimum performance.

As with all of Vitesse's ASIC products, the FX arrays interface with TTL and ECL devices directly. The FX array family uses standard power supplies and is supported on the ASIC industry's most popular CAE platforms for schematic capture, behavioral modeling and logic synthesis.

741 Calle Plano, Camarillo, CA 93012 • 805/388-3700 • FAX: 805/987-5896

Applications

The FX Family of gate arrays can be used in a wide variety of applications including: mainframe computers, workstations and communications equipment. This family of high performance semi-custom products is ideally suited for systems requiring very high speed, low power digital logic at high levels of integration.

Computers

The ultra high integration offered by the FX arrays, combined with their high performance and low power consumption, makes them ideally suited for the implementation of high performance processors and processor support logic. Offering a big performance increase over BiCMOS technology and substantially lower power than ECL technology, the FX Family gate arrays are the perfect choice for systems with clock rates in excess of 50 MHz. Specific computer applications for FX arrays include integer arithmetic processing, floating-point processing, cache control, and bus interface functions.

Communications

Intelligent fiber optic communication links for voice and data transmission can be designed with the FX family. These applications can greatly benefit from the low power dissipation inherent in the FX arrays while allowing the user to implement the high speed VLSI and LSI circuits necessary to handle the new generation of high-bandwidth telecommunications standards. The implementation of large switching networks on a single chip is just one example of these applications.

Table 1: FX Array Specific Features

Array Name	*# of Internal Gates*			*# of Input Cells*	*# of I/O Cells*	*Max TTL Outputs/ Bidirects (B Option)*	*Total Signal Pins*	*Package Options*
	Total Raw Gates	*Usable Gates*	*D Flip-Flops*					
VGFX20K	20K	10K	1K	14	23	0	37	52 LDCC
				40	51	26	91	132 PGA 132 LDCC
VGFX40K	42K	21K	2.1K	43	96	96	139	195 PGA
VGFX100K	100K	50K	5K	74	99	48	173	211 PGA
				92	99	48	191	256 LDCC 264 TBGA
VGFX150K	150K	72K	7.2K	100	155	148	255	344 LDCC
VGFX200K	220K	110K	11K	83	172	172	255	415 PPGA
VGFX350K	350K	175K	17.5K	107	218	218	325	557 PPGA 578 TBGA

741 Calle Plano, Camarillo, CA 93012 • 805/388-3700 • FAX: 805/987-5896

Architecture

The FX arrays contain three cell types: internal logic cells, input only cells, and input/output (I/O) cells. All input only and input/output cells contain undedicated logic which is used to incorporate logic functions in the I/O macrocells. There is enough configurable logic in these cells to implement moderately complex functions such as multiplexers and flip flops, allowing the arrays to conform to the JTAG boundary scan standard.

FX arrays can be designed to implement full custom megacells such as SRAM and pre-defined core based megacells such as register files. In addition, a proprietary compiler is available to customers wishing to incorporate custom RAM configurations in their designs. A depiction of a VGFX350K with megacells incorporated is shown on page 1. The table below is a summary of the internal cells, I/O and package options for arrays in the FX family.

Clock Distribution

A generic high-drive clock buffer and distribution scheme has been developed for each member of the FX family. This pre-defined clock tree minimizes clock skew to registered functions within the array. The clock tree is capable of driving between 820 and 11,000 flip-flops depending on the size of the array being implemented. Clock skew of 50 ps is achievable.

Internal Logic Cells

The internal logic cells comprise most of the area of the array. These cells use direct coupled FET logic (DCFL), which minimizes the number of elements needed for each logic function. The primitive element or building block is a cell which consists of a single depletion-mode transistor and two enhancement-mode transistors which can be connected to make a 2-input NOR gate.

Input Only Cells

Input only cells are located predominantly on two edges of the periphery of the array. Input cells are also located in Input/Output cells. I/O macrocells can incorporate logic functions by utilizing the 24 logic cells contained in the input cell. Input cells are compatible with TTL and ECL signals. Both signal levels can be used in one chip design to optimize overall system performance. Input cells can provide 1x or 2x drive on either the true or complement signal. The input cells translate off-chip logic levels to internal GaAs logic levels for efficient internal operation. These cells also provide ESD input protection.

Each input only cell has resources to form a JTAG-compatible boundary scan flip-flop. This feature allows a user to implement boundary scan without using core cells.

Input/Output (I/O) Cells

Input/Output cells are located on two edges of the periphery of the array. I/O cells can be configured as output drivers, input receivers, or bidirectional transceivers. TTL and ECL signal levels are supported on the same chip. I/O macrocells can incorporate logic functions by utilizing the 48 logic cells contained in the input/output cell. Boundary scan can be easily accommodated since each I/O cell can be configured as a scan flip-flop. When configured as an ECL driver, the output cell can interface with ECL 10KH or 100K receivers while driving a 50Ω load. Two output cells may be paralleled to drive a double-terminated ECL bus (25Ω DC load).

741 Calle Plano, Camarillo, CA 93012 • 805/388-3700 • FAX: 805/987-5896

Power Supplies

The FX family uses industry standard power supplies. For an FX array requiring only ECL levels, -2V ± 5% is the only power supply required. For FX arrays requiring only TTL levels, 5V ± 5% and 2V ± 5% power supplies must be used. If both ECL and TTL levels are required, -2V ± 5% and 3.3V ± 5% are the specified power supplies.

Macrocell Library

The FX Macrocell Library contains information to fully evaluate the function and performance of logic blocks (macrocells). The library includes functional equivalents for all FURY™ Family macrocells as well as optimized megacell functions. The table on page 1- 5 is a representative list of the macrocells which are available for the FX arrays. Performance characteristics for selected macrocells begin on page 1-10. For a complete set of specifications, refer to the FX/Viper Macrocell Library, a separately bound document available from Vitesse.

Table 2: Input/Output Buffers

Name	*Description*
BIE	ECL Bi-directional Buffer (1X Drive)
BIE25NR2	ECL Bi-directional 25W Buffer w/2-Input NOR (1X Drive)
BIE25NR2S	ECL Input Buffer & Bi-directional 25 W Buffer w/2-Input NOR (1X Drive)
BIE25NR2T	ECL Input Buffer & Bi-directional 25 W Buffer w/2-Input NOR (2X Drive)
BIE25NR3	ECL Bi-directional 25W Buffer w/3-Input NOR (1X Drive)
BIENR2	ECL Bi-directional Buffer w/2-Input NOR (1X Drive)
BIENR2S	ECL Bi-directional Buffer w/2-Input NOR (1X Drive)
BIENR2T	ECL Bi-directional Buffer w/2-Input NOR (2X Drive)
BIT	TTL Bi-directional Buffer (-2.V/+3.3 V) (1X Drive)
BITK	TTL Bi-directional Buffer (+2 V/+5 V) (1X Drive)
BIT2K	TTL Bi-directional Buffer (+2 V/+5 V) (1X Drive)
BITOC	TTL Bi-directional Buffer w/Open Collector Output (-2 V/+3.3 V) (1X Drive)
BITOCK	TTL Bi-directional Buffer w/Open Collector Output (+2 V/+5 V) (1X Drive)
IE1F	ECL Inverting Input Buffer (1X Drive)
IE1T	ECL Input Buffer (1X Drive)
IE2T	ECL Input Buffer (2X Drive)
IECK3	ECL Input Buffer w/Dual Outputs (3X Drive)
IEDIFF	ECL Differential Input Buffer (1X Drive)
IEDIF2	ECL Differential Input Buffer (2X Drive)
IEDIF3	ECL Differential Input Buffer w/Dual Outputs (3X Drive)
IEINV2T	ECL Input Buffer w/Conditional Inversion (2X Drive)
IETOM6	ECL Input Buffer w/ 6:1 Test Output
IT1T	TTL Input Buffer (1X Drive) (-2 V/+3.3 V)
IT1TK	TTL Input Buffer (1X Drive) (+2 V/+5 V)
OE	ECL Output Buffer

741 Calle Plano, Camarillo, CA 93012 • 805/388-3700 • FAX: 805/987-5896

Table 2: Input/Output Buffers

Name	*Description*
OE25	ECL 25W Output Buffer
OENOR3	ECL Output Buffer w/3-Input NOR
OEPNC	ECL Output Buffer w/PNC Test Mode
OESD	ECL Differential Output Buffer
OT	TTL Output Buffer (-2 V/+3.3 V)
OTPNC	TTL Output Buffer w/PNC Test Mode
OTK	TTL Output Buffer (+2 V/+5 V)
OTKPNC	TTL Output Buffer w/PNC Test Mode
OT2K	TTL Output Buffer (+2 V/+5 V)

Table 3: Input/Output Registers

Name	*Description*
BIEJ	ECL Bi-directional Buffer w/JTAG Register (1X Drive)
BIER	ECL Bi-directional Buffer w/Scan Register & Register Enable (1X Drive)
IEJ1T	ECL Input Buffer w/JTAG Register (1X Drive)
IELBS1T	ECL Input Buffer w/Scan Register & Bypass (1X Drive)
IEMDF	ECL Input Buffer w/Scan Register (1X Drive)
IER1T	ECL Input Buffer w/Scan Register & Register Enable (1X Drive)
IERINV1T	ECL Input Buffer w/Scan Register & Conditional Inversion (1X Drive)
OEDRR4	ECL Output Buffer w/Double Ranked Register
OEJ	ECL Output Buffer w/JTAG Register
OEMDF	ECL Output Buffer w/Scan Register
OER	ECL Output Buffer w/Scan Register & Register Enable
IETO	ECL Input Buffer w/RAM Test Output (1X Drive)
OETI	ECL Output Buffer w/RAM Test Mode

Table 4: Buffers/Inverters

Name	*Description*
CLK0	Clock Buffer (1.5X Drive)
CLK1	Clock Buffer (3X Drive)
LB3S	Inverter (1X Drive)
LDLY1	Delay Buffer (0.5X Drive)
LDLY2	Delay Buffer (0.5X Drive)
LDR1	Inverting Buffer/Line Driver (1X Drive)
LDR2	Inverting Buffer/Line Driver (2X Drive)
LDR3	Inverting Buffer/Line Driver (3X Drive)
LAND	2-Input AND Gate (1X Drive)

741 Calle Plano, Camarillo, CA 93012 • 805/388-3700 • FAX: 805/987-5896

Table 4: Buffers/Inverters

Name	*Description*
LANDU	2-Input AND Gate (0.5X Drive)
LAND3U	3-Input AND Gate (0.5X Drive)
LAND4	4-Input AND Gate (1X Drive)
LANDI31U	3-Input AND Gate w/Single Inverting Input (0.5X Drive)
LANDI41U	4-Input AND Gate w/Single Inverting Input (0.5X Drive)
LN2	2-Input NOR Gate (1X Drive)
LN2B	2-Input NOR Gate (2X Drive)
LN2US	2-Input NOR Gate (0.5X Drive)
LN3	3-Input NOR Gate (1X Drive)
LN3U	3-Input NOR Gate (0.5X Drive)
LN4	4-Input NOR Gate (1X Drive)
LN4B	4-Input NOR Gate (2X Drive)
LN4U	4-Input NOR Gate (0.5X Drive)
LN6	6-Input NOR Gate (1X Drive)
LN6U	6-Input NOR Gate (0.5X Drive)
LN9	9-Input NOR Gate (1X Drive)
LN9B	9-Input NOR Gate (2X Drive)
LN9U	9-Input NOR Gate (0.5X Drive)
LNA2	2-Input NAND Gate (1X Drive)
LNA2U	2-Input NAND Gate (0.5X Drive)
LNA2Z	Low Speed 2-Input NAND Gate (0.5X Drive)
LNA4	4-Input NAND Gate (1X Drive)
LNA4U	4-Input NAND Gate (0.5X Drive)
LNI21	2-Input NOR Gate w/Single Inverting Input (1X Drive)
LNI21U	2-Input NOR Gate w/Single Inverting Input (0.5X Drive)
LNI31	3-Input NOR Gate w/Single Inverting Input (1X Drive)
LNI31U	3-Input NOR Gate w/Single Inverting Input (0.5X Drive)
LNI42U	4-Input NOR Gate w/Dual Inverting Inputs (0.5X Drive)
LO2	2-Input OR Gate (1X Drive)
LO2B	2-Input OR Gate (2X Drive)
LO2U	2-Input OR Gate (0.5X Drive)
LO32B	3-Input OR Gate w/Dual Outputs (2X Drive)
LO34	3-Input OR Gate w/Quad Outputs (1X Drive)
LO3C	3-Input OR Gate (3X Drive)
LO4	4-Input OR Gate (1X Drive)
LO4B	4-Input OR Gate (2X Drive)
LO4U	4-Input OR Gate (0.5X Drive)
LOI21	2-Input OR Gate w/Single Inverting Input (1X Drive)

741 Calle Plano, Camarillo, CA 93012 • 805/388-3700 • FAX: 805/987-5896

Table 4: Buffers/Inverters

Name	*Description*
LOI21U	2-Input OR Gate w/Single Inverting Input (0.5X Drive)
LOI31	3-Input OR Gate w/Single Inverting Input (1X Drive)
LOI31U	3-Input OR Gate w/Single Inverting Input (0.5X Drive)
LOI42	4-Input OR Gate w/Dual Inverting Inputs (1X Drive)
LOI42U	4-Input OR Gate w/Dual Inverting Inputs
LX1	2-Input Exclusive OR Gate (1X Drive)
LX1U	2-Input Exclusive OR Gate (0.5X Drive)
LX2	2-Input Exclusive NOR Gate (1X Drive)
LX2U	2-Input Exclusive NOR Gate (0.5X Drive)
LX3	3-Input Exclusive OR Gate (1X Drive)
LX4	4-Input Exclusive OR Gate (1X Drive)

Table 5: Complex Gates

Name	*Description*
OA21	2-1 Input OR-AND Complex Gate (1X Drive)
OA21U	2-1 Input OR-AND Complex Gate (0.5X Drive)
OA22	22-InputOR-ANDComplexGate(1XDrive)
OA22B	2 2-Input OR-AND Complex Gate (2X Drive)
OA22U	2 2-Input OR-AND Complex Gate (0.5X Drive)
OA222	3 2-Input OR-AND Complex Gate (1X Drive)
OA222B	3 2-Input OR-AND Complex Gate (2X Drive)
OA222U	3 2-Input OR-AND Complex Gate (0.5X Drive)
OA2222	4 2-Input OR-AND Complex Gate (1X Drive)
OA2222B	4 2-Input OR-AND Complex Gate (2X Drive)
OA2222U	4 2-Input OR-AND Complex Gate (0.5X Drive)
OA2X6	6 2-Input OR-AND Complex Gate (1X Drive)
OA2X6U	6 2-Input OR-AND Complex Gate (0.5X Drive)
OA2X9	9 2-Input OR-AND Complex Gate(1X Drive)
OA2X9U	9 2-Input OR-AND Complex Gate (0.5X Drive)
OA2X12	12 2-Input OR-AND Complex Gate (1X Drive)
OA41	4-1 Input OR-AND Complex Gate (1X Drive)
OA41U	4-1 Input OR-AND Complex Gate (0.5X Drive)
OA4321	4-3-2-1 Input OR-AND Complex Gate (1X Drive)
OA4321U	4-3-2-1 Input OR-AND Complex Gate (0.5X Drive)
OA44	2 4-Input OR-AND Complex Gate (1X Drive)
OA44U	2 4-Input OR-AND Complex Gate (0.5X Drive)
OA4444	4 4-Input OR-AND Complex Gate (1X Drive)

741 Calle Plano, Camarillo, CA 93012 • 805/388-3700 • FAX: 805/987-5896

Table 5: Complex Gates

Name	*Description*
OA4444U	4 4-Input OR-AND Complex Gate (0.5X Drive)
OAI221U	2-1 Input OR-AND Complex Gate w/Inverting AND Input
OAI231U	2-1-1 Input OR-AND Complex Gate w/Single Inverting AND Input
ON22	2 2-Input OR-NAND Complex Gate (1X Drive)
ON22B	2 2-Input OR-NAND Complex Gate (2X Drive)
ON222	3 2-Input OR-NAND Complex Gate (1X Drive)
ON222B	3 2-Input OR-NAND Complex Gate (2X Drive)
ON2222	4 2-Input OR-NAND Complex Gate (1X Drive)
ON2222B	4 2-Input OR-NAND Complex Gate (2X Drive)
ON2X9	9 2-Input OR-NAND Complex Gate (1X Drive)
ON2X9U	9 2-Input OR-NAND Complex Gate (0.5X Drive)

Table 6: Encoders/Decoders

Name	*Description*
LDE4	2-4 Decoder

Table 7: Multiplexers

Name	*Description*
LM1	2:1 Multiplexer (1X Drive)
LM1B	2:1 Multiplexer (2X Drive)
LM1U	2:1 Multiplexer (0.5X Drive)
LM3	4:1 Multiplexer (1X Drive)
LM3B	4:1 Multiplexer (2X Drive)
LM3U	4:1 Multiplexer (0.5X Drive)
LM3X2U	Dual 4:1 Multiplexer (0.5X Drive)
LM7	8:1 Multiplexer (1X Drive)

741 Calle Plano, Camarillo, CA 93012 • 805/388-3700 • FAX: 805/987-5896

Table 8: Latches

Name	*Description*
LLN1	Negative Transparent D Latch (1X Drive)
LLP1	Positive Transparent D Latch (1X Drive)
LLP1U	Positive Transparent D Latch (0.5X Drive)
LLP2	Positive Transparent D Latch w/2-Input OR (1X Drive)
LLP3	Positive Transparent D Latch w/2:1 Mux (1X Drive)
LLP4U	Positive Transparent D Latch w/Q & QN Outputs (0.5X Drive)

Table 9: Flip-Flops

Name	*Description*
LFP1	Positive Edge D Flip-Flop (1X Drive)
LFP1B	Positive Edge D Flip-Flop (2X Drive)
LFP1U	Positive Edge D Flip-Flop (0.5X Drive)
LFP2	Low Power Positive Edge D Flip-Flop (1X Drive)
LFP2U	Low Power Positive Edge D Flip-Flop (0.5X Drive)
LFP3	Positive Edge D Flip-Flop w/Set & Reset (1X Drive)
LFP3U	Positive Edge D Flip-Flop w/Set & Reset (0.5X Drive)
LFP4	Positive Edge D Flip-Flop w/Set (1X Drive)
LFP5	Positive Edge D Flip-Flop w/4-Input OR (1X Drive)
LFP6U	Positive Edge D Flip-Flop w/Q, QN Outputs & Set, Reset (0.5X Drive)
LJK1U	Positive Edge JK Flip-Flop (0.5X Drive)
LJK3U	Positive Edge JK Flip-Flop w/Set & Reset (0.5X Drive)
LTF3U	T Flip-Flop w/Set & Reset (0.5X Drive)

Table 10: Registers

Name	*Description*
LDRR4	Double Ranked Register (1X Drive)
LDRR4U	Double Ranked Register (1X Drive)
LJP1	JTAG Register (1X Drive)
LSP1	Scan Register (1X Drive)
LSP1U	Scan Register (0.5X Drive)
LSP1Z	Low Speed Scan Register (0.5X Drive)
LSP1R	Scan Register w/Reset (1X Drive)
LSP2	Scan Register w/Enable (1X Drive)
LSP2U	Scan Register w/Enable (0.5X Drive)
LSP3	Scan Register w/Enable (1X Drive)
LSP3B	Scan Register w/Enable (2X Drive)

741 Calle Plano, Camarillo, CA 93012 • 805/388-3700 • FAX: 805/987-5896

Table 10: Registers

Name	*Description*
LSP3U	Scan Register w/Enable (0.5X Drive)
LSP4	Scan Register w/Enable & Bus Inputs (1X Drive)
LSP4U	Scan Register w/Enable & Bus Inputs (0.5X Drive)

Table 11: Arithmetic Functions

Name	*Description*
CNT1	Positive Edge Triggered 1-Bit Counter (1.5X Drive)
LA1	Half-Adder (1X Drive)
LA1U	Half-Adder (0.5X Drive)
LA2	Full-Adder (1X Drive)
LA2B	Full-Adder (2X Drive)
LA2U	Full-Adder (0.5X Drive)
LADD4	4-Bit Adder (1X Drive)
LCAR4	4-Bit Carry-Lookahead Generator w/Inverted Outputs (1X Drive)
LCL1	4-Bit Carry-Lookahead Generator w/block Outputs (1X Drive)
LCL2	4-Bit Carry-Lookahead Generator w/Carry Outputs (1X Drive)
LCL3	4-Bit Carry-Lookahead Generator w/3 Carry Outputs (1X Drive)
LCS1	1-Bit Carry Select Adder (1X Drive)
LCSA1	3-2 Carry Save Adder (1X Drive)
XN2222	4-Bit Comparator w/Inverted Output (1X Drive)

Table 12: Fixed Clock Tree Drivers

Name	*Description*
CLK20K	ECL Differential Input Fixed Clock Tree for 20K Array
CLK20KT	TTL Input Fixed Clock Tree for 20K Array
CLK40K	ECL Differential Input Fixed Clock Tree for 40K Array
CLK40KT	TTL Input Fixed Clock Tree for 40K Array
CLK100K	ECL Differential Input Fixed Clock Tree for 100K Array
CLK100KT	TTL Input Fixed Clock Tree for 100K Array
CLK200K	ECL Differential Input Fixed Clock Tree for 200K Array
CLK200KT	TTL Input Fixed Clock Tree for 200K Array
CLK350K	ECL Differential Input Fixed Clock Tree for 350K Array
CLK350KT	TTL Input Fixed Clock Tree for 350K Array

741 Calle Plano, Camarillo, CA 93012 • 805/388-3700 • FAX: 805/987-5896

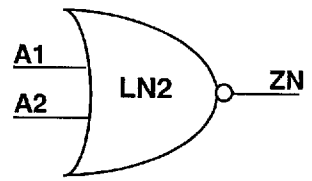
Table 13: Miscellaneous

Name	*Description*
LOAD	Load Macro
PD	Pull-Down to VTT (-2 V/0 V, -2 V/+3.3 V) or VCC (+2 V/+5 V)

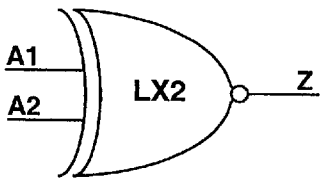
741 Calle Plano, Camarillo, CA 93012 • 805/388-3700 • FAX: 805/987-5896

Selected Macrocell AC Performance *(Commercial Arrays)*

(V_{TT} = -2.0V, V_{CC} = V_{CCA} = GND, T_C = 25°C, Load: F.O. = Ø; Ø mm wire.)

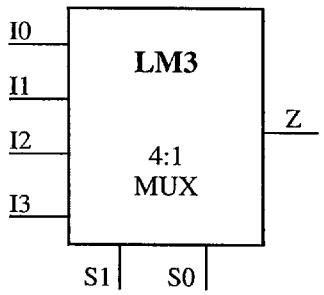


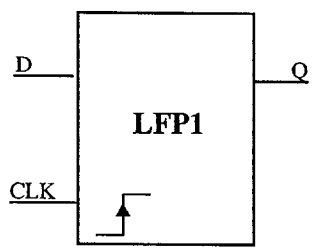
LN2: Buffered 2-input NOR	*Parameter*		*Min*	*Typ*	*Max*	*Units*
	Propagation Delay					
	A1, A2 to ZN	Rising Signal	24	—	81	ps
		Falling Signal	15	—	52	ps
	Load Dependent Delay					
	Delay/Fan-out	Rising Signal	3		9	ps
		Falling Signal	2		6	ps
	Delay / mm wire	Rising Signal	44	—	147	ps
		Falling Signal	24	—	84	ps
	Power Dissipation		-	0.58	0.87	mW



LN2: 2-input XNOR	*Parameter*		*Min*	*Typ*	*Max*	*Units*
	Propagation Delay					
	A1, A2 to ZN	Rising Signal	54	—	343	ps
		Falling Signal	69	—	322	ps
	Load Dependent Delay					
	Delay/Fan-out	Rising Signal	3	—	9	ps
		Falling Signal	2	—	7	ps
	Delay / mm wire	Rising Signal	44	—	147	ps
		Falling Signal	31	—	106	ps
	Power Dissipation		-	1.12	1.68	mW

741 Calle Plano, Camarillo, CA 93012 • 805/388-3700 • FAX: 805/987-5896

LM3: 4:1 Multiplexer	*Parameter*		*Min*	*Typ*	*Max*	*Units*
	Propagation Delay					
	S0, S1 to Z	Rising Signal	63	—	364	ps
		Falling Signal	81	—	354	ps
	I0-I3 to Z	Rising Signal	63	—	212	ps
		Falling Signal	81	—	281	ps
	Load Dependent Delay					
	Delay/Fan-out	Rising Signal	3	—	10	ps
		Falling Signal	2	—	7	ps
	Delay / mm wire	Rising Signal	50	—	167	ps
		Falling Signal	31	—	106	ps
	Power Dissipation		-	1.67	2.5	mW

LFP1: Positive Edge Triggered D Flop-flop	*Parameter*		*Min*	*Typ*	*Max*	*Units*
	Propagation Delay					
	CLK to Q	Rising Signal	54	—	182	ps
		Falling Signal	87	—	302	ps
	t_{SET-UP}		62	—	104	ps
	t_{HOLD}		43	—	73	ps
	Load Dependent Delay					
	Delay/Fan-out	Rising Signal	3	—	9	ps
		Falling Signal	2	—	7	ps
	Delay / mm wire	Rising Signal	44	—	147	ps
		Falling Signal	29	—	102	ps
	Power Dissipation		—	2.03	3.05	mW

741 Calle Plano, Camarillo, CA 93012 • 805/388-3700 • FAX: 805/987-5896

Absolute Maximum Ratings for ECL Only (-2V) and Mixed ECL/TTL (-2V, +3.3V) Power Supply Levels (1)

Power Supply Voltage (ECL), V_{TT} potential to GND ..... -2.2V to +0.5 V
Power Supply Voltage (TTL), V_{TTL} potential to GND ..... -0.5V to +4.3 V
ECL Input Voltage Applied, $(V_{IN\ ECL})^{(2)}$ ..... +0.5V to V_{TT}
TTL Input Voltage Applied, $(V_{IN\ TTL})^{(2)}$ ..... -0.5V to V_{TTL} + 1.0 V
ECL or TTL Output Current, I_{OUT} 50m
Case Temperature Under Bias, $(T_C)^{(3)}$ ..... -55 to +125°C
Storage Temperature, $(T_{STG})^{(3)}$ ..... -65C to +150°C

NOTES: (1) CAUTION: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.
(2) V_{TT}, V_{TTL} must be applied before any input signal voltage and V_{ECLIN} input must be greater than V_{TT} - 0.5V.
(3) Lower limit is ambient temperature and upper limit is case temperature.

Recommended Operating Conditions for ECL Only (-2V) and Mixed ECL/TTL (-2V, +3.3V) Power Supply Levels

ECL Supply Voltage, (V_{TT}) ..... -2.0V ± 5%
TTL Supply Voltage, (V_{TTL}) ..... +3.3V ± 5%
Commercial Operating Temperature Range, (T)(1). ..... 0 to 70°C
Industrial Operating Temperature Range, (T)(1) ..... -40 to 85°C
Military Operating Temperature Range, (T)(1). ..... -55 to 125°C
V_{CC} = V_{CCA} = GND, Output load 50Ω to -2.0V)

NOTES: (1) Lower limit is ambient temperature and upper limit is case temperature.

741 Calle Plano, Camarillo, CA 93012 • 805/388-3700 • FAX: 805/987-5896

DC Characteristics for -2V, +3.3V Power Supply Levels

Table 14: TTL Inputs/Outputs *(Over recommended commercial operating conditions, TTLGND = GND)*

Parameters	*Description*	*Min*	*Max*	*Units*	*Conditions*
V_{OH}	Output HIGH voltage	2.4	—	V	I_{OH} = -2.4 mA
V_{OL}	Output LOW voltage	0	0.4	V	I_{OL} = 16 mA
V_{IH}	Input HIGH voltage	2.0	V_{TTL} +1.0	V	Guaranteed HIGH for all inputs
V_{IL}	Input LOW voltage	0	0.8	V	Guaranteed LOW for all inputs
I_{IH}	Input HIGH current	—	50	µA	V_{IN} = 2.4V
I_{IL}	Input LOW current	-500	—	µA	V_{IN} = 0.4V
I_{OZH}	3-State Output OFF Current HIGH	—	200	µA	V_{OUT} = 2.4V
I_{OZL}	3-State Output OFF Current LOW	-100	—	µA	V_{OUT} = 0.4V
I_{OCZ}	Open collector output leakage current	—	200	µA	V_{OUT} = 2.4V

NOTES:
(1) Differential ECL output pins must be terminated identically

Table 15: ECL Inputs/Outputs *(Over recommended commercial operating conditions with internal V_{REF}*

Parameters	*Description*	*Min*	*Max*	*Units*	*Conditions*
V_{OH}	Output HIGH voltage	-1020	-700	mV	$V_{IN} = V_{IH}^{(max)}$
V_{OL}	Output LOW voltage	-2000	-1620	mV	or $V_{IL}^{(min)}$
V_{IH}	Input HIGH voltage	-1100	-700	mV	Guaranteed HIGH for all inputs
V_{IL}	Input LOW voltage	-2000	-1540	mV	Guaranteed LOW for all inputs
I_{IH}	Input HIGH current	—	200	µA	$V_{IN} = V_{IH}^{(max)}$
I_{IL}	Input LOW current	-50	—	µA	$V_{IN} = V_{IL}^{(min)}$

741 Calle Plano, Camarillo, CA 93012 • 805/388-3700 • FAX: 805/987-5896

Absolute Maximum Ratings for TTL ONLY (+2V, +5V) Power Supply Levels[1]

Power Supply Voltage, (V_{MM}) potential to GND ..... -0.5V to +2.5V
Power Supply Voltage (TTL), V_{TTL} potential to GND ..... -0.5V to +5.5V
TTL Input Voltage Applied, ($V_{IN\ TTL}$) ..... -0.5V to V_{TTL} + 1.0V
TTL Output Current, I_{OUT} (DC, output HI) 50mA
Case Temperature Under Bias, (T_C)[2] ..... -55C to +125°C
Storage Temperature, (T_{STG})[2] ..... -65C to +150°C

NOTES: (1) CAUTION: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.
(2) Lower limit is ambient temperature and upper limit is case temperature.

Recommended Operating Conditions for TTL ONLY (+2V, +5V) Power Supply Levels

Supply Voltage, (V_{MM}) ..... +2.0V ± 5%
TTL Supply Voltage, (V_{TTL}) ..... +5.0V ± 5%
Commercial Operating Temperature Range, (T)[1] ..... 0 to 70°C
Industrial Operating Temperature Range, (T)[1] ..... -40 to 85°C
Military Operating Temperature Range, (T)[1] ..... -55 to 125°C

NOTE: (1) Lower limit is ambient temperature and upper limit is case temperature.

741 Calle Plano, Camarillo, CA 93012 • 805/388-3700 • FAX: 805/987-5896

DC Characteristics for TTL only +2V, +5V Power Supply Levels

Table 16: TTL Inputs/Outputs *(Over recommended commercial operating conditions, TTLGND = GND)*

Parameters	*Description*	*Min*	*Max*	*Units*	*Conditions*
V_{OH}	Output HIGH voltage	2.4	—	V	I_{OH} = -2.4 mA
V_{OL}	Output LOW voltage	0	0.5	V	I_{OL} = 8 mA
V_{IH}	Input HIGH voltage	2.0	V_{TTL} +1.0	V	Guaranteed HIGH for all inputs
V_{IL}	Input LOW voltage	0	0.8	V	Guaranteed LOW for all inputs
I_{IH}	Input HIGH current	—	50	µA	V_{IN} = 2.4V
I_{IL}	Input LOW current	-500	—	µA	V_{IN} = 0.5V
I_{OZH}	3-State Output OFF Current HIGH	—	200	µA	V_{OUT} = 2.4V
I_{OZL}	3-State Output OFF Current LOW	-200	—	µA	V_{OUT} = 0.5V
I_{OCZ}	Open collector output leakage current	—	200	µA	V_{OUT} = 2.4V

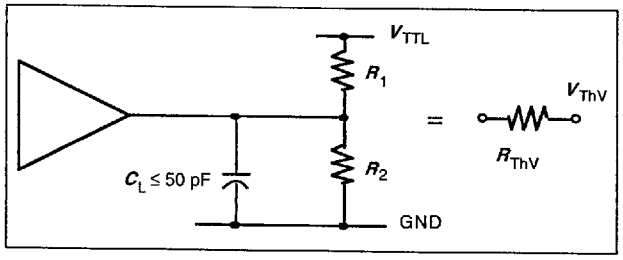
Table 17: PECL Inputs/Outputs (Over recommended commercial operating conditions full external V_{REF} = *V_{TTL} -1.32, Output load 50Ω to V_{TTL}-2.0V).*

Parameters	*Description*	*Min*	*Max*	*Units*	*Conditions*
V_{OH}	Output HIGH voltage	V_{TTL} -1020	V_{TTL} -700	mV	
V_{OL}	Output LOW voltage	V_{TTL} -2000	V_{TTL} -1620	mV	
V_{IH}	Input HIGH voltage	V_{TTL} -1100	V_{TTL} -700	mV	Guaranteed HIGH for all inputs
V_{IL}	Input LOW voltage	V_{TTL} -2000	V_{TTL} -1540	mV	Guaranteed LOW for all inputs
I_{IH}	Input HIGH current	—	200	µA	V_{IN} = V_{IH} (max)
I_{IL}	Input LOW current	-50	—	µA	V_{IN} = V_{IL} (min)

741 Calle Plano, Camarillo, CA 93012 • 805/388-3700 • FAX: 805/987-5896

Equivalent Circuits for Output Loads

TTL



ECL

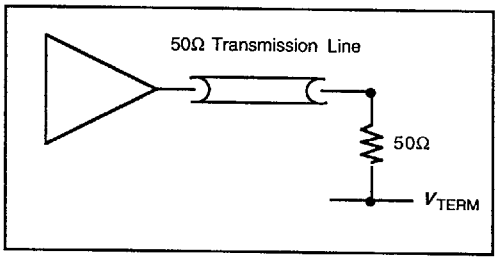
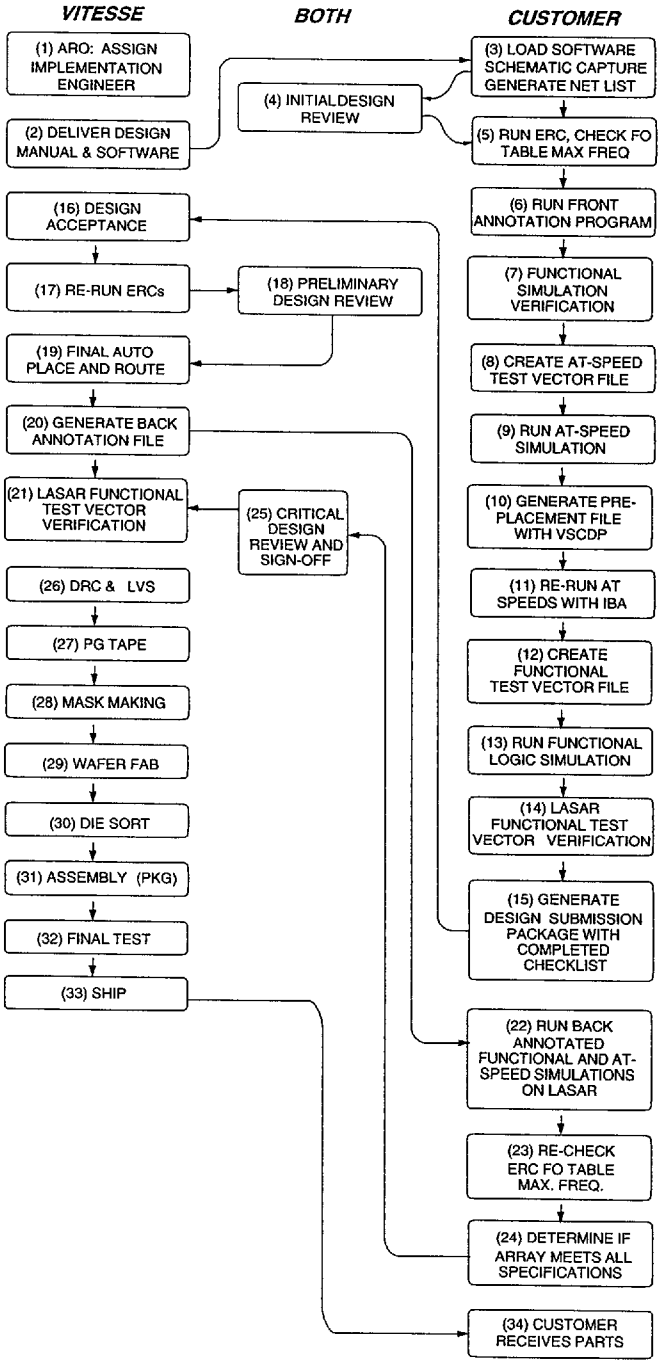


Table 18: Equivalent Circuits for Output Loads

Power Levels	R_1	R_2	R_{ThV}	V_{ThV}
+2, +5	467	301	183	1.96V
-2, +3.3	252	189	108	2.14V

741 Calle Plano, Camarillo, CA 93012 • 805/388-3700 • FAX: 805/987-5896

Figure 1: Gate Array Design Flow



741 Calle Plano, Camarillo, CA 93012 • 805/388-3700 • FAX: 805/987-5896

Option Development Procedure

Vitesse Semiconductor offers its customers the option of fully designing their own gate array, or having Vitesse perform a turn-key implementation of their design based on mutually agreed specifications. Regardless of the interface, a Vitesse implementation engineer is assigned to the customer to answer questions and track the progress of the design from start to finish. The following steps are normally performed by Vitesse design and implementation engineers:

- Masterslice design
- Custom megacell design
- Final placement and routing of the design
- Net-length extraction
- Fan-out and metal delay calculation
- Design rule checking and layout vs schematic

Through experience with many gate array designs, Vitesse has created a design automation framework and a well defined flow for smooth implementation of customer designs. The flowchart on the previous page summarizes the typical gate array project flow and the various tasks delegated to the customer or to Vitesse. For complete details on development options, refer to the FX/Viper Design Manual.

CAE/EDA Tools/Support

FX designs are currently supported on Mentor, Synopsys, Cadence, and Viewlogic platforms. Cadence includes support for Composer and Verilog-XL. LASAR simulation software is used to verify the functional and AC performance of the design by accounting for on-chip timing variations. Macrocell libraries for the MOTIVE™ timing verifier from Quad Design are also available. A Vitesse Design Kit includes documentation and software to allow a designer to perform schematic capture, functional simulation, front-annotated timing simulation, electrical rule checks, and back-annotated simulation after place and route. To facilitate floorplanning and block pre-placement, Vitesse has developed an interactive graphical pre-placement tool, supported in the X Windows™ environment, which the customer may use for their design. Cadence place and route tools are used for the actual physical implementation at Vitesse.

Training

Design classes are provided to help the customer understand the design methodology and tools utilized in the gate array design process. These classes are recommended for all customers planning to implement a design in a Vitesse gate array. Training can be provided at the Vitesse facility or at the customer's site.

Notice

Vitesse Semiconductor Corporation reserves the right to make changes in its' products specifications or other information at any time without prior notice. Therefore the reader is cautioned to confirm that this datasheet is current prior to placing any orders. The company assumes no responsibility for any circuitry described other than circuitry entirely embodied in a Vitesse product.

Warning

Vitesse Semiconductor Corporation's product are not intended for use in life support appliances, devices or systems. Use of a Vitesse product in such applications without the written consent of the appropriate Vitesse officer is prohibited.

741 Calle Plano, Camarillo, CA 93012 • 805/388-3700 • FAX: 805/987-5896