

BUK962R2-40C

N-channel TrenchMOS logic level FET

Rev. 02 — 17 April 2008

Product data sheet

1. Product profile

1.1 General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product has been designed and qualified to the appropriate AEC standard for use in automotive critical applications.

1.2 Features and benefits

- Low conduction losses due to low on-state resistance
- Suitable for logic level gate drive sources
- Q101 compliant
- Suitable for thermally demanding environments due to 175 °C rating

1.3 Applications

- 12 V loads
- General purpose power switching
- Automotive systems
- Motors, lamps and solenoids

1.4 Quick reference data

Table 1. Quick reference

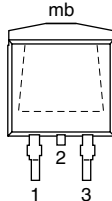
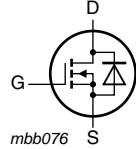
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}$	-	-	40	V
I_D	drain current	$V_{GS} = 5\text{ V}; T_j = 25\text{ °C};$ see Figure 1 and 4	[1][2]	-	100	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C};$ see Figure 2	-	-	333	W
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 100\text{ A}; V_{sup} \leq 40\text{ V};$ $R_{GS} = 50\ \Omega; V_{GS} = 5\text{ V};$ $T_{j(init)} = 25\text{ °C};$ unclamped	-	-	1.2	J
Dynamic characteristics						
Q_{GD}	gate-drain charge	$V_{GS} = 5\text{ V}; I_D = 25\text{ A};$ $V_{DS} = 32\text{ V};$ see Figure 14	-	73	-	nC
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 5\text{ V}; I_D = 25\text{ A};$ $T_j = 25\text{ °C};$ see Figure 12 , 11 and 13	-	2	2.2	m Ω

[1] Continuous current is limited by package.

[2] Refer to document 9397 750 12572 for further information.

2. Pinning information

Table 2. Pinning

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		
2	D	drain		
3	S	source		
mb	D	mounting base; connected to drain		

SOT404 (D2PAK)

3. Ordering information

Table 3. Ordering information

Type number	Package		Version
	Name	Description	
BUK962R2-40C	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404

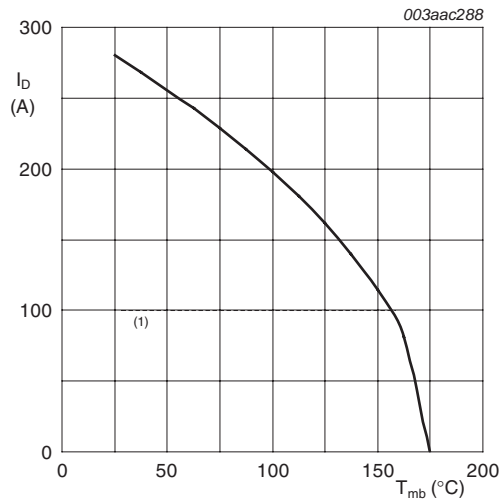
4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$	-	40	V
V_{DGR}	drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$	-	40	V
V_{GS}	gate-source voltage		-15	15	V
I_D	drain current	$T_{mb} = 25\text{ °C}$; $V_{GS} = 5\text{ V}$; see Figure 1	[1]	280	A
		$V_{GS} = 5\text{ V}$; $T_j = 100\text{ °C}$; see Figure 1	[2][3]	100	A
		$V_{GS} = 5\text{ V}$; $T_j = 25\text{ °C}$; see Figure 1 and 4	[2][3]	100	A
I_{DM}	peak drain current	$T_{mb} = 25\text{ °C}$; $t_p \leq 10\text{ }\mu\text{s}$; pulsed; see Figure 4	-	1130	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; see Figure 2	-	333	W
T_{stg}	storage temperature		-55	175	°C
T_j	junction temperature		-55	175	°C
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 100\text{ A}$; $V_{sup} \leq 40\text{ V}$; $R_{GS} = 50\text{ }\Omega$; $V_{GS} = 5\text{ V}$; $T_{j(init)} = 25\text{ °C}$; unclamped	-	1.2	J
$E_{DS(AL)R}$	repetitive drain-source avalanche energy	see Figure 3	[4][5] [6]	-	J
Source-drain diode					
I_S	source current	$T_{mb} = 25\text{ °C}$	[2][3]	100	A
I_{SM}	peak source current	$t_p \leq 10\text{ }\mu\text{s}$; pulsed; $T_{mb} = 25\text{ °C}$	-	1130	A

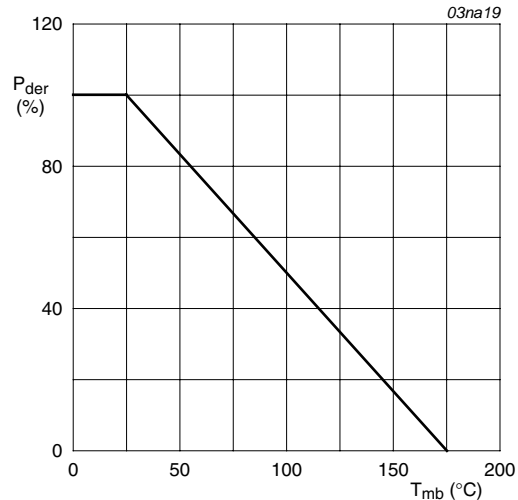
- [1] Current is limited by chip power dissipation rating.
- [2] Continuous current is limited by package.
- [3] Refer to document 9397 750 12572 for further information.
- [4] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.
- [5] Repetitive avalanche rating limited by an average junction temperature of 170 °C.
- [6] Refer to application note AN10273 for further information.



$V_{GS} \geq 5V$

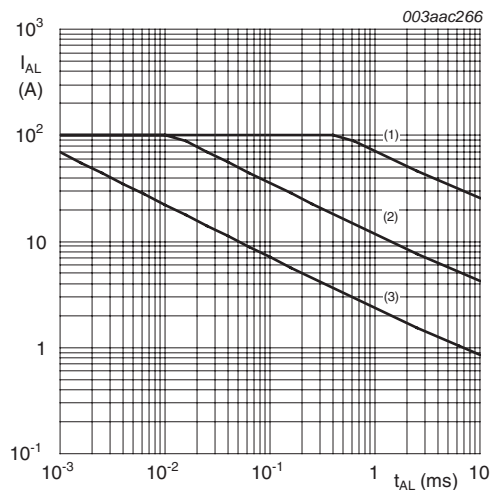
(1) Capped at 100 A due to package.

Fig 1. Continuous drain current as a function of mounting base temperature



$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized total power dissipation as a function of mounting base temperature



(1) Single-pulse; $T_j = 25^{\circ}C$.

(2) Single-pulse; $T_j = 150^{\circ}C$.

(3) Repetitive.

Fig 3. Single-pulse and repetitive avalanche rating; avalanche current as a function of avalanche time

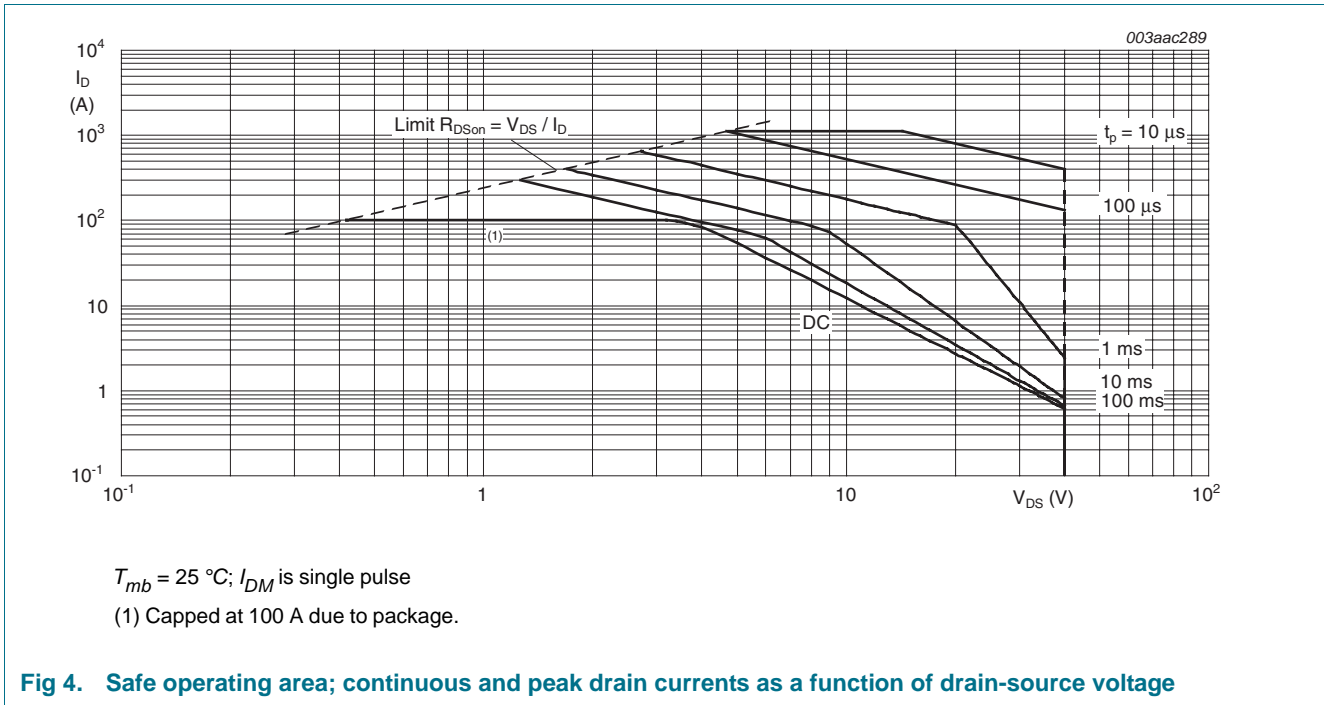
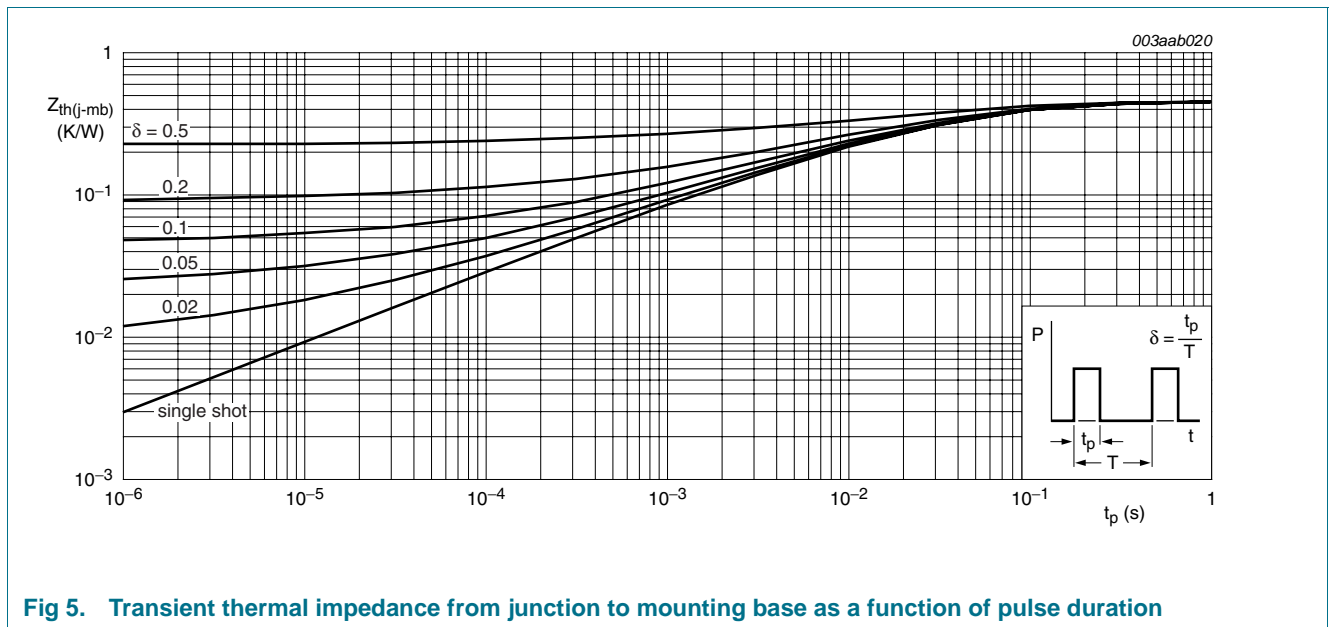


Fig 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	minimum footprint; mounted on a printed circuit	-	50	-	K/W
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 5	-	-	0.45	K/W



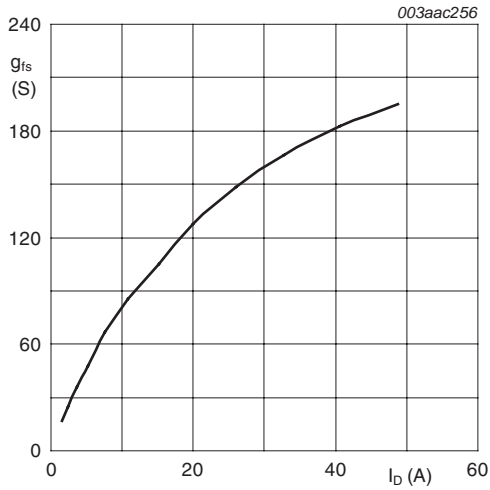
6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	40	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	36	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C;$ see Figure 9 and 10	1	1.5	2	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ C;$ see Figure 9	-	-	2.3	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ C;$ see Figure 9	0.5	-	-	V
I_{DSS}	drain leakage current	$V_{DS} = 40 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 \text{ }^\circ C$	-	-	500	μA
		$V_{DS} = 40 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	0.02	1	μA

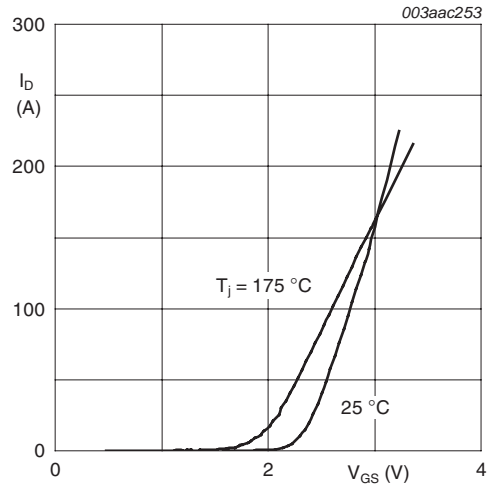
Table 6. Characteristics ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I _{GSS}	gate leakage current	V _{DS} = 0 V; V _{GS} = 15 V; T _j = 25 °C	-	2	100	nA
		V _{DS} = 0 V; V _{GS} = -15 V; T _j = 25 °C	-	2	100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = 4.5 V; I _D = 25 A; T _j = 25 °C	-	-	2.45	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _j = 25 °C	-	1.6	1.9	mΩ
		V _{GS} = 5 V; I _D = 25 A; T _j = 175 °C; see Figure 11	-	-	4.2	mΩ
		V _{GS} = 5 V; I _D = 25 A; T _j = 25 °C; see Figure 12 , 11 and 13	-	2	2.2	mΩ
Source-drain diode						
V _{SD}	source-drain voltage	I _S = 25 A; V _{GS} = 0 V; T _j = 25 °C; see Figure 16	-	0.85	1.2	V
t _{rr}	reverse recovery time	I _S = 25 A; dI _S /dt = 100 A/μs;	-	70	-	ns
Q _r	recovered charge	V _{GS} = 0 V; V _{DS} = 30 V	-	60	-	nC
Dynamic characteristics						
Q _{G(tot)}	total gate charge	I _D = 25 A; V _{DS} = 32 V; V _{GS} = 5 V; see Figure 14	-	120	-	nC
Q _{GS}	gate-source charge		-	30	-	nC
Q _{GD}	gate-drain charge		-	73	-	nC
C _{iss}	input capacitance	V _{GS} = 0 V; V _{DS} = 25 V;	-	12487	16700	pF
C _{oss}	output capacitance	f = 1 MHz; T _j = 25 °C; see Figure 15	-	1323	1600	pF
C _{rss}	reverse transfer capacitance		-	938	1290	pF
t _{d(on)}	turn-on delay time	V _{DS} = 30 V; R _L = 1.2 Ω;	-	130	-	ns
t _r	rise time	V _{GS} = 5 V; R _{G(ext)} = 10 Ω	-	310	-	ns
t _{d(off)}	turn-off delay time		-	380	-	ns
t _f	fall time		-	250	-	ns
L _D	internal drain inductance	from upper edge of drain mounting base to centre of die	-	2.5	-	nH
L _S	internal source inductance	from source lead to source bond pad	-	7.5	-	nH



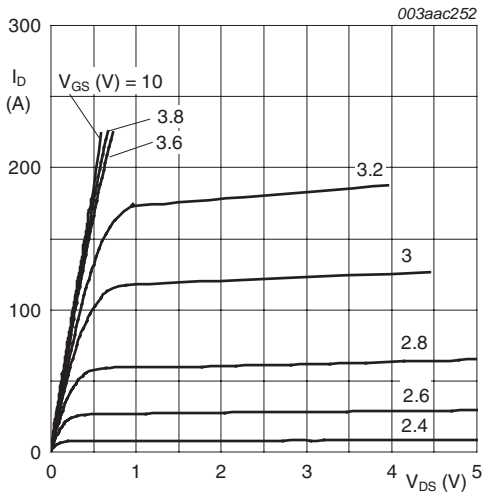
$T_j = 25\text{ }^\circ\text{C}; V_{DS} = 25\text{ V}$

Fig 6. Forward transconductance as a function of drain current; typical values



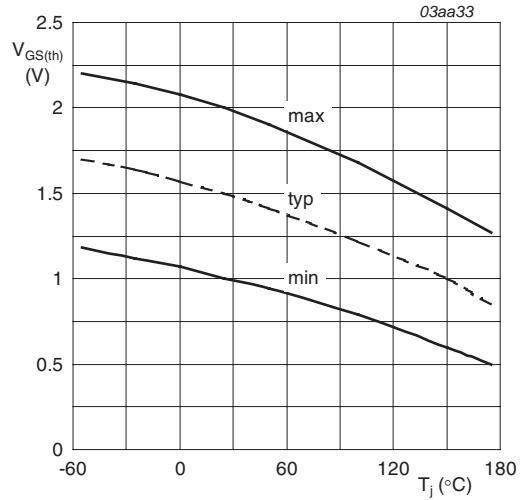
$V_{DS} = 25\text{ V}$

Fig 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values



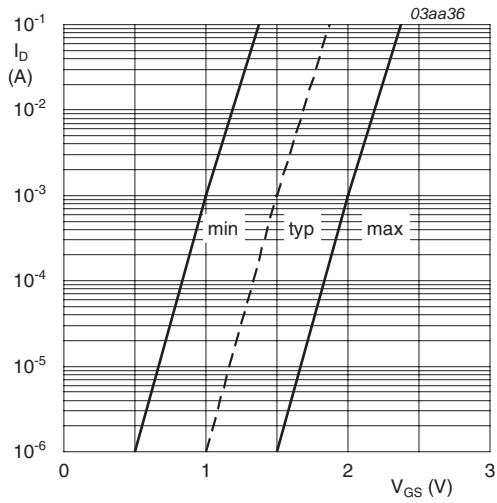
$T_j = 25\text{ }^\circ\text{C}$

Fig 8. Output characteristics: drain current as a function of drain-source voltage; typical values



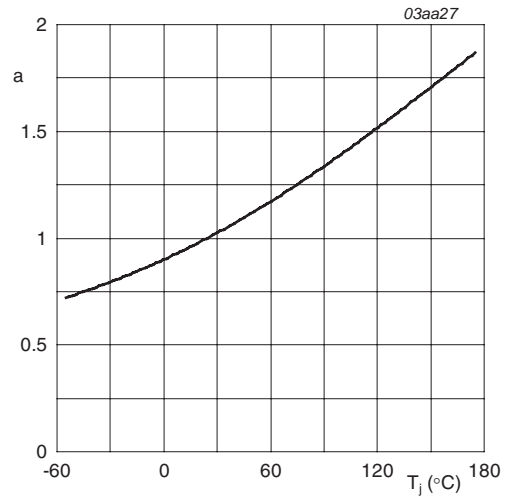
$I_D = 1\text{ mA}; V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature



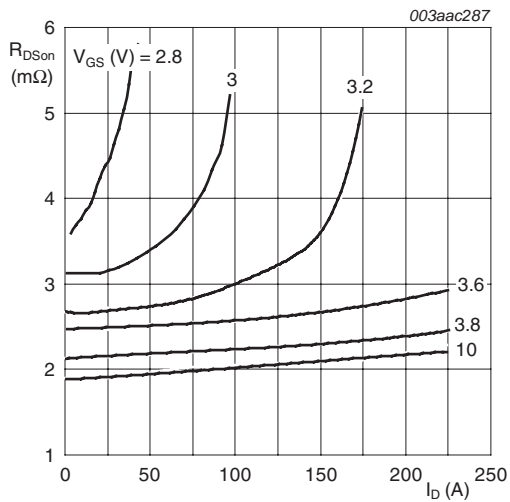
$T_j = 25\text{ }^\circ\text{C}; V_{DS} = V_{GS}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage



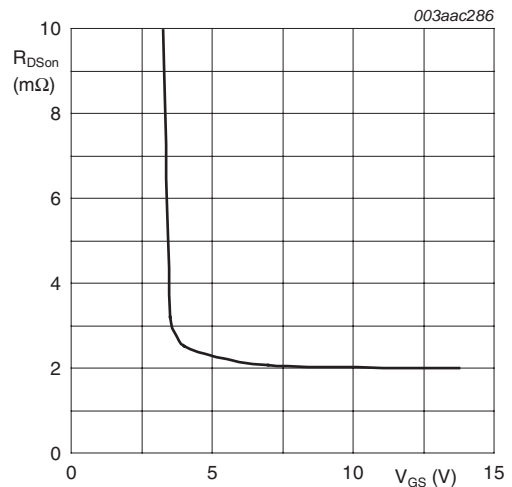
$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$

Fig 11. Normalized drain-source on-state resistance factor as a function of junction temperature



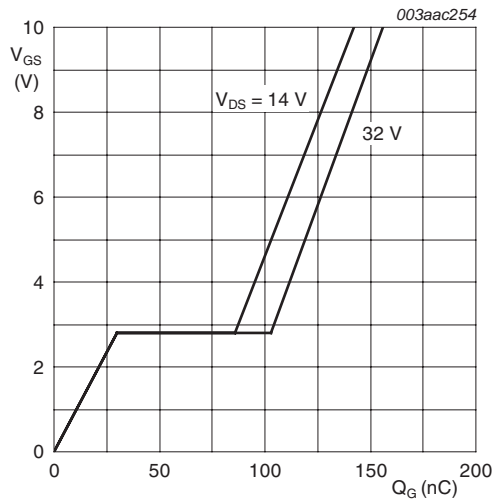
$T_j = 25\text{ }^\circ\text{C}$

Fig 12. Drain-source on-state resistance as a function of drain current; typical values



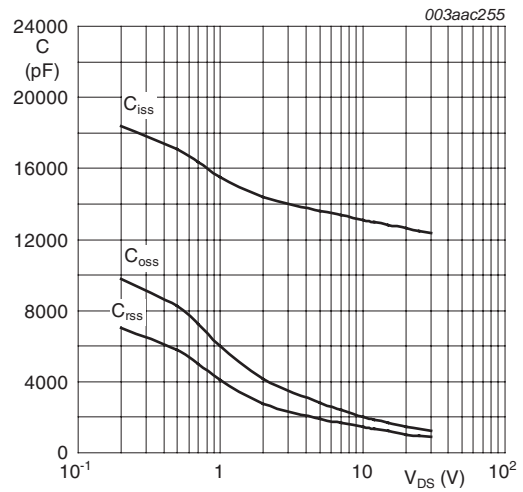
$T_j = 25\text{ }^\circ\text{C}; I_D = 25\text{ A}$

Fig 13. Drain-source on-state resistance as a function of gate-source voltage; typical values



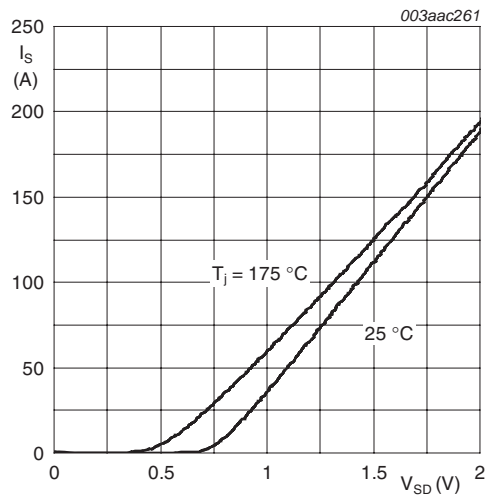
$T_j = 25\text{ }^\circ\text{C}; I_D = 25\text{ A}$

Fig 14. Gate-source voltage as a function of gate charge; typical values



$V_{GS} = 0\text{ V}; f = 1\text{ MHz}$

Fig 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$V_{GS} = 0\text{ V}$

Fig 16. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

7. Package outline

Plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)

SOT404

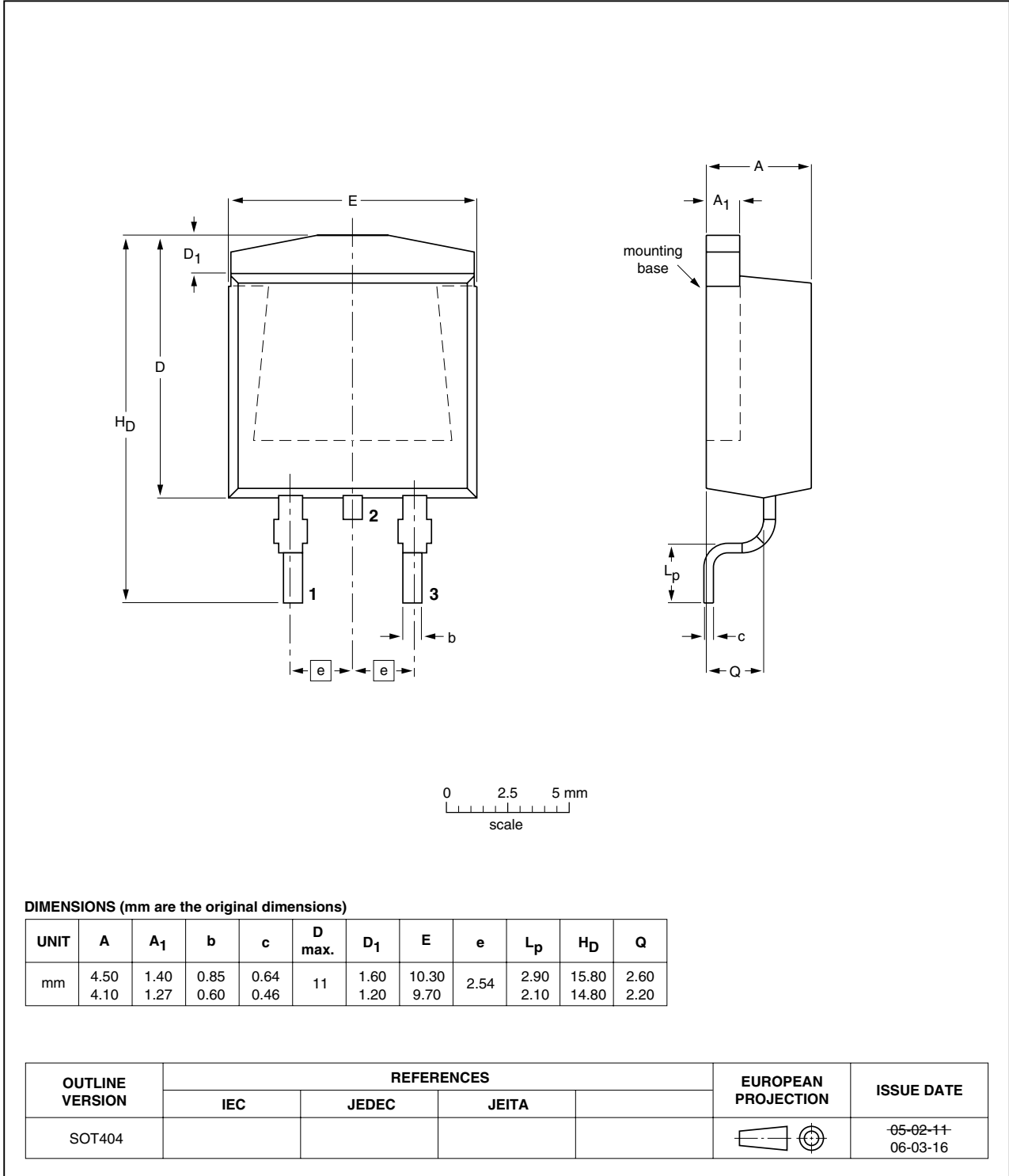


Fig 17. Package outline SOT404 (D2PAK)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BUK962R2-40C_2	20080417	Product data sheet	-	BUK962R2-40C_1
Modifications:	• Table 6 : V_{DS} condition for I_{DSS} corrected.			
BUK962R2-40C_1	20080328	product data sheet	-	-

9. Legal information

9.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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11. Contents

1 Product profile 1

1.1 General description 1

1.2 Features and benefits 1

1.3 Applications 1

1.4 Quick reference data 1

2 Pinning information 2

3 Ordering information 2

4 Limiting values 2

5 Thermal characteristics 5

6 Characteristics 5

7 Package outline 10

8 Revision history 11

9 Legal information 12

9.1 Data sheet status 12

9.2 Definitions 12

9.3 Disclaimers 12

9.4 Trademarks 12

10 Contact information 12

11 Contents 13

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