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FDC37C77

ADVANCE INFORMATION

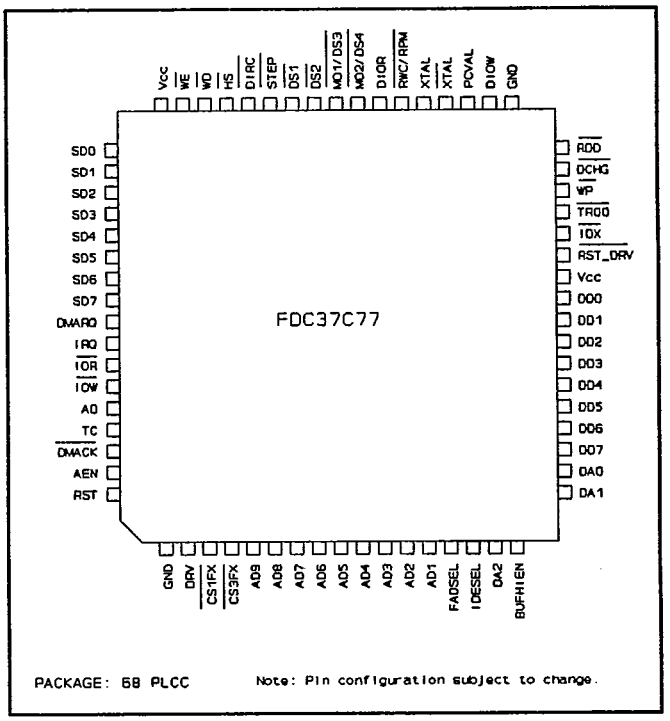
T-52-33-61

Enhanced Floppy Disk Subsystem Controller

FEATURES

- ☐ Provides complete "Paddle Card" function with the addition of just one 74LS245
- ☐ 1 Mbit/sec Data Rate
- ☐ Complete Floppy Disk Control System, Integrating:
  - Floppy Disk Formatter/Controller
  - IBM® PC/AT® Bus Interface
  - Address Decoder
  - Data Separator
  - Drive Interface
  - Write Precompensation Generator
  - Data Rate Selector
  - Clock Generator
  - 16 Byte FIFO
- ☐ Includes IDE Interface/Decoder
- ☐ Supports Vertical Recording Format
- ☐ IBM PC/AT Compatible Format (Single and Double Density)
  - Provides Required Signal Qualification to DMA Channel (in PC/AT Mode)
  - BIOS Compatible
  - Supports Dual Speed Spindle Drive
- ☐ Enhanced Host Interface:
  - Supports 12 MHz, 286 µP With 0 Wait States
  - Capable of Driving 20 LS TTL Loads
  - Schmitt Trigger Inputs (Except Data Bus)
- ☐ Direct Floppy Disk Drive Interface
  - 48 mA Drivers
  - Schmitt Trigger Inputs
- ☐ Multisector and Multitrack Transfer
- ☐ Internal Address Mark Detection Circuitry
- ☐ User Programmable Track Stepping Rate and Head Load/Unload Time
- ☐ Automatic Write Precompensation

PIN CONFIGURATION



PACKAGE: 68 PLCC Note: Pin configuration subject to change.

- ☐ Data Transfer in DMA or Non-DMA Mode
- ☐ Parallel Seek Operations
- ☐ On Chip Clock Generation Requires Just One 32 MHz Crystal for All Functions
- ☐ Controls up to Four Drives
- ☐ Internal Power-Up Reset Circuitry
- ☐ Standby Mode Reduces Power Consumption
- ☐ Low Power CMOS; Single +5 V Supply

GENERAL DESCRIPTION

The FDC37C77 combines a floppy disk formatter/controller, high performance data separator, write precompensation generator, data rate selector, clock generator, 16 byte FIFO, and IDE interface/decoder/driver in one 68 pin PLCC package. High current drivers and TTL compatible Schmitt trigger circuits on all inputs except the data bus allow direct host and drive connection.

The combination of a host interface which supports a 12 MHz PC/AT bus without the use of wait states, and a 16 byte FIFO ensure optimal system performance.

The internal IDE interface/decoder and AT bus address decoder eliminate the external address decoder circuitry previously required for both the floppy disk controller and ATA compatible drive. External components are further reduced by the high current drivers of the FDC37C77. All drive related outputs can sink 48 mA; all host related outputs can sink 12 mA. All host and drive related inputs except for the data bus and crystal have internal Schmitt triggers.

The FDC37C77 utilizes the SMC CMOS 765 core for guaranteed compatibility with existing software. The high performance digital data separator, which requires no external components, implements the proven FDC92C39 data separator algorithm for high bit jitter tolerance.

Toshiba format vertical (perpendicular) recording is supported as well as conventional longitudinal format recording.

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DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	DESCRIPTION
HOST PROCESSOR INTERFACE			
	Data 0-7	SD0-SD7	Input/Output. The data bus connection to the host microprocessor. These pins are used by the host to transmit data to and from the FDC37C77 and are in the high-impedance state when not being used.
	$\overline{\text{Read}}$	$\overline{\text{IOR}}$	Input. This active low signal is issued by the host microprocessor to indicate a read operation. A low pulse on this input when the FDC37C77 is selected enables data from the Buffer or Status Register onto the data bus for reading by the host.
	$\overline{\text{Write}}$	$\overline{\text{IOW}}$	Input. This active low signal is issued by the host microprocessor to indicate a write operation. A low pulse on this input when the FDC37C77 is selected enables data from the data bus to be written into the FDC37C77.
	Address Enable	AEN	Input. This active high signal allows DMA data transfers to occur. When AEN = "1", the DMA controller has control of the address bus, $\overline{\text{IOR}}$ and $\overline{\text{IOW}}$. When AEN = "0", addresses to the FDC37C77 are valid.
	Direct Memory Access Request	DMARQ	Output. This active high signal is a DMA request for byte transfers of data. This signal is cleared when the host responds with the $\overline{\text{DMACK}}$ signal going low. This signal is normally driven in the Base Mode. When the FDC37C77 is in the Special or PC/AT mode, this pin is three-stated and is enabled by the DMAEN from the Digital Output Register.
	$\overline{\text{DMA Acknowledge}}$	$\overline{\text{DMACK}}$	Input. A low level on this pin indicates a response by the host to a DMA request. It is used by the DMA controller to transfer data to or from the FDC37C77. In Special or PC/AT mode, this signal is qualified by DMAEN from the Digital Output Register.
	Terminal Count	TC	Input. This active high signal indicates to the FDC37C77 that data transfer is complete. In Base Mode, TC will be qualified by $\overline{\text{DMACK}}$ only in DMA operations. In non-DMA (Programmed I/O) operations, and the $\overline{\text{IOR}}$ and $\overline{\text{IOW}}$ signals are used as a gating function. In Special or PC/AT mode, TC will always be qualified by $\overline{\text{DMACK}}$ (whether in DMA or non-DMA operations), but will only be qualified by $\overline{\text{DMACK}}$ if DMAEN from the Digital Output Register is a logic "1". In PC/AT mode, non-DMA operations will occur successfully but will cause an abnormal termination error at the completion of a command.
	Drive Interrupt	IRQ	Output. This signal is an interrupt indicating the completion of command execution or data transfer requests (in non-DMA operations). This signal is normally driven in the Base mode. When the FDC37C77 is in the Special or PC/AT mode, this pin is three-stated and is enabled by the DMAEN signal for the Digital Output Register.
	Reset	RST	Input. This active high signal resets the FDC37C77. When RST occurs, the FDC37C77 defaults to Base Mode and the data rate is defaulted to 250K MFM. When RST is active, the high current driver outputs to the disk drive are disabled.
	Address 0-9	AD0-AD9	Inputs. These TTL level inputs are tied to the PC/AT bus address bits SA0-SA9 and generate the internal register addresses and register load enables. In addition, these bits are used to generate the Chip Select signals $\overline{\text{CS1FX}}$ and $\overline{\text{CS3FX}}$ for the IDE drive, and to gate the Disk Change status bit onto data bit D7 during a read of the Control Block Register (3F7H).
	Floppy Disk Address Select	FADSEL	Input. This TTL input with internal pull-up resistor is used to select the Primary or Secondary floppy disk controller AT addresses. When FADSEL = "1", the Primary Addresses are selected. When FADSEL = "0", the Secondary Addresses are selected.

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	DESCRIPTION
DRIVE INTERFACE			
	Read Disk Data	RDD	Input. Raw serial bit stream from the disk drive. Each falling edge represents a flux transition of the encoded data.
	Write Enable	WE	Output. This active low driver allows current to flow through the write head. It becomes active just prior to writing to the diskette.
	Write Data	WD	Output. This active low driver provides the encoded data to the disk drive. Each falling edge causes a flux transition on the media.
	Head Select	HS	Output. This high current output selects the floppy disk side for reading or writing. A logic "1" on this pin means side 0 will be accessed, while a logic "0" means side 1 will be accessed.
	Direction Control	DIRC	Output. This high current output determines the direction of the head movement. A logic "1" on this pin means outward motion, while a logic "0" means inward motion.
	Step Pulse	STEP	Output. This active low high current driver issues a low pulse for each track-to-track movement of the head.
	Disk Change	DCHG	Input. This active low input senses from the disk drive that the drive door is open or that the diskette has possibly been changed since the last drive selection.
	Drive Select 1	DS1	Output. This is an active low high current output. When the FDC37C77 is in the PC/AT Mode, a logic "0" on DSEL and a logic "1" on MOEN1 from the Digital Output Register will cause the signal to enable the drive number 1 interface. When the FDC37C77 is in the Base Mode or the Special Mode, this output is number 1 of the four decoded Unit Selects, as specified in the device command syntax.
	Drive Select 2	DS2	Output. This is an active low high current output. When the FDC37C77 is in the PC/AT Mode, a logic "0" on DSEL and a logic "1" on MOEN2 from the Digital Output Register will cause the signal to enable the interface in drive number 2. When the FDC37C77 is in the Base Mode or the Special Mode, this output is number 2 of the four decoded Unit Selects, as specified in the device command syntax.
	Motor On 1/ Drive Select 3	MO1/DS3	Output. This is an active low high current output. When the FDC37C77 is in the PC/AT Mode, a logic "1" on MOEN1 from the Digital Output Register will cause this output to go low, thereby acting as the Motor On Enable for drive number 1. When the FDC37C77 is in the Base Mode or the Special Mode, this output is number 3 of the four decoded Unit Selects, as specified in the device command syntax, thereby acting as drive select 3.
	Motor On 2/ Drive Select 4	MO2/DS4	Output. This is an active low high current output. When the FDC37C77 is in the PC/AT Mode, a logic "1" on MOEN2 from the Digital Output Register will cause this output to go low, thereby acting as the Motor On Enable for drive number 2. When the FDC37C77 is in the Base Mode or the Special Mode, this output is number 4 of the four decoded Unit Selects, as specified in the device command syntax, thereby acting as drive select 4.
	Reduced Write Current/ Revolutions Per Minute	RWC/RPM	Output. This active low signal occurs when tracks greater than 28 are being accessed, and the inner track locations have caused increased bit density. This signal, valid in the Base Mode and the Special Mode, indicates that write precompensation is necessary. In the PC/AT mode, this active low signal may be used to select a 300 RPM spindle rate on two speed drives when 250 Kbps MFM is selected.
	Write Protected	WP	Input. This active low, Schmitt Trigger input senses from the disk drive that a disk is write protected.

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	DESCRIPTION
	Track 00	TR00	Input. This active low, Schmitt Trigger input senses from the disk drive that the head is positioned over the outermost track, 00.
	Index	IDX	Input. This active low, Schmitt Trigger input senses from the disk drive that the head is positioned over the beginning of a track.
	Precomp-ensation Value	PCVAL	Input. The level on this pin determines the amount of write precompensation to be used on the inner tracks of the diskette. Logic "1" programs the value of 125 ns; Logic "0" programs 187 ns. This input has an internal pull up resistor.
	Drive Type	DRV	Input. This input is used to indicate the drive type being used. A logic "0" on this input indicates a two speed spindle motor.
IDE DRIVE INTERFACE			
	Chip Select 0	CS1F	Output. Active low chip select for the IDE drive's CS1FX input. It is decoded from the AD0-AD9 PC/AT address inputs and is used by the IDE drive to select the host-accessible Command Block registers, 1F0H to 1F7H.
	Chip Select 1	CS3F	Output. Active low chip select for the IDE drive's CS3FX input. It is decoded from the AD0-AD9 PC/AT address inputs and is used by the IDE drive to select the host-accessible Control Block Registers, 3F6H and 3F7H.
	Buffered Address 0-2	DA0 - DA2	Buffered address bits A0, A1, and A2 to the IDE drive.
	Data Bits D0-D6	DD0 - DD6	Data bits DD0 through DD6 to/from the IDE drive.
	Data Bit D7	DD7	This signal from the IDE drive is buffered by the FDC37C77. It is connected to At bus data I/O pin SD7 when data transfer is to or from the IDE drive except when the FDC37C77 register 3F7H is being read. During register 3F7 reads, bit SD7 will be sourced by register 3F7 (Digital Input Register) when FADSEL = "1", or will be high impedance when FADSEL = "0".
	Reset Drive	RST_DRV	This signal is the inverted and buffered RST from the host AT to the IDE drive.
	Drive I/O Write	DIOW	Buffered Drive I/O Write to the IDE drive.
	Drive I/O Read	DIOR	Buffered Drive I/O Read to the IDE drive.
	IDE Address Select	IDESEL	This input with internal pull-up resistor is used to select the Primary or Secondary floppy disk controller AT addresses for the IDE drive. When IDESEL = "1", the Primary Addresses are selected. When IDESEL = "0", the Secondary Addresses are selected.
	High Buffer Enable	BUFHIEN	This output enables the optional external LS245 Buffer for the AT upper eight data bits.
MISCELLANEOUS			
	Crystal	XTAL	An external 24 MHz parallel resonant crystal should be connected to these pins for all standard data rates. If an external TTL clock is used, it should be connected to XTAL, and XTAL should be left floating.
	Crystal	XTAL	
	Power Supply	V_{cc}	+ 5 Volt supply pin.
	Ground	GND	Ground pin.

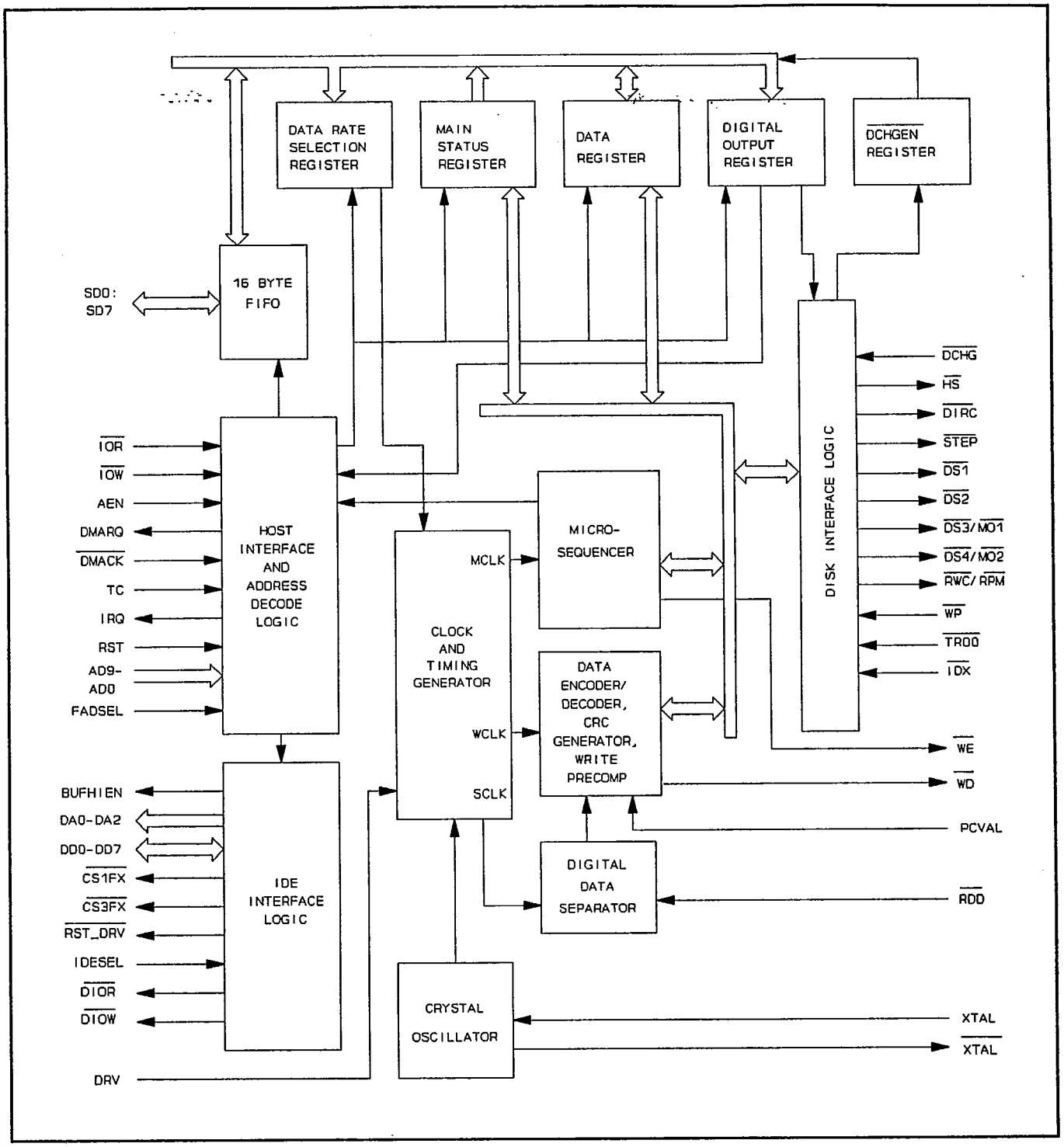
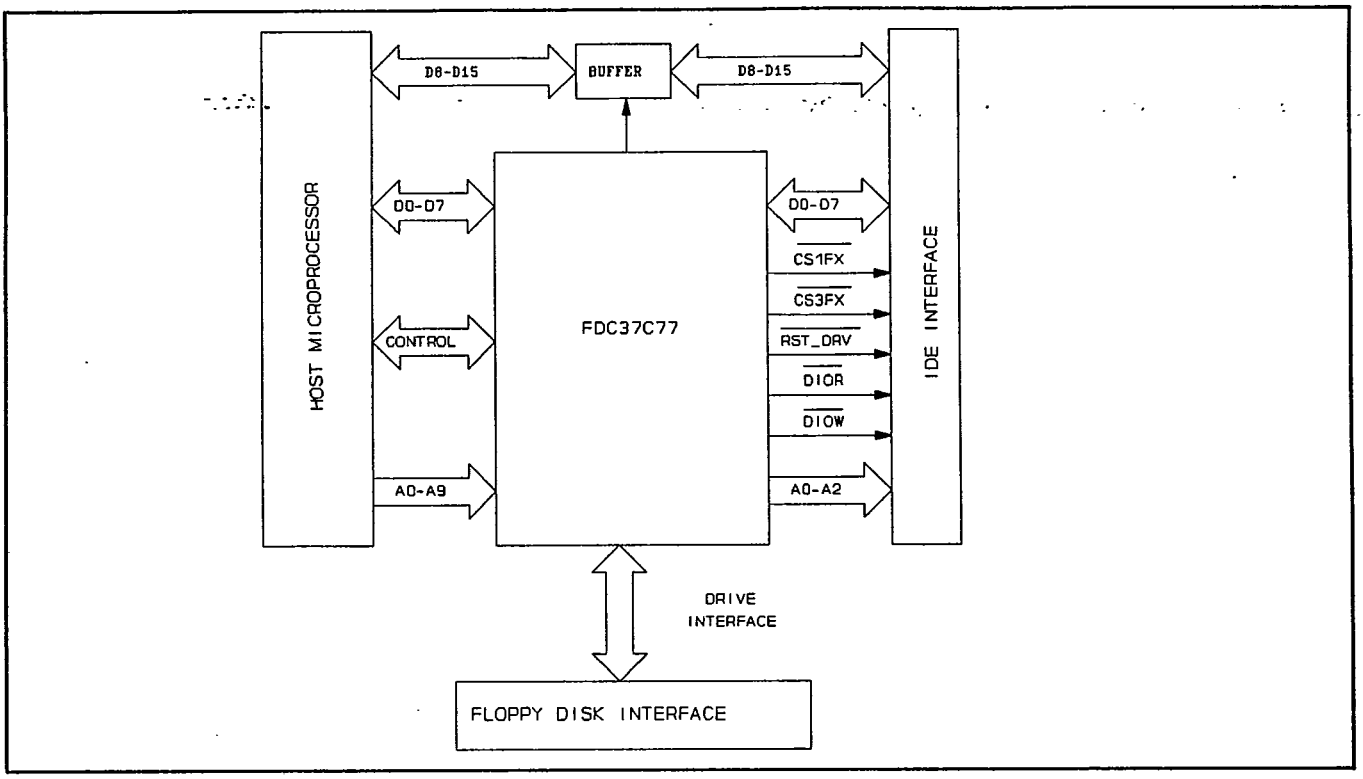


Figure 1: FDC37C77 BLOCK DIAGRAM

TYPICAL APPLICATION: FLOPPY DISK CONTROLLER WITH IDE INTERFACE



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