

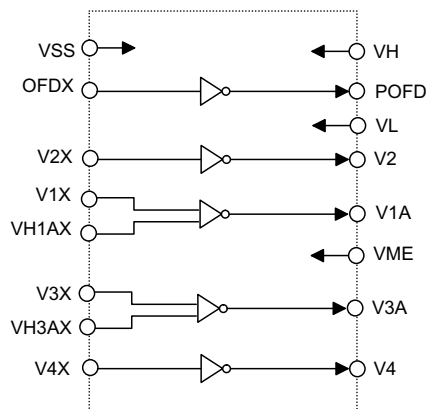
### Features

- Input voltage: 3.0V~5.5V
- Seven Integrated Circuits
  - ♦ 2-level output:
    - 2 circuits for vertical CCD clock driver output voltage level (typ.) = -8.5V to 0V.
  - ♦ 3-level output:
    - 2 circuits for vertical CCD clock driver output voltage level (typ.) = -8.5V to 15V.
  - ♦ 2-level output:
    - 1 circuits for shutter driver output voltage level (typ.) = -8.5V to 15V.
- Switchable between NTSC(EIA) and PAL(CCIR) modes
- 16-pin SSOP, 16-pin TSSOP package

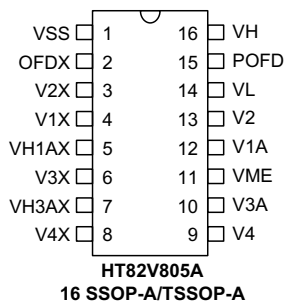
### General Descriptions

The HT82V805A is a CMOS vertical clock driver and shutter driver IC for CCD area sensors. It has the capability of converting the voltage and impedance from the CMOS level.

### Block Diagram



### Pin Assignment



## Pin Description

Pin Name	I/O	Description
VSS	—	Negative power supply, ground
OFDX	I	Electronic shutter pulse input
V1X, V2X, V3X, V4X	I	Vertical transfer pulse input
VH1AX, VH3AX	I	Pulse that transfers the charge of the photo-diode to the vertical shift register
VH	—	Power supply for high level of V1A, V3A
V4	O	Pulse to drive vertical CCD shift register (2 level: VME, VL)
V3A	O	Pulse to drive vertical CCD shift register (3 level: VME, VL, VH)
VME	—	Power supply for intermediate level of V1A, V3A
V1A	O	Pulse to drive vertical CCD shift register (3 level: VME, VL, VH)
V2	O	Pulse to drive vertical CCD shift register (2 level: VME, VL)
VL	—	Power supply for all low level output pulses
POFD	O	Electronic shutter pulse output (2 level: VL, VH)

## Absolute Maximum Ratings

Supply Voltage .....	$V_{SS}-0.3V$ to $V_L+3.5V$	Storage Temperature .....	$-55^{\circ}C$ to $150^{\circ}C$
Input Voltage .....	$V_{SS}-0.3V$ to $V_H+0.3V$	Operating Temperature .....	$-25^{\circ}C$ to $70^{\circ}C$

Note: These are stress ratings only. Stresses exceeding the range specified under “Absolute Maximum Ratings” may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

## Recommended Operating Conditions

Symbol	Parameter	Value	Unit
$V_H$	Supply Voltage	$-0.3 \sim V_L + 3.5$	V
$V_L$		$0 \sim -10$	V
VEM		$V_L - 0.3 \sim 3.0$	V
V1A, V2, V3A, V4, POFD	Output Voltage	$V_L - 0.3 \sim V_H + 0.3$	V

## Logic Function Table

Input				Output		
V1X, V3X	VH1AX, VH3AX	V2X, V4X	OFDX	V1A, V3A	V2, V4	POFD
L	L	—	—	VH	—	—
L	L	—	—	Z	—	—
H	H	—	—	VME	—	—
H	H	—	—	VL	—	—
—	—	L	—	—	—	—
—	—	H	—	—	VME	—
—	—	—	—	—	VL	—
—	—	—	L	—	—	VH
—	—	—	H	—	—	VL

## D.C. Characteristics

 $V_H = 15V, V_{ME} = 0V, V_L = -8.5V, T_a = 25^\circ C$ 

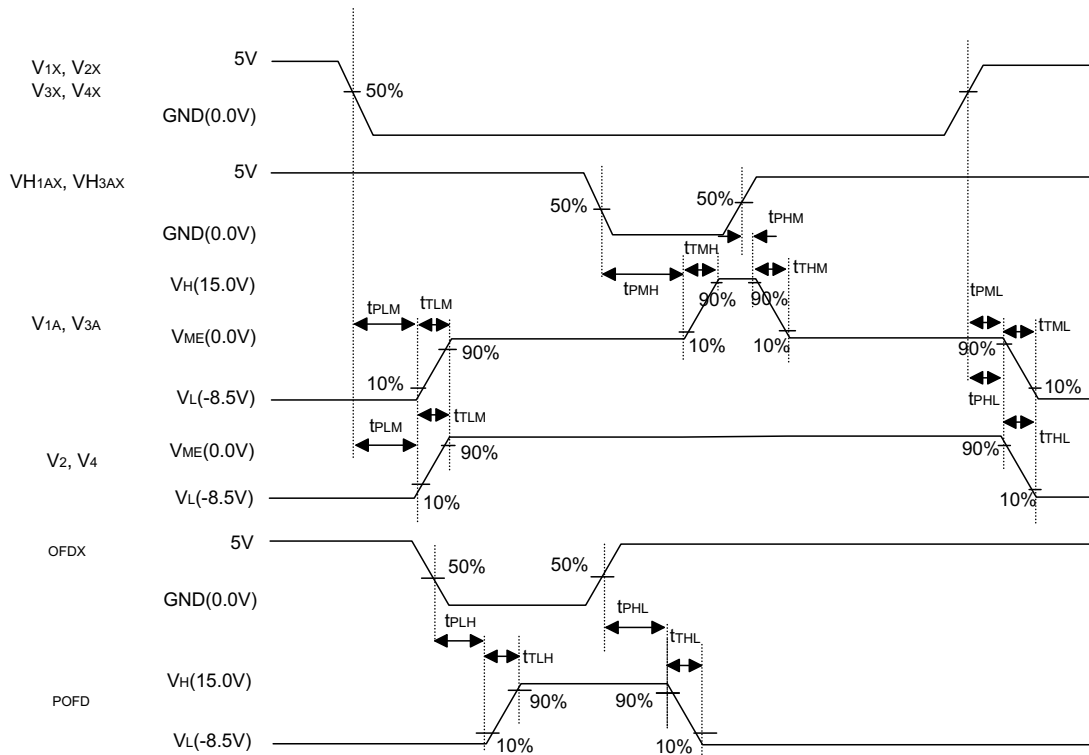
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{DD}$	Logic Supply Voltage	—	3.0	3.3	5.5	V
$V_H$	Supply Voltage	—	14.5	15.0	15.5	V
$V_L$		—	-9.5	-8.5	-7.5	V
$V_{IH}$	High Level Input Voltage	—	2.3	—	—	V
$V_{IL}$	Low Level Input Voltage	—	—	—	1.2	V
$I_{VH}$	Operating Current	Shutter speed = 100kHz	—	2.9	—	mA
$I_{VL}$			—	-1.7	—	mA
$I_{OL}$	Output Current	V1A, V2, V3A, V4 = -8.0V	—	31.5	—	mA
$I_{OM1}$		V1A, V2, V3A, V4 = -0.5V	—	-8.5	—	mA
$I_{OM2}$		V1A, V3A = 0.5V	—	8.5	—	mA
$I_{OH}$		V1A, V3A = 14.5V	—	-10	—	mA
$I_{OSL}$		OFDX = -8.0V	—	18.5	—	mA
$I_{OSH}$		POFD = 14.5V	—	-8.0	—	mA

## A.C. Characteristics

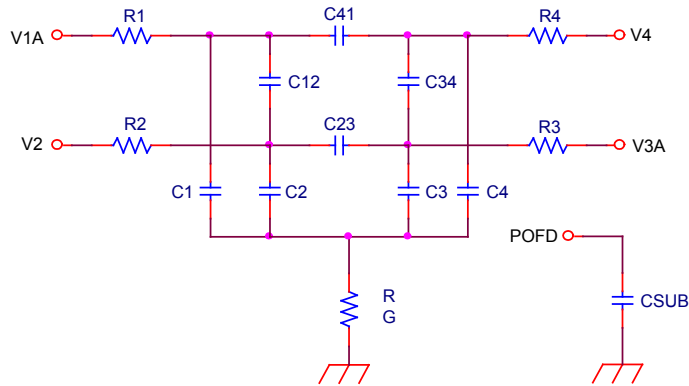
 $V_H = 15V, V_{ME} = 0V, V_L = -8.5V, T_a = 25^\circ C$ 

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{PLM}$	Delay Time	—	—	70	—	ns
$t_{PMH}$		—	—	70	—	ns
$t_{PLH}$		—	—	70	—	ns
$t_{PML}$		—	—	70	—	ns
$t_{PHM}$		—	—	70	—	ns
$t_{PHL}$		—	—	70	—	ns
$t_{TLM}$	Rising Time	—	—	800	—	ns
$t_{TMH}$		—	—	1000	—	ns
$t_{TLH}$		—	—	320	—	ns
$t_{TML}$		—	—	900	—	ns
$t_{THM}$		—	—	1400	—	ns
$t_{THL}$		—	—	220	—	ns

### Timing Diagram

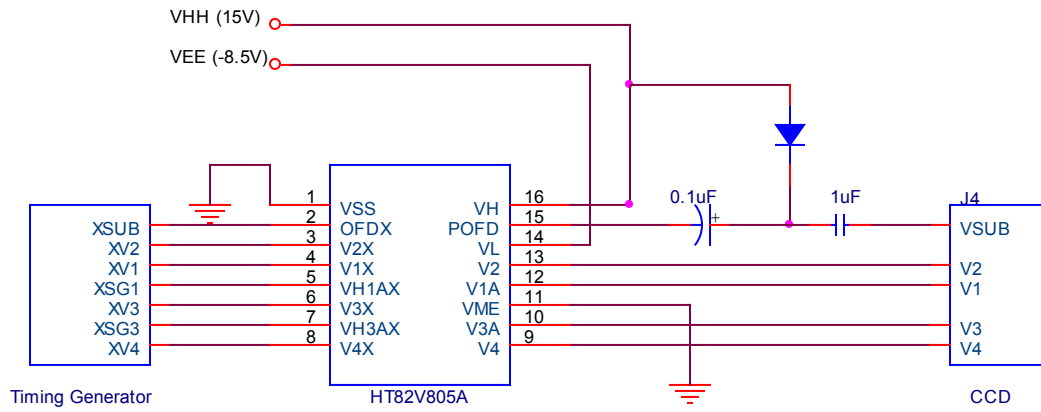


### Test Circuits



Note: R1 to R4=27Ω  
 C1 to C4=3300pF  
 CSUB=500pF  
 RG=5Ω  
 C12, C23, C34, C41=1500pF

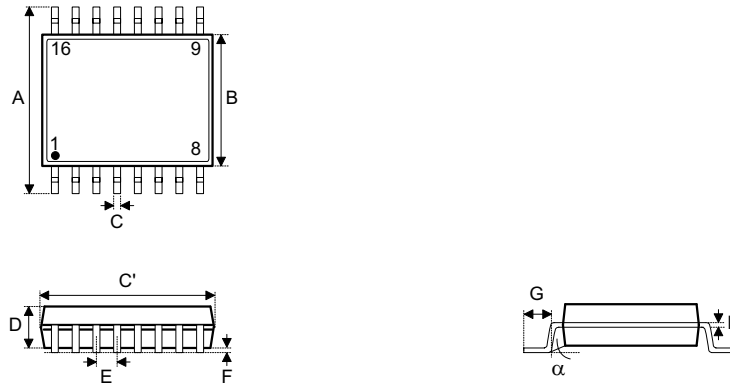
Application Circuits



## Package Information

Note that the package information provided here is for consultation purposes only. As this information may be updated at regular intervals users are reminded to consult the Holtek website (<http://www.holtek.com.tw/english/literature/package.pdf>) for the latest version of the package information.

### 16-pin SSOP (150mil) Outline Dimensions

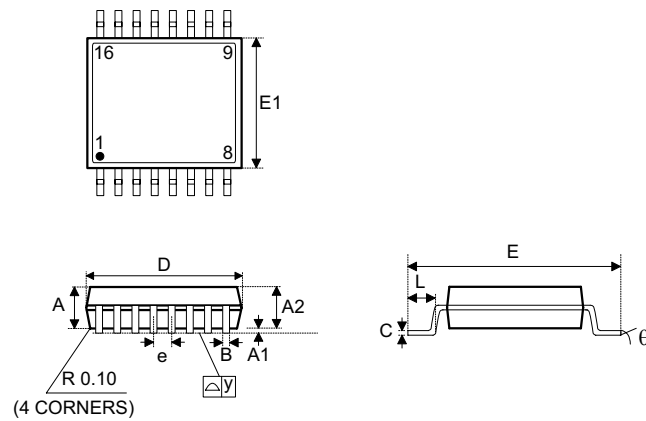


### 16-pin SSOP (150mil)

Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	0.228	—	0.244
B	0.150	—	0.157
C	0.008	—	0.012
C'	0.189	—	0.197
D	0.054	—	0.060
E	—	0.025	—
F	0.004	—	0.010
G	0.022	—	0.028
H	0.007	—	0.010
$\alpha$	0°	—	8°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	5.79	—	6.20
B	3.81	—	3.99
C	0.20	—	0.30
C'	4.80	—	5.00
D	1.37	—	1.52
E	—	0.64	—
F	0.10	—	0.25
G	0.56	—	0.71
H	0.18	—	0.25
$\alpha$	0°	—	8°

16-pin TSSOP Outline Dimensions

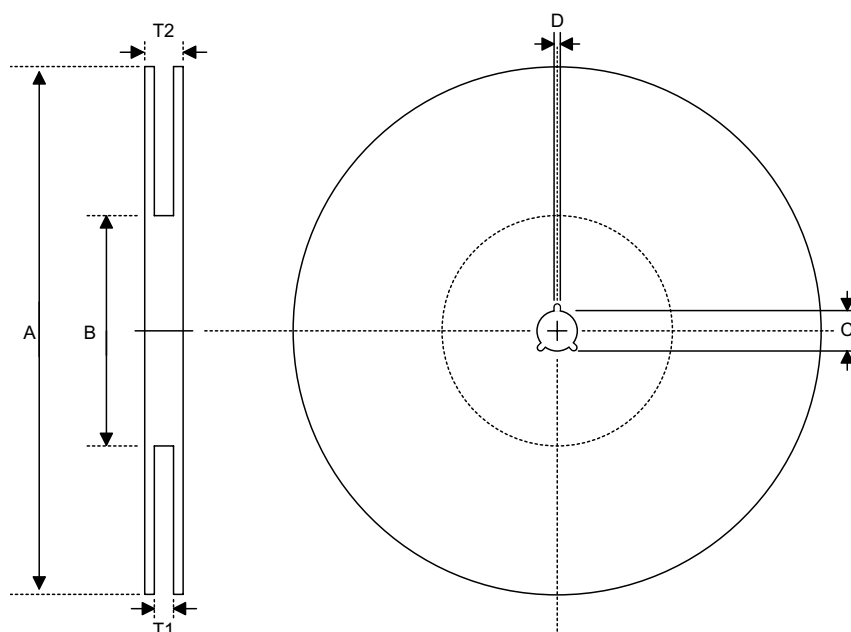


16-pin TSSOP

Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	0.039	—	0.041
A1	0.002	—	0.006
A2	0.041	—	0.047
B	—	0.010	—
C	0.004	—	0.006
D	0.193	—	0.201
E	0.244	—	0.260
E1	0.169	—	0.177
e	—	0.026	—
L	0.020	—	0.028
y	—	—	0.003
$\theta$	0°	—	8°

Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	1.00	—	1.05
A1	0.05	—	0.15
A2	1.05	—	1.20
B	—	0.25	—
C	0.11	—	0.15
D	4.90	—	5.10
E	6.20	—	6.60
E1	4.30	—	4.50
e	—	0.65	—
L	0.50	—	0.70
y	—	—	0.076
$\theta$	0°	—	8°

Reel Dimensions



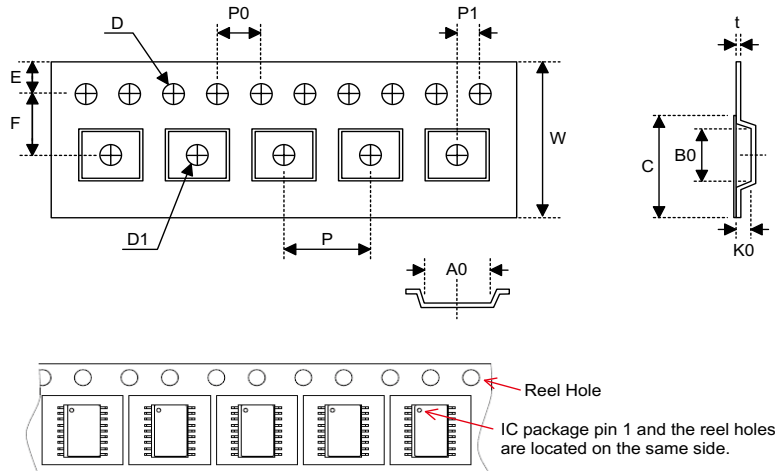
16-pin SSOP

Symbol	Description	Dimensions in mm
A	Reel Outer Diameter	330.0±1.0
B	Reel Inner Diameter	100.0±1.5
C	Spindle Hole Diameter	13.0 <sup>+0.5/-0.2</sup>
D	Key Slit Width	2.0±0.5
T1	Space Between Flange	12.8 <sup>+0.3/-0.2</sup>
T2	Reel Thickness	18.2±0.2

16-pin TSSOP

Symbol	Description	Dimensions in mm
A	Reel Outer Diameter	330.0±1.0
B	Reel Inner Diameter	100.0±1.5
C	Spindle Hole Diameter	13.0 <sup>+0.5/-0.2</sup>
D	Key Slit Width	2.0±0.5
T1	Space Between Flange	16.8 <sup>+0.3/-0.2</sup>
T2	Reel Thickness	22.2±0.2



**Carrier Tape Dimensions**

**16-pin SSOP**

Symbol	Description	Dimensions in mm
W	Carrier Tape Width	12.0 <sup>+0.3/-0.1</sup>
P	Cavity Pitch	8.0±0.1
E	Perforation Position	1.75±0.10
F	Cavity to Perforation (Width Direction)	5.5±0.1
D	Perforation Diameter	1.55±0.10
D1	Cavity Hole Diameter	1.50 <sup>+0.25/-0.00</sup>
P0	Perforation Pitch	4.0±0.1
P1	Cavity to Perforation (Length Direction)	2.0±0.1
A0	Cavity Length	6.4±0.1
B0	Cavity Width	5.2±0.1
K0	Cavity Depth	2.1±0.1
t	Carrier Tape Thickness	0.30±0.05
C	Cover Tape Width	9.3±0.1

**16-pin TSSOP**

Symbol	Description	Dimensions in mm
W	Carrier Tape Width	16.0 <sup>+0.3/-0.1</sup>
P	Cavity Pitch	8.0±0.1
E	Perforation Position	1.75±0.10
F	Cavity to Perforation (Width Direction)	7.5±0.5
D	Perforation Diameter	1.5 <sup>+0.1/-0.0</sup>
D1	Cavity Hole Diameter	1.5 <sup>+0.1/-0.0</sup>
P0	Perforation Pitch	4.0±0.1
P1	Cavity to Perforation (Length Direction)	2.0±0.1
A0	Cavity Length	6.8±0.1
B0	Cavity Width	5.4±0.1
K0	Cavity Depth	1.6±0.1
t	Carrier Tape Thickness	0.300±0.013
C	Cover Tape Width	13.3±0.1

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