12 x 12-bit parallel multiplier

LMU12

general information

The LMU12 is a 12-bit parallel multiplier featuring high speed and low power consumption. The LMU12 multiplier is pin and functionally compatible with TRW MPY-12HJ parts. Full military ambient temperature range operation is attained by the use of advanced CMOS technology.

The A and B operands and their mode controls TCA, TCB have 13-bit input registers. A logical one on the TCA or TCB input specifies the corresponding operand as two's complement format.

At the output, a right shift control (RS) allows the user to select either a left shifted 23-bit product suitable for two's complement only, or a full 24-bit product.

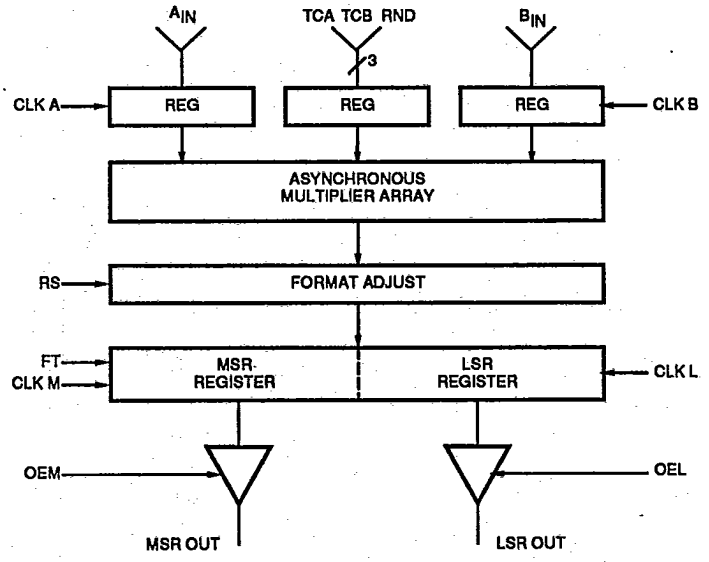
Two 12-bit output registers are provided to hold the most and least significant halves of the result (MSR and LSR) as defined by RS. For asynchronous output these registers may be made transparent by taking the feed through control (FT) high. A round control (RND) allows the rounding of the MSR; this control is registered, and is entered whenever either input register is clocked.

In the LMU12 the A, B, MSR and LSR registers have independent clocks: CLKA, CLKB, CLKM, CLKL.

features

- High-speed **(35ns)**, low-power (60mW) CMOS 12 x 12 Parallel Multiplier
- LMU12 functionally and pin compatible with **TRW MPY-12HJ**
- TTL inputs and outputs
- Three-state outputs
- Two's complement, unsigned, or mixed operands
- High-Rel screening available

functional diagram



LMU12 FUNCTIONAL DIAGRAM

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device pinouts

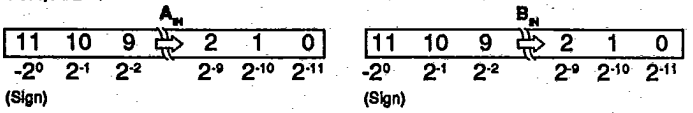
PIN P,D	PIN G[1]	Function	PIN P,D	PIN G[1]	Function
1	F02	A7	35	G10	R18
2	F01	A6	36	G11	R19
3	E02	A5	37	H10	R20
4	E01	A4	38	H11	R21
5	D02	A3	39	J10	R22
6	D01	A2	40	J11	R23
7	C02	A1	41	K10	TCB
8	C01	A0	42	L10	B11
9	B02	R0	43	K09	B10
10	A02	R1	44	L09	B9
11	B03	R2	45	K08	B8
12	A03	R3	46	L08	B7
13	B04	R4	47	K07	B6
14	A04	R5	48	L07	V_{cc}
15	B05	R6	49	K06	V_{cc}
16	A05	R7	50	L06	V_{cc}
17	B06	R8	51	K05	B5
18	A06	R9	52	L05	B4
19	B07	R10	53	K04	B3
20	A07	R11	54	L04	B2
21	B08	/OEL	55	K03	B1
22	A08	/OEM	56	L03	B0
23	B09	GND	57	K02	TCA
24	A09	GND	58	K01	RND
25	B10	FT	59	J02	CLKB
26	B11	RS	60	J01	CLKA
27	C10	CLKL	61	H02	A11
28	C11	CLKM	62	H01	A10
29	D10	R12	63	G02	A9
30	D11	R13	64	G01	A8
31	E10	R14		A10	NC
32	E11	R15		K11	NC
33	F10	R16		L02	NC
34	F11	R17		B01	NC

NC= No Connection
1) See mechanical data section of LOGIC DEVICES PRODUCT CATALOG for pin number to pin location correspondence

INPUT FORMATS

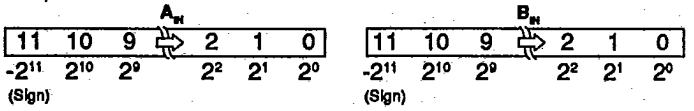
Fractional Two's Complement

TCA,TCB=1



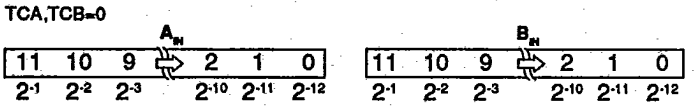
Integer Two's Complement

TCA,TCB=1



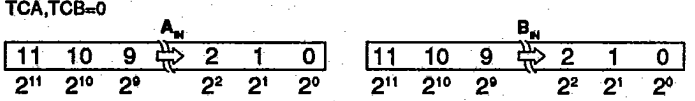
Unsigned Fractional

TCA,TCB=0



Unsigned Integer

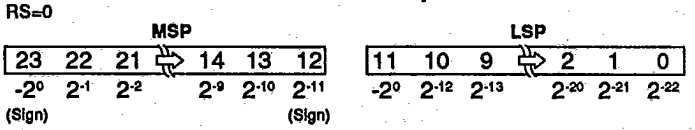
TCA,TCB=0



OUTPUT FORMATS

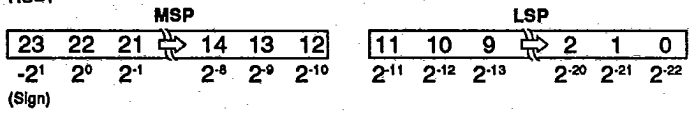
Fractional Two's Complement*

RS=0



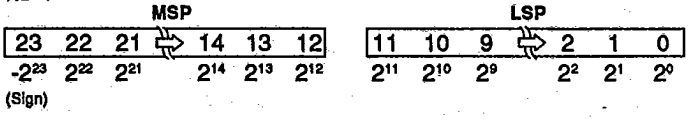
Fractional Two's Complement (Shifted)

RS=1



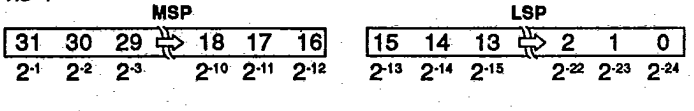
Integer Two's Complement

RS=1



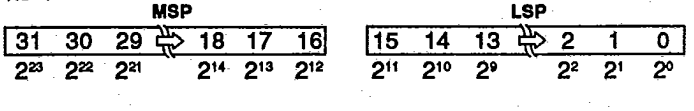
Unsigned Fractional

RS=1



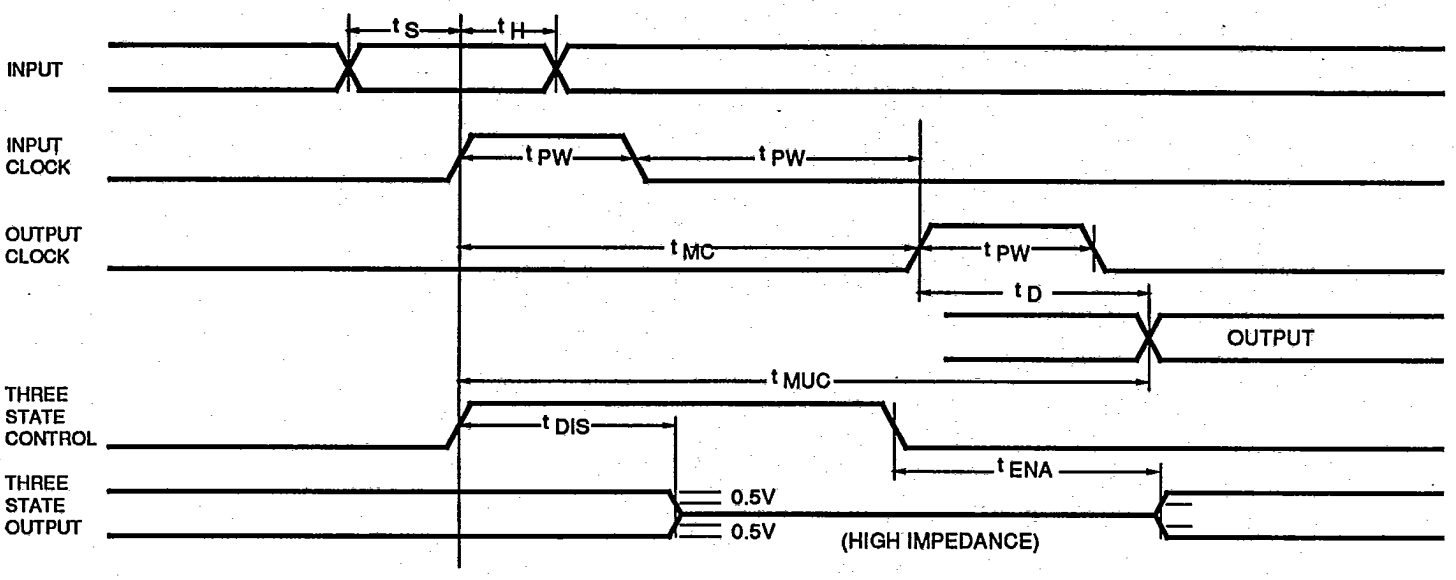
Unsigned Integer

RS=1



*In this format an overflow occurs when the 2's complement number 1.00...(-1) is multiplied with itself. The result of the multiplication is 1.000...(-1).

timing diagram



switching characteristics

I. LMU12 Guaranteed Performance - Commercial Range

	Suffix:	None		65		45		35		units
PARAMETER	DESCRIPTION	min	max	min	max	min	max	min	max	
t_{MC}	Multiply Time (Clocked)		80		65		45		35	ns
t_{MUC}	Unclocked Multiply Time		110		95		65		55	
t_{D}	Output Delay		30		26		25		25	
t_{ENA}	Three-State Enable Time		26		22		22		20	
t_{DIS}	Three-State Disable Time		24		20		20		18	
t_{PW}	Clock Pulse Width	25		25		15		15		
t_{H}	Input Register Hold Time	5		0		0		0		
t_{S}	Input Register Setup Time	15		15		15		10		

AC TEST CONDITIONS: Input levels: 0 to 3V Output timing reference level: 1.5V Output load: 1.0KΩ to 5V, 820Ω to GND, 60pF to GND

II. LMU12 Guaranteed Performance - Military Range

	Suffix:	None		75		55		45		units
PARAMETER	DESCRIPTION	min	max	min	max	min	max	min	max	
t_{MC}	Multiply Time (Clocked)		100		75		55		45	ns
t_{MUC}	Unclocked Multiply Time		130		110		75		65	
t_{D}	Output Delay		35		30		30		25	
t_{ENA}	Three-State Enable Time		35		26		26		24	
t_{DIS}	Three-State Disable Time		35		24		24		22	
t_{PW}	Clock Pulse Width	25		25		20		15		
t_{H}	Input Register Hold Time	6		0		0		0		
t_{S}	Input Register Setup Time	20		18		15		12		

AC TEST CONDITIONS: Input levels: 0 to 3V Output timing reference level: 1.5V Output load: 1.0KΩ to 5V, 820Ω to GND, 60pF to GND

12 x 12-bit parallel multiplier

LMU12

absolute maximum ratings

Supply Voltage	-0.5V to 7.0V
Input Voltage	0V to 5.5V
Output Voltage	0V to 5.5V
Operating Temperature (Ambient)	-55°C to 125 °C
Storage Temperature	-65°C to 150°C

recommended operating conditions

PARAMETER	DESCRIPTION		min	typ	max	unit
V_{CC}	Supply Voltage	Commercial	4.75	5.0	5.25	V
		Military	4.50	5.0	5.5	V
I_{OL}	Low Level Output Current				4.0	mA
I_{OH}	High Level Output Current				-2.0	mA
T_{AMB}	Operating Temperature	Commercial	0	25	70	°C
		Military	-55	25	125	°C

electrical characteristics

PARAMETER	DESCRIPTION		min	typ	max	unit
V_{IL}	Low level Input Voltage				0.8	V
V_{IH}	High Level Input Voltage		2.0			V
V_{OL}	Low Level Output Voltage (I_{OL} = 4 mA)				0.5	V
V_{OH}	High Level Output Voltage (I_{OH} = -2 mA)		3.5			V
I_{IL}	Low Level Input Current (V_{IL} = 0.4 V)				20	µA
I_{IH}	High Level Input Current (V_{IH} = 2.4 V)				20	µA
I_{OZ}	Output Current (High-Impedance State)				20	µA
I_{CC}	Supply Current	(Quiescent)			1.0	mA
		(Dynamic)		12[1]	25[2]	mA

1) 5 MHz clock rate, V_{IH} = 2.4V, V_{IL} = 0.4V, V_{CC} = 5V, T_{AMB} = 25°C, random input patterns; no load.
2) 5 MHz clock rate, V_{IH} = 2.0V, V_{IL} = 0.8V, V_{CC} = 5.5V, T_{AMB} = -55°C, all outputs toggling every cycle; no load.

ordering information

Ordering Code	Speed (NS)	Package Type	Operating Range
LMU12 PC-35	35	P4	Commercial
LMU12 DC-35		D6	
LMU12 GC-35		G2	
LMU12 PCR-35		P4	
LMU12 DCR-35		D6	
LMU12 GCR-35		G2	
LMU12 PC-45	45	P4	Commercial
LMU12 DC-45		D6	
LMU12 GC-45		G2	
LMU12 PCR-45		P4	
LMU12 DCR-45		D6	
LMU12 GCR-45		G2	
LMU12 DM-45	45	D6	Military
LMU12 GM-45		G2	
LMU12 DMB-45		D6	
LMU12 GMB-45		G2	
LMU12 DM-55	55	D6	Military
LMU12 GM-55		G2	
LMU12 DMB-55		D6	
LMU12 GMB-55		G2	
LMU12 PC-65	65	P4	Commercial
LMU12 DC-65		D6	
LMU12 GC-65		G2	
LMU12 PCR-65		P4	
LMU12 DCR-65		D6	
LMU12 GCR-65		G2	
LMU12 DM-75	75	D6	Military
LMU12 GM-75		G2	
LMU12 DMB-75		D6	
LMU12 GMB-75		G2	
LMU12 PC	80	P4	Commercial
LMU12 DC		D6	
LMU12 GC		G2	
LMU12 PCR		P4	
LMU12 DCR		D6	
LMU12 GCR		G2	
LMU12 DM	100	D6	Military
LMU12 GM		G2	
LMU12 DMB		D6	
LMU12 GMB		G2	

LOGIC DEVICES INCORPORATED

LOGIC Devices Incorporated 628 East Evelyn Avenue Sunnyvale, California 94086 (408) 720-8630 Telex 172 387