| REVISIONS | | | |
|---|---|---|---|
| LTR | DESCRIPTION | DATE (YR-MO-DA) | APPROVED |
| A | Add device type 05. Update boilerplate. Make corrections to figure 4. Editorial changes throughout. | 94-06-22 | M.A. Frye |

| REV | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SHEET | | | | | | | | | | | | | | | | | | | |
| REV | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| SHEET | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 | 32 | 33 | 34 |

| REV STATUS OF SHEETS | REV | A | A | A | A | A | A | A | A | A | A | A | A | A |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | SHEET | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 |

PMIC N/A

**STANDARDIZED MILITARY DRAWING**

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
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DRAWING APPROVAL DATE
12 MAY 1990

REVISION LEVEL A

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

# MICROCIRCUIT, MEMORY, DIGITAL, CMOS, 4K X 9 PARALLEL SERIAL FIFO, MONOLITHIC SILICON

| SIZE | CAGE CODE | 5962-89943 |
|---|---|---|
| A | 67268 | |

SHEET 1 OF 34

DESC FORM 193
JUL 91

5962-E256-94

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

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1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example:

1.2.1 Device type(s). The device type(s) shall identify the circuit function as follows:

| Device type | Generic number | Circuit function | Access time |
|---|---|---|---|
| 01 | (see 6.6) | 4k X 9-bit parallel-serial FIFO | 120 ns |
| 02 | (see 6.6) | 4k X 9-bit parallel-serial FIFO | 80 ns |
| 03 | (see 6.6) | 4k X 9-bit parallel-serial FIFO | 65 ns |
| 04 | (see 6.6) | 4k X 9-bit parallel-serial FIFO | 50 ns |
| 05 | (see 6.6) | 4k X 9-bit parallel-serial FIFO | 40 ns |

1.2.2 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

| Outline letter | Descriptive designator | Terminals | Package style |
|---|---|---|---|
| Q | GDIP1-T40 or CDIP2-T40 | 40 | Dual-in-line |
| X | CQCC1-N44 | 44 | Square leadless chip carrier |

1.2.3 Lead finish. The lead finish shall be as specified in MIL-STD-883 (see 3.1 herein). Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings.

Terminal voltage with respect to ground . . . . . -0.5 V dc to +7.0 V dc
DC output current . . . . . 50 mA
Storage temperature range . . . . . -65°C to +150°C
Maximum power dissipation ($P_D$) . . . . . 1.0 W
Lead temperature (soldering, 10 seconds) . . . . . +260°C
Thermal resistance, junction-to-case ($\theta_{JC}$) . . . . . See MIL-STD-1835
Junction temperature ($T_J$) . . . . . +150°C 1/

1.4 Recommended operating conditions.

Supply voltage range ($V_{CC}$) . . . . . 4.5 V dc to 5.5 V dc
Minimum high level input voltage ($V_{IH}$) . . . . . 2.2 V dc
Maximum low level input voltage ($V_{IL}$) . . . . . +0.8 V dc 2/
Case operating temperature range ($T_C$) . . . . . -55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and bulletin. Unless otherwise specified, the following specification, standards, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

1/ Maximum junction temperature may be increased to +175°C during burn-in and steady-state life.
2/ 1.5 V undershoots are allowed for 10 ns once per cycle.



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SPECIFICATION

MILITARY

MIL-I-38535 - Integrated Circuits (Microcircuits) Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

(Copies of the specification, standards, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-I-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-I-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-I-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-STD-883 (see 3.1 herein) and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth tables. The truth tables shall be as specified on figure 2.

3.2.3 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103 (see 6.6 herein).

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.6 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.



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TABLE I. Electrical performance characteristics.

| Test | Symbol | Conditions<br>$-55°C \le T_C \le +125°C$<br>$V_{SS}$ = 0 V, 4.5 V ≤ $V_{CC}$ < 5.5 V<br>unless otherwise specified | | Device type | Group A subgroups | Limits | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | | Min | Max | |
| Input leakage current | $I_{LI}$ | 0.4 V ≤ $V_{IN}$ ≤ $V_{OUT}$ | | All | 1,2,3 | -10 | 10 | µA |
| Output leakage current | $I_{LO}$ | 0.4 V ≤ $V_{OUT}$ ≤ $V_{CC}$, $\overline{R} \ge V_{IH}$ | | All | 1,2,3 | -10 | 10 | µA |
| Output low voltage | $V_{OL}$ | $V_{CC}$ = 4.5 V, $V_{IL}$ = 0.8 V, $V_{IH}$ = 2.2 V | SO, $I_{OUT}$ = 16 mA | All | 1,2,3 | | 0.4 | V |
| | | | All other outputs, $I_{OUT}$ = 8.0 mA | | | | 0.4 | |
| Output high voltage | $V_{OH}$ | $V_{CC}$ = 4.5 V, $V_{IL}$ = 0.8 V, $V_{IH}$ = 2.2 V | SO, $I_{OUT}$ = -8.0 mA | All | 1,2,3 | 2.4 | | V |
| | | | All other outputs, $I_{OUT}$ = -2.0 mA | | | 2.4 | | |
| Power supply current | $I_{CC1}$ | f = $f_S$, outputs open, $V_{CC}$ = 5.5 V | | All | 1,2,3 | | 160 | mA |
| Average standby current | $I_{CC2}$ | $\overline{R} = \overline{W} = \overline{RS} = \overline{FL}/\overline{RT} = V_{IH}$, outputs open | | All | 1,2,3 | | 25 | mA |
| Power down current | $I_{CC3}$ | $\overline{RS} = \overline{FL}/\overline{RT} = \overline{W} = \overline{R}$ = $V_{CC}$ - 0.2 V, all other inputs ≥ $V_{CC}$ - 0.2 V or ≤ 0.2 V, outputs open | | All | 1,2,3 | | 4.0 | mA |
| Input capacitance 1/ | $C_{IN}$ | $V_I$ = 0 V, f = 1.0 MHz, $T_A$ = +25°C, see 4.3.1c | | All | 4 | | 10 | pF |
| Output capacitance 1/ | $C_{OUT}$ | $V_O$ = 0 V, f = 1.0 MHz, $T_A$ = +25°C, see 4.3.1c | | All | 4 | | 12 | pF |
| Functional tests | | See 4.3.1d | | All | 7,8A,8B | | | |
| Parallel I/O shift frequency | $f_S$ | $C_L$ = 30 pF, see figures 3 and 4 | | 01 | 9,10,11 | | 7.0 | MHz |
| | | | | 02 | | | 10 | |
| | | | | 03 | | | 12.5 | |
| | | | | 04 | | | 15 | |
| | | | | 05 | | | 20 | |

See footnotes at end of table.



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TABLE I. Electrical performance characteristics - Continued.

| Test | Symbol | Conditions<br>$-55°C \le T_C \le +125°C$<br>$V_{SS}$ = 0 V, 4.5 V $\le V_{CC} <$ 5.5 V<br>unless otherwise specified | Device type | Group A subgroups | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| Serial-out shift frequency | $f_{SOCP}$ | $C_L$ = 30 pF, see figures 3 and 4 | 01 | 9,10,11 | | 25 | MHz |
| | | | 02 | | | 28 | |
| | | | 03 | | | 33 | |
| | | | 04 | | | 40 | |
| | | | 05 | | | 50 | |
| Serial-in shift frequency | $f_{SICP}$ | | 01 | 9,10,11 | | 25 | MHz |
| | | | 02 | | | 28 | |
| | | | 03 | | | 33 | |
| | | | 04 | | | 40 | |
| | | | 05 | | | 50 | |
| PARALLEL OUTPUT MODE TIMINGS | | | | | | | |
| Access time | $t_A$ | $C_L$ = 30 pF, see figures 3 and 4 | 01 | 9,10,11 | | 120 | ns |
| | | | 02 | | | 80 | |
| | | | 03 | | | 65 | |
| | | | 04 | | | 50 | |
| | | | 05 | | | 40 | |
| Read recovery time | $t_{RR}$ | | 01,02 | 9,10,11 | 20 | | ns |
| | | | 03,04 | | 15 | | |
| | | | 05 | | 10 | | |
| Read pulse width | $t_{RPW}$ | | 01 | 9,10,11 | 120 | | ns |
| | | | 02 | | 80 | | |
| | | | 03 | | 65 | | |
| | | | 04 | | 50 | | |
| | | | 05 | | 40 | | |

See footnotes at end of table.



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TABLE I. Electrical performance characteristics - Continued.

| Test | Symbol | Conditions<br>$-55°C \le T_C \le +125°C$<br>$V_{SS}$ = 0 V, $4.5 V \le V_{CC} < 5.5$ V<br>unless otherwise specified | Device type | Group A subgroups | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| Read cycle time | $t_{RC}$ | $C_L$ = 30 pF, see figures 3 and 4 | 01 | 9,10,11 | 140 | | ns |
| | | | 02 | | 100 | | |
| | | | 03 | | 80 | | |
| | | | 04 | | 65 | | |
| | | | 05 | | 50 | | |
| Write pulse low to data bus at low Z 2/ | $t_{WLZ}$ | | 01,02 | 9,10,11 | 20 | | ns |
| | | | 03,04 | | 15 | | |
| | | | 05 | | 5 | | |
| Read pulse low to data bus at low Z 2/ | $t_{RLZ}$ | | 01-04 | 9,10,11 | 10 | | ns |
| | | | 05 | | 5 | | |
| Read pulse high to data bus at high Z 2/ | $t_{RHZ}$ | | 01,02 | 9,10,11 | | 35 | ns |
| | | | 03,04 | | | 30 | |
| | | | 05 | | | 25 | |
| Data valid from read pulse high | $t_{DV}$ | | All | 9,10,11 | 5.0 | | ns |
| PARALLEL INPUT MODE TIMINGS | | | | | | | |
| Data setup time | $t_{DS}$ | $C_L$ = 30 pF, see figures 3 and 4 | 01,02 | 9,10,11 | 40 | | ns |
| | | | 03,04 | | 30 | | |
| | | | 05 | | 20 | | |
| Data hold time | $t_{DH}$ | | 01-03 | 9,10,11 | 10 | | ns |
| | | | 04 | | 5.0 | | |
| | | | 05 | | 0 | | |
| Write cycle time | $t_{WC}$ | | 01 | 9,10,11 | 140 | | ns |
| | | | 02 | | 100 | | |
| | | | 03 | | 80 | | |
| | | | 04 | | 65 | | |
| | | | 05 | | 50 | | |

See footnotes at end of table.



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TABLE I. Electrical performance characteristics - Continued.

| Test | Symbol | Conditions<br>$-55°C \le T_C \le +125°C$<br>$V_{SS}$ = 0 V, 4.5 V $\le V_{CC} <$ 5.5 V<br>unless otherwise specified | Device type | Group A subgroups | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| Write pulse width | $t_{WPW}$ | $C_L$ = 30 pF, see figures 3 and 4 | 01 | 9,10,11 | 120 | | ns |
| | | | 02 | | 80 | | |
| | | | 03 | | 65 | | |
| | | | 04 | | 50 | | |
| | | | 05 | | 40 | | |
| Write recovery time | $t_{WR}$ | | 01,02 | 9,10,11 | 20 | | ns |
| | | | 03,04 | | 15 | | |
| | | | 05 | | 10 | | |
| RESET TIMINGS | | | | | | | |
| Reset cycle time | $t_{RSC}$ | $C_L$ = 30 pF, see figures 3 and 4 | 01 | 9,10,11 | 140 | | ns |
| | | | 02 | | 100 | | |
| | | | 03 | | 80 | | |
| | | | 04 | | 65 | | |
| | | | 05 | | 50 | | |
| Reset pulse width | $t_{RS}$ | | 01 | 9,10,11 | 120 | | ns |
| | | | 02 | | 80 | | |
| | | | 03 | | 65 | | |
| | | | 04 | | 50 | | |
| | | | 05 | | 40 | | |
| Reset setup time | $t_{RSS}$ | | 01 | 9,10,11 | 120 | | ns |
| | | | 02 | | 80 | | |
| | | | 03 | | 65 | | |
| | | | 04 | | 50 | | |
| | | | 05 | | 40 | | |
| Reset recovery time | $t_{RSR}$ | | 01,02 | 9,10,11 | 20 | | ns |
| | | | 03,04 | | 15 | | |
| | | | 05 | | 10 | | |

See footnotes at end of table.



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TABLE I. Electrical performance characteristics - Continued.

| Test | Symbol | Conditions $-55°C \le T_C \le +125°C$, $V_{SS} = 0$ V, $4.5\ V \le V_{CC} < 5.5$ V unless otherwise specified | Device type | Group A subgroups | Limits Min | Limits Max | Unit |
|---|---|---|---|---|---|---|---|
| RESET TO FLAGS DELAYS | | | | | | | |
| Reset to $\overline{EF}$, $\overline{AEF}$, and EF+1 low | $t_{RSF1}$ | $C_L$ = 30 pF, see figures 3 and 4 | 01 | 9,10,11 | | 140 | ns |
| | | | 02 | | | 100 | |
| | | | 03 | | | 80 | |
| | | | 04 | | | 65 | |
| | | | 05 | | | 50 | |
| Reset to $\overline{HF}$, $\overline{FF}$, and $\overline{FF-1}$ high | $t_{RSF2}$ | | 01 | 9,10,11 | | 140 | ns |
| | | | 02 | | | 100 | |
| | | | 03 | | | 80 | |
| | | | 04 | | | 65 | |
| | | | 05 | | | 50 | |
| RESET TO TIME DELAYED OUTPUTS - SERIAL MODE ONLY | | | | | | | |
| Reset going low to $Q_{0-8}$ low | $t_{RSQL}$ | $C_L$ = 30 pF, see figures 3 and 4 | 01 | 9,10,11 | 105 | | ns |
| | | | 02 | | 65 | | |
| | | | 03 | | 50 | | |
| | | | 04 | | 35 | | |
| | | | 05 | | 20 | | |
| Reset going high to $Q_{0-8}$ high | $t_{RSQH}$ | | 01 | 9,10,11 | 105 | | ns |
| | | | 02 | | 65 | | |
| | | | 03 | | 50 | | |
| | | | 04 | | 35 | | |
| | | | 05 | | 20 | | |
| Reset going low to $D_{0-8}$ low | $t_{RSDL}$ | | 01 | 9,10,11 | 105 | | ns |
| | | | 02 | | 65 | | |
| | | | 03 | | 50 | | |
| | | | 04 | | 35 | | |
| | | | 05 | | 20 | | |

See footnotes at end of table.



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TABLE I. Electrical performance characteristics - Continued.

| Test | Symbol | Conditions<br>$-55°C \le T_C \le +125°C$<br>$V_{SS}$ = 0 V, 4.5 V $\le V_{CC} <$ 5.5 V<br>unless otherwise specified | Device type | Group A subgroups | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| **RETRANSMIT TIMINGS** | | | | | | | |
| Retransmit cycle time | $t_{RTC}$ | $C_L$ = 30 pF, see figures 3 and 4 | 01 | 9,10,11 | 140 | | ns |
| | | | 02 | | 100 | | |
| | | | 03 | | 80 | | |
| | | | 04 | | 65 | | |
| | | | 05 | | 50 | | |
| Retransmit pulse width | $t_{RT}$ | | 01 | 9,10,11 | 120 | | ns |
| | | | 02 | | 80 | | |
| | | | 03 | | 65 | | |
| | | | 04 | | 50 | | |
| | | | 05 | | 40 | | |
| Retransmit setup time | $t_{RTS}$ | | 01 | 9,10,11 | 120 | | ns |
| | | | 02 | | 80 | | |
| | | | 03 | | 65 | | |
| | | | 04 | | 50 | | |
| | | | 05 | | 40 | | |
| Retransmit recovery time | $t_{RTR}$ | | 01,02 | 9,10,11 | 20 | | ns |
| | | | 03,04 | | 15 | | |
| | | | 05 | | 10 | | |
| **PARALLEL MODE FLAG PROPAGATION DELAYS** | | | | | | | |
| Read low to $\overline{EF}$ low | $t_{REF}$ | $C_L$ = 30 pF, see figures 3 and 4 | 01-03 | 9,10,11 | | 60 | ns |
| | | | 04 | | | 45 | |
| | | | 05 | | | 35 | |
| Read high to $\overline{FF}$ high | $t_{RFF}$ | | 01-03 | 9,10,11 | | 60 | ns |
| | | | 04 | | | 45 | |
| | | | 05 | | | 35 | |

See footnotes at end of table.



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TABLE I. Electrical performance characteristics - Continued.

| Test | Symbol | Conditions<br>$-55°C \le T_C \le +125°C$<br>$V_{SS}$ = 0 V, 4.5 V ≤ $V_{CC}$ < 5.5 V<br>unless otherwise specified | Device type | Group A subgroups | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| Read high to transitioning HF, AEF, and FF-1 | $t_{RF}$ | $C_L$ = 30 pF, see figures 3 and 4 | 01 | 9,10,11 | | 140 | ns |
| | | | 02 | | | 100 | |
| | | | 03 | | | 80 | |
| | | | 04 | | | 65 | |
| | | | 05 | | | 50 | |
| Read low to transitioning AEF and EF+1 | $t_{RE}$ | | 01 | 9,10,11 | | 140 | ns |
| | | | 02 | | | 100 | |
| | | | 03 | | | 80 | |
| | | | 04 | | | 65 | |
| | | | 05 | | | 45 | |
| Read pulse width after EF high | $t_{RPE}$ | | 01 | 9,10,11 | 120 | | ns |
| | | | 02 | | 80 | | |
| | | | 03 | | 65 | | |
| | | | 04 | | 50 | | |
| | | | 05 | | 40 | | |
| Write high to $\overline{EF}$ high | $t_{WEF}$ | | 01-03 | 9,10,11 | | 60 | ns |
| | | | 04 | | | 45 | |
| | | | 05 | | | 35 | |
| Write low to $\overline{FF}$ low | $t_{WFF}$ | | 01-03 | 9,10,11 | | 60 | ns |
| | | | 04 | | | 45 | |
| | | | 05 | | | 35 | |
| Write low to transitioning HF, AEF, and FF-1 | $t_{WF}$ | | 01 | 9,10,11 | | 140 | ns |
| | | | 02 | | | 100 | |
| | | | 03 | | | 80 | |
| | | | 04 | | | 65 | |
| | | | 05 | | | 50 | |

See footnotes at end of table.



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TABLE I. Electrical performance characteristics - Continued.

| Test | Symbol | Conditions<br>$-55°C \le T_C \le +125°C$<br>$V_{SS}$ = 0 V, 4.5 V $\le V_{CC} <$ 5.5 V<br>unless otherwise specified | Device type | Group A subgroups | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| Write high to transitioning AEF and EF+1 | $t_{WE}$ | $C_L$ = 30 pF, see figures 3 and 4 | 01 | 9,10,11 | | 140 | ns |
| | | | 02 | | | 100 | |
| | | | 03 | | | 80 | |
| | | | 04 | | | 65 | |
| | | | 05 | | | 50 | |
| Write pulse width after FF high | $t_{WPF}$ | | 01 | 9,10,11 | 120 | | ns |
| | | | 02 | | 80 | | |
| | | | 03 | | 65 | | |
| | | | 04 | | 50 | | |
| | | | 05 | | 40 | | |
| DEPTH EXPANSION MODE DELAYS | | | | | | | |
| Read/write to $\overline{XO}$ low | $t_{XOL}$ | $C_L$ = 30 pF, see figures 3 and 4 | 01 | 9,10,11 | | 120 | ns |
| | | | 02 | | | 80 | |
| | | | 03 | | | 65 | |
| | | | 04 | | | 50 | |
| | | | 05 | | | 40 | |
| Read/write to $\overline{XO}$ high | $t_{XOH}$ | | 01 | 9,10,11 | | 120 | ns |
| | | | 02 | | | 80 | |
| | | | 03 | | | 65 | |
| | | | 04 | | | 50 | |
| | | | 05 | | | 40 | |
| $\overline{XI}$ pulse width | $t_{XI}$ | | 01 | 9,10,11 | 120 | | ns |
| | | | 02 | | 80 | | |
| | | | 03 | | 65 | | |
| | | | 04 | | 50 | | |
| | | | 05 | | 40 | | |

See footnotes at end of table.



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TABLE I. Electrical performance characteristics - Continued.

| Test | Symbol | Conditions<br>$-55°C \le T_C \le +125°C$<br>$V_{SS}$ = 0 V, 4.5 V $\le V_{CC} <$ 5.5 V<br>unless otherwise specified | Device type | Group A subgroups | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| $\overline{XI}$ recovery time | $t_{XIR}$ | $C_L$ = 30 pF, see figures 3 and 4 | All | 9,10,11 | 10 | | ns |
| $\overline{XI}$ setup time | $t_{XIS}$ | | All | 9,10,11 | 15 | | ns |
| SERIAL INPUT MODE TIMINGS | | | | | | | |
| Serial data in setup time to SICP rising edge | $t_{S2}$ | $C_L$ = 30 pF, see figures 3 and 4 | 01,02 | 9,10,11 | 20 | | ns |
| | | | 03,04 | | 15 | | |
| | | | 05 | | 12 | | |
| Serial data in hold time from SICP rising edge | $t_{H2}$ | | 01,02 | 9,10,11 | 5.0 | | ns |
| | | | 03-05 | | 0 | | |
| SIX setup time to SICP rising edge | $t_{S3}$ | | All | 9,10,11 | 5.0 | | ns |
| $\overline{W}$ setup time to SICP rising edge | $t_{S4}$ | | All | 9,10,11 | 5.0 | | ns |
| $\overline{W}$ hold time to SICP rising edge | $t_{H4}$ | | 01 | 9,10,11 | 15 | | ns |
| | | | 02 | | 12 | | |
| | | | 03 | | 10 | | |
| | | | 04,05 | | 7.0 | | |
| Serial in clock width high/low | $t_{SICW}$ | | 01,02 | 9,10,11 | 15 | | ns |
| | | | 03,04 | | 10 | | |
| | | | 05 | | 8 | | |
| $\overline{SI/PI}$ setup time to SICP rising edge | $t_{S5}$ | | 01 | 9,10,11 | 120 | | ns |
| | | | 02 | | 80 | | |
| | | | 03 | | 65 | | |
| | | | 04 | | 50 | | |
| | | | 05 | | 40 | | |

See footnotes at end of table.



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TABLE I. Electrical performance characteristics - Continued.

| Test | Symbol | Conditions<br>$-55°C \le T_C \le +125°C$<br>$V_{SS}$ = 0 V, 4.5 V $\le V_{CC} <$ 5.5 V<br>unless otherwise specified | Device type | Group A subgroups | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| **SERIAL OUTPUT MODE TIMINGS** | | | | | | | |
| $\overline{SO}$/PO setup time to SOCP rising edge | $t_{S6}$ | $C_L$ = 30 pF, see figures 3 and 4 | 01 | 9,10,11 | 120 | | ns |
| | | | 02 | | 80 | | |
| | | | 03 | | 65 | | |
| | | | 04 | | 50 | | |
| | | | 05 | | 40 | | |
| SOX setup time to SOCP rising edge | $t_{S7}$ | | All | 9,10,11 | 5.0 | | ns |
| $\overline{R}$ setup time to SOCP rising edge | $t_{S8}$ | | All | 9,10,11 | 5.0 | | ns |
| $\overline{R}$ hold time to SOCP rising edge | $t_{H8}$ | | 01 | 9,10,11 | 15 | | ns |
| | | | 02 | | 12 | | |
| | | | 03 | | 10 | | |
| | | | 04,05 | | 7.0 | | |
| Serial in clock width high/low | $t_{SOCW}$ | | 01,02 | 9,10,11 | 15 | | ns |
| | | | 03,04 | | 10 | | |
| | | | 05 | | 8 | | |
| **SERIAL MODE RECOVERY TIMINGS** | | | | | | | |
| Recovery time SOCP after EF goes high | $t_{REFSO}$ | $C_L$ = 30 pF, see figures 3 and 4 | 01 | 9,10,11 | 120 | | ns |
| | | | 02 | | 80 | | |
| | | | 03 | | 65 | | |
| | | | 04 | | 50 | | |
| | | | 05 | | 40 | | |
| Recovery time SICP after FF goes high | $t_{RFFSI}$ | | 01,02 | 9,10,11 | 20 | | ns |
| | | | 03-05 | | 15 | | |

See footnotes at end of table.



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TABLE I. Electrical performance characteristics - Continued.

| Test | Symbol | Conditions<br>$-55°C \le T_C \le +125°C$<br>$V_{SS}$ = 0 V, 4.5 V $\le V_{CC} <$ 5.5 V<br>unless otherwise specified | Device type | Group A subgroups | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| SERIAL MODE FLAG PROPAGATION DELAYS | | | | | | | |
| SOCP rising edge (bit 0 - first word) to EF low | $t_{SOCEF}$ | $C_L$ = 30 pF, see figures 3 and 4 | 01-03 | 9,10,11 | | 30 | ns |
| | | | 04,05 | | | 25 | |
| SOCP rising edge (bit 0 - first word) to FF high | $t_{SOCFF}$ | | 01,02 | 9,10,11 | | 60 | ns |
| | | | 03 | | | 50 | |
| | | | 04 | | | 40 | |
| | | | 05 | | | 35 | |
| SOCP rising edge (bit 0 - second word) to FF-1, HF, AEF, EF+1 high | $t_{SOCF}$ | | 01,02 | 9,10,11 | | 60 | ns |
| | | | 03 | | | 50 | |
| | | | 04 | | | 40 | |
| | | | 05 | | | 35 | |
| SICP rising edge (bit 0 - first word) to EF high | $t_{SICEF}$ | | 01-03 | 9,10,11 | | 80 | ns |
| | | | 04 | | | 65 | |
| | | | 05 | | | 50 | |
| SICP rising edge (bit 0 - first word) to FF low | $t_{SICFF}$ | | 01,02 | 9,10,11 | | 60 | ns |
| | | | 03 | | | 50 | |
| | | | 04 | | | 40 | |
| | | | 05 | | | 35 | |
| SICP rising edge (bit 0 - second word) to EF+1, HF, AEF, FF-1 high | $t_{SICF}$ | | 01-03 | 9,10,11 | | 80 | ns |
| | | | 04 | | | 65 | |
| | | | 05 | | | 50 | |
| SERIAL INPUT MODE DELAYS | | | | | | | |
| SICP rising edge to D 2/ | $t_{PD1}$ | $C_L$ = 30 pF, see figures 3 and 4 | 01 | 9,10,11 | 5.0 | 35 | ns |
| | | | 02 | | 5.0 | 30 | |
| | | | 03 | | 5.0 | 25 | |
| | | | 04 | | 5.0 | 20 | |
| | | | 05 | | 5.0 | 17 | |

See footnotes at end of table.



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TABLE I. Electrical performance characteristics - Continued.

| Test | Symbol | Conditions $-55°C \le T_C \le +125°C$, $V_{SS}$ = 0 V, $4.5 V \le V_{CC} < 5.5$ V unless otherwise specified | Device type | Group A subgroups | Limits Min | Limits Max | Unit |
|---|---|---|---|---|---|---|---|
| SERIAL OUTPUT MODE DELAYS | | | | | | | |
| SOCP rising edge to Q 2/ | $t_{PD2}$ | $C_L$ = 30 pF, see figures 3 and 4 | 01,02 | 9,10,11 | 5.0 | 30 | ns |
| | | | 03 | | 5.0 | 25 | |
| | | | 04 | | 5.0 | 20 | |
| | | | 05 | | 5.0 | 17 | |
| SOCP rising edge to SO at high-Z 2/ | $t_{SOHZ}$ | | 01 | 9,10,11 | 5.0 | 30 | ns |
| | | | 02 | | 5.0 | 25 | |
| | | | 03 | | 5.0 | 20 | |
| | | | 04,05 | | 5.0 | 16 | |
| SOCP rising edge to SO at low-Z 2/ | $t_{SOLZ}$ | | 01 | 9,10,11 | 5.0 | 35 | ns |
| | | | 02 | | 5.0 | 30 | |
| | | | 03-05 | | 5.0 | 22 | |
| SOCP rising edge to valid data on SO | $t_{SOPD}$ | | 01 | 9,10,11 | | 35 | ns |
| | | | 02 | | | 30 | |
| | | | 03 | | | 22 | |
| | | | 04,05 | | | 18 | |
| OUTPUT ENABLE/DISABLE DELAYS | | | | | | | |
| Output enable to high-Z (disable) 2/ | $t_{OEHZ}$ | $C_L$ = 30 pF, see figures 3 and 4 | 01 | 9,10,11 | | 30 | ns |
| | | | 02 | | | 25 | |
| | | | 03 | | | 20 | |
| | | | 04,05 | | | 16 | |
| Output enable to low-Z (enable) 2/ | $t_{OELZ}$ | | All | 9,10,11 | 5.0 | | ns |
| Output enable to data valid ($Q_{0-8}$) | $t_{AOE}$ | | 01 | 9,10,11 | | 35 | ns |
| | | | 02 | | | 30 | |
| | | | 03 | | | 25 | |
| | | | 04 | | | 22 | |
| | | | 05 | | | 20 | |

1/ Shall be tested initially and after any design or process changes which may affect this parameter, and therefore shall be guaranteed to the limits specified in table I.
2/ May not be tested, but shall be guaranteed to the limits specified in table I.



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| Device types | All | |
|---|---|---|
| Case outlines | Q | X |
| Terminal number | Terminal symbol | |
| 1 | $\overline{SO}$ | $\overline{W}$ |
| 2 | $\overline{AEF}$ | $D_4$ |
| 3 | $\overline{FF}$-1 | $D_3$ |
| 4 | FF | $D_2$ |
| 5 | $Q_0$ | $D_1$ |
| 6 | $Q_1$ | GND |
| 7 | $Q_2$ | $D_0$ |
| 8 | $Q_3$ | $\overline{XI}$ |
| 9 | $Q_4$ | SO/PO |
| 10 | $\overline{GND}$ | SOX |
| 11 | $\overline{R}$ | SOCP |
| 12 | $Q_5$ | $\overline{SO}$ |
| 13 | $Q_6$ | $\overline{AEF}$ |
| 14 | $Q_7$ | $\overline{FF}$-1 |
| 15 | $Q_8$ | FF |
| 16 | $\overline{XO}/\overline{HF}$ | $Q_0$ |
| 17 | $\overline{EF}$ | GND |
| 18 | $\overline{EF}$+1 | $Q_1$ |
| 19 | $\overline{OE}$ | $Q_2$ |
| 20 | SI/PI | $Q_3$ |
| 21 | SIX | $Q_4$ |
| 22 | SICP | $\overline{GND}$ |
| 23 | $\overline{SI}$ | $\overline{R}$ |
| 24 | $\overline{RS}$ | $Q_5$ |
| 25 | FL/RT | $Q_6$ |
| 26 | $D_8$ | $Q_7$ |
| 27 | $D_7$ | $Q_8$ |
| 28 | $D_6$ | $\overline{GND}$ |
| 29 | $D_5$ | $\overline{XO}/\overline{HF}$ |
| 30 | $V_{CC}$ | $\overline{EF}$ |
| 31 | $\overline{W}$ | $\overline{EF}$+1 |
| 32 | $D_4$ | $\overline{OE}$ |
| 33 | $D_3$ | SI/PI |
| 34 | $D_2$ | SIX |
| 35 | $D_1$ | SICP |
| 36 | $D_0$ | SI |
| 37 | $\overline{XI}$ | $\overline{RS}$ |
| 38 | SO/PO | FL/RT |
| 39 | SOX | GND |
| 40 | SOCP | $D_8$ |
| 41 | --- | $D_7$ |
| 42 | --- | $D_6$ |
| 43 | --- | $D_5$ |
| 44 | --- | $V_{CC}$ |

FIGURE 1. Terminal connections.



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Reset and retransmit
Single device configuration/width expansion mode

| Mode | Inputs | | | Internal status | | Outputs | | |
|---|---|---|---|---|---|---|---|---|
| | $\overline{RS}$ | $\overline{FL}$ | $\overline{XI}$ | Read pointer | Write pointer | $\overline{AEF}$, $\overline{EF}$, $\overline{EF+1}$ | $\overline{FF}$, $\overline{FF-1}$ | $\overline{HF}$ |
| Reset | 0 | X | 0 | Location zero | Location zero | 0 | 1 | 1 |
| Retransmit | 1 | 0 | 0 | Location zero | Unchanged | X | X | X |
| Read/Write | 1 | 1 | 0 | Increment 1/ | Increment 1/ | X | X | X |

1/ Pointer will increment if flag is high.

Reset and first load
Depth expansion/compound expansion mode

| Mode | Inputs | | | Internal status | | Outputs | |
|---|---|---|---|---|---|---|---|
| | $\overline{RS}$ | $\overline{FL}$ | $\overline{XI}$ | Read pointer | Write pointer | $\overline{EF}$ | $\overline{FF}$ |
| Reset first device | 0 | 0 | 1/ | Location zero | Location zero | 0 | 1 |
| Reset all other devices | 0 | 1 | 1/ | Location zero | Location zero | 0 | 1 |
| Read/Write | 1 | X | 1/ | X | X | X | X |

1/ $\overline{XI}$ is connected to $\overline{XO}$ of previous device.

NOTE: $\overline{RS}$ = Reset input, $\overline{FL}/\overline{RT}$ = First load/retransmit, $\overline{EF}$ = Empty flag output, $\overline{FF}$ = Full flag output, XI = Expansion input, and HF = Half-full flag output
0 = Low level voltage
1 = High level voltage
X = Don't care

FIGURE 2. Truth tables.



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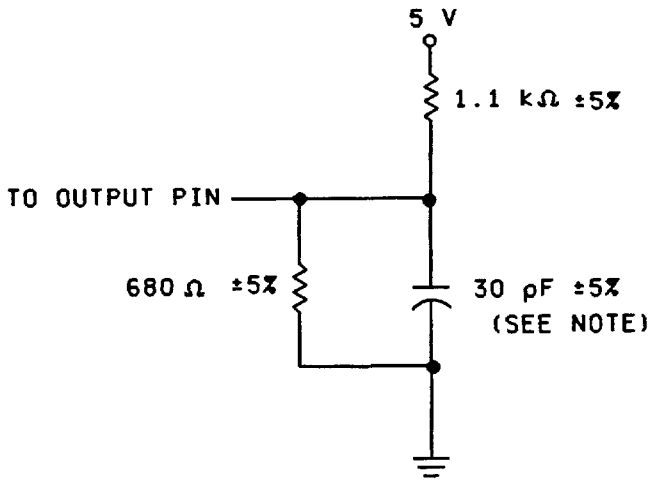


NOTE: $C_L$ includes scope and jig capacitance.

AC test conditions

| | |
|---|---|
| Input pulse levels | GND to 3.0 V |
| Input rise and fall times | 3.0 ns |
| Input timing reference levels | 1.5 V |
| Output reference levels | 1.5 V |

FIGURE 3. Output load circuit and ac test conditions.



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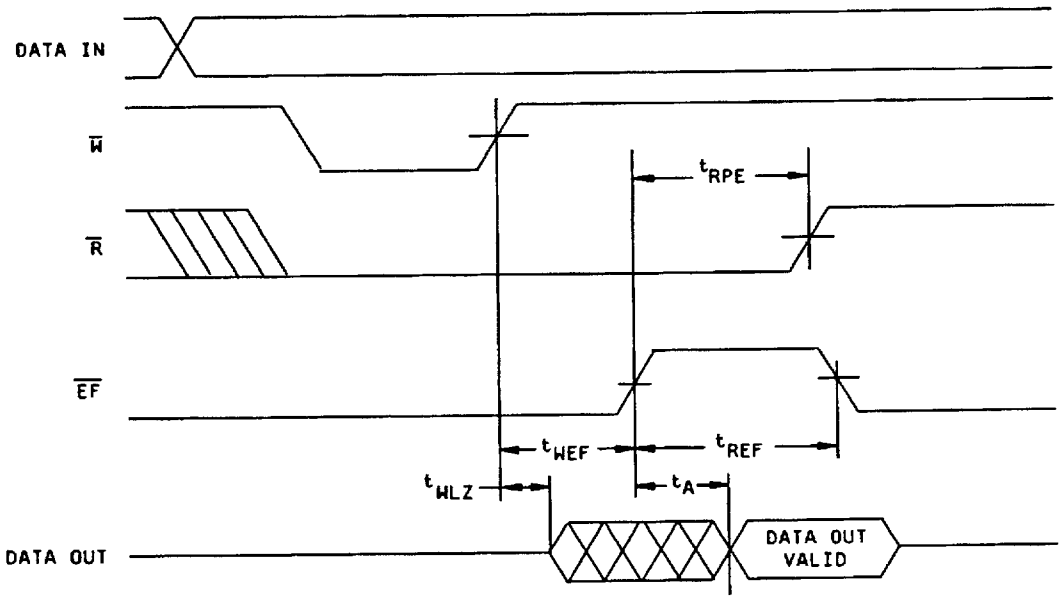
FIFO EMPTY BOUNDARY CONDITION TIMING




FIFO FULL BOUNDARY CONDITION TIMING

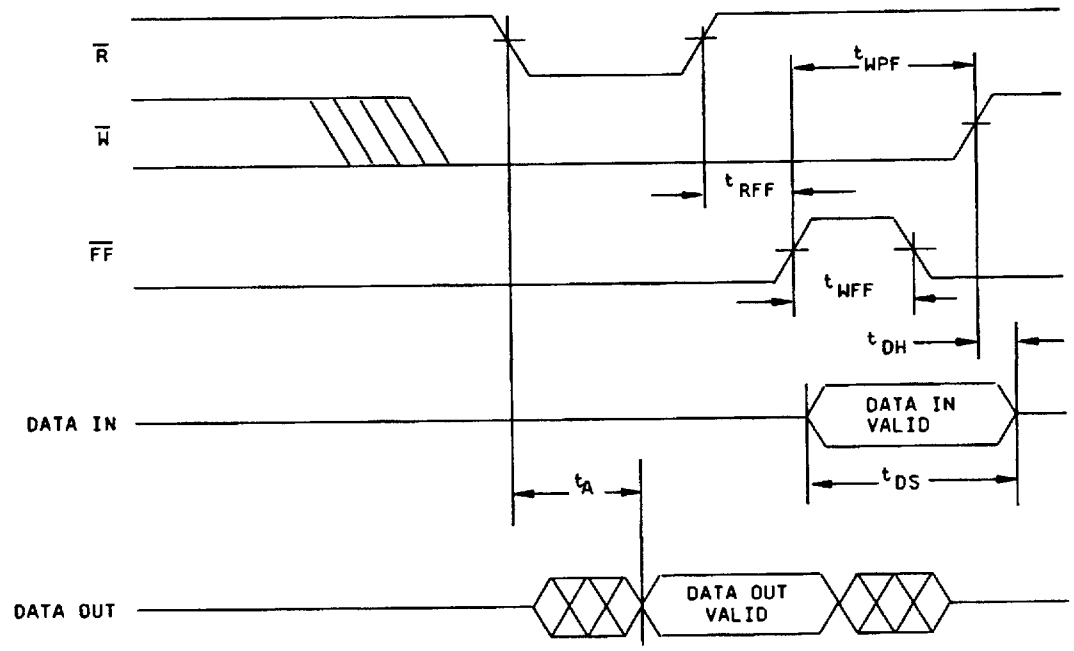



FIGURE 4. Timing waveforms.



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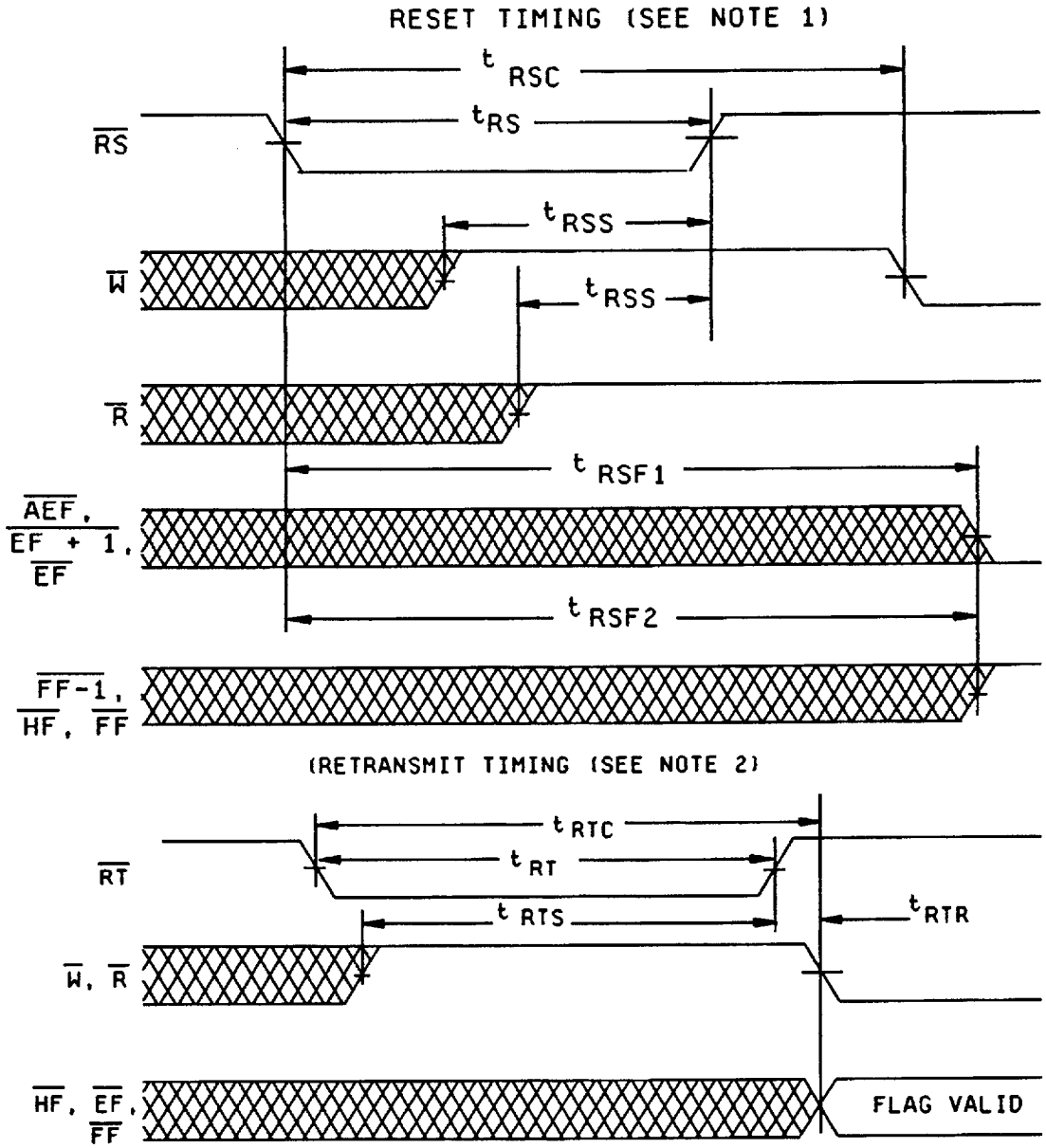


FIGURE 4. Timing waveforms - Continued.



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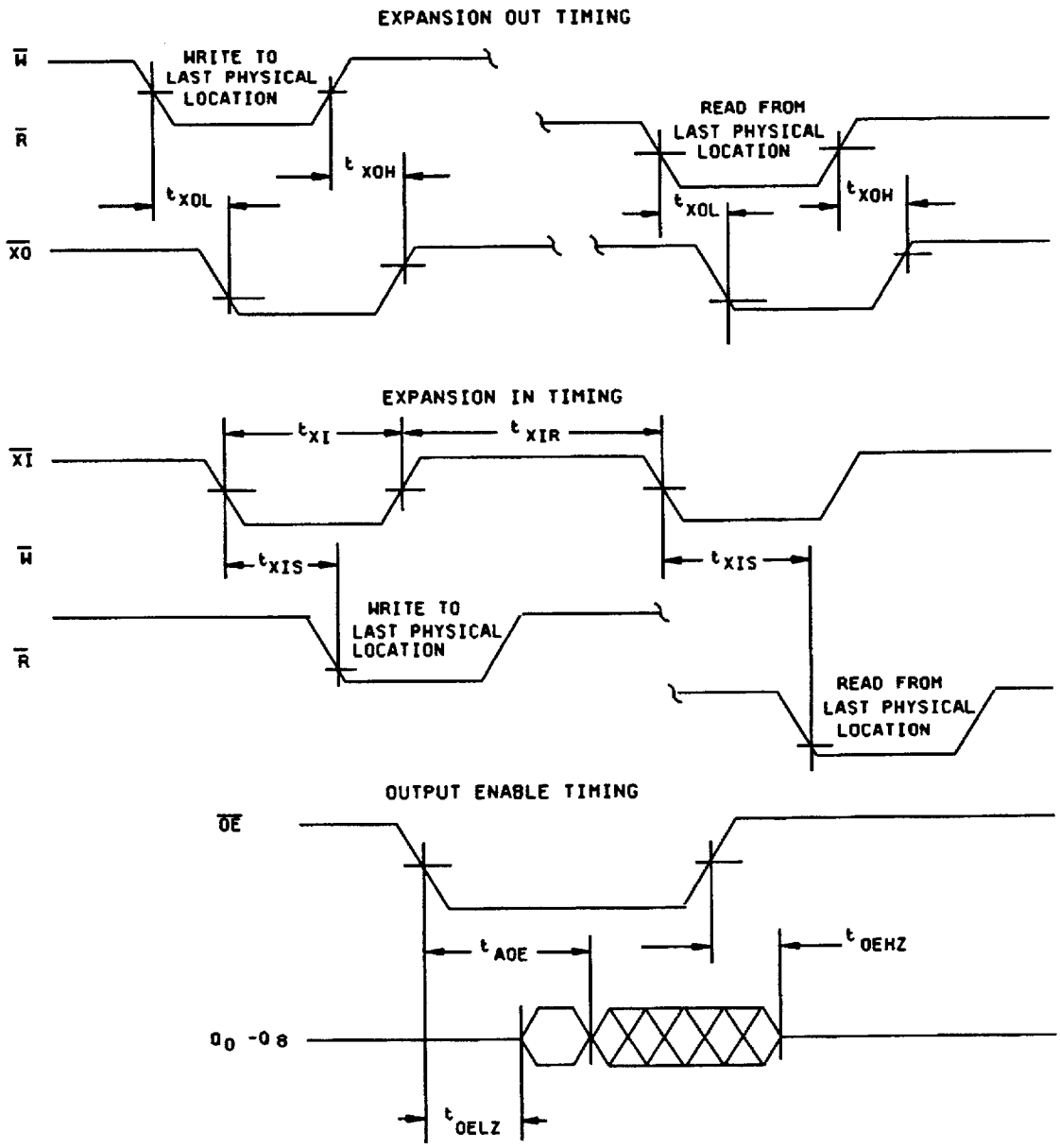


FIGURE 4. Timing waveforms - Continued.

| | | | |
|---|---|---|---|
| STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444 | SIZE A | | 5962-89943 |
| | | REVISION LEVEL A | SHEET 21 |

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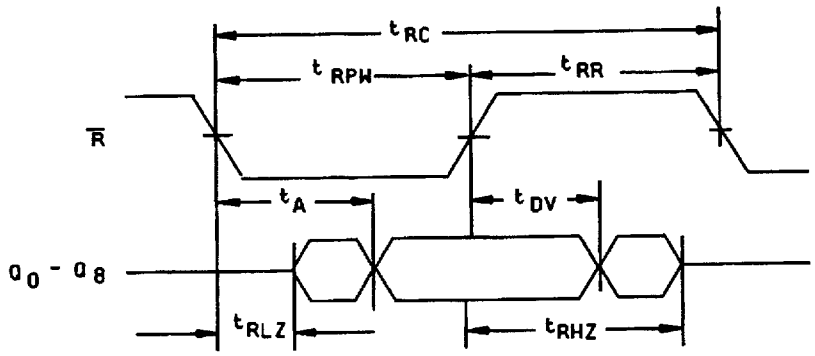
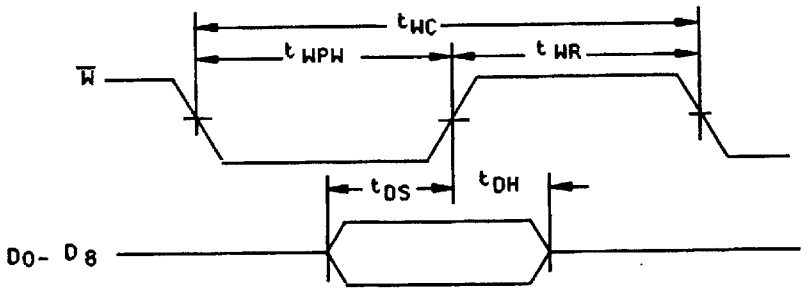
READ OPERATION IN PARALLEL DATA OUT MODE




WRITE OPERATION IN PARALLEL DATA IN MODE




EMPTY FLAG TIMING IN PARALLEL-OUT MODE

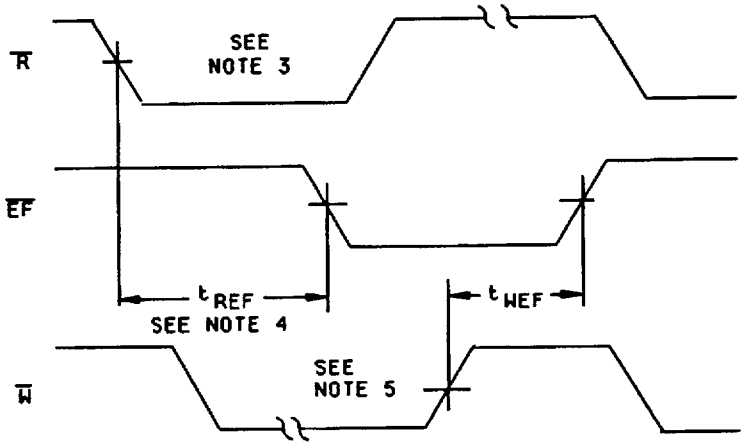



FIGURE 4. Timing waveforms - Continued.

| STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444 | SIZE A | | 5962-89943 |
|---|---|---|---|
| | | REVISION LEVEL A | SHEET 22 |

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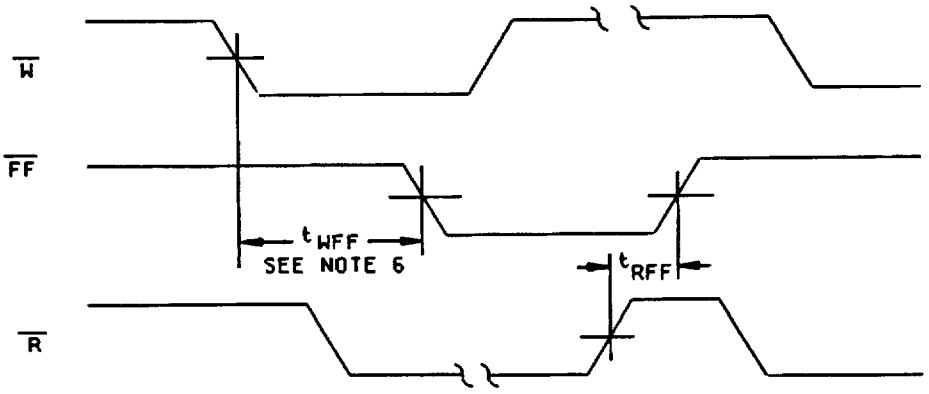
FULL FLAG TIMING IN PARALLEL-IN MODE




ALMOST-FULL, HALF-FULL, AND FULL-1 FLAG TIMING

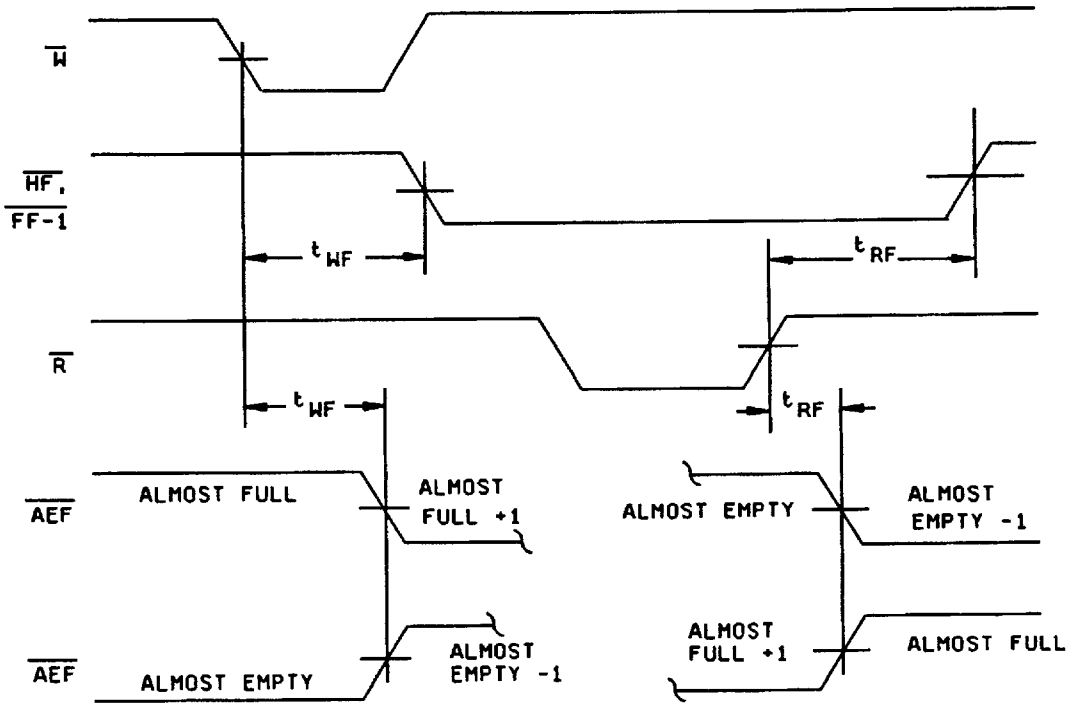



FIGURE 4. Timing waveforms - Continued.



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EMPTY +1 FLAG TIMINGS

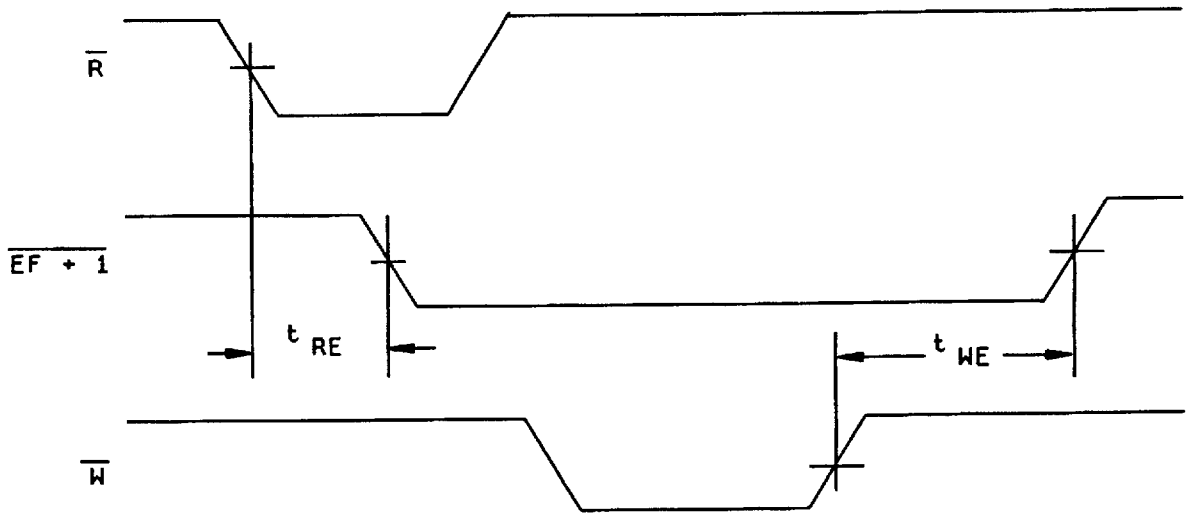


FIGURE 4. Timing waveforms - Continued.



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READ OPERATIONS IN SERIAL-OUT MODE

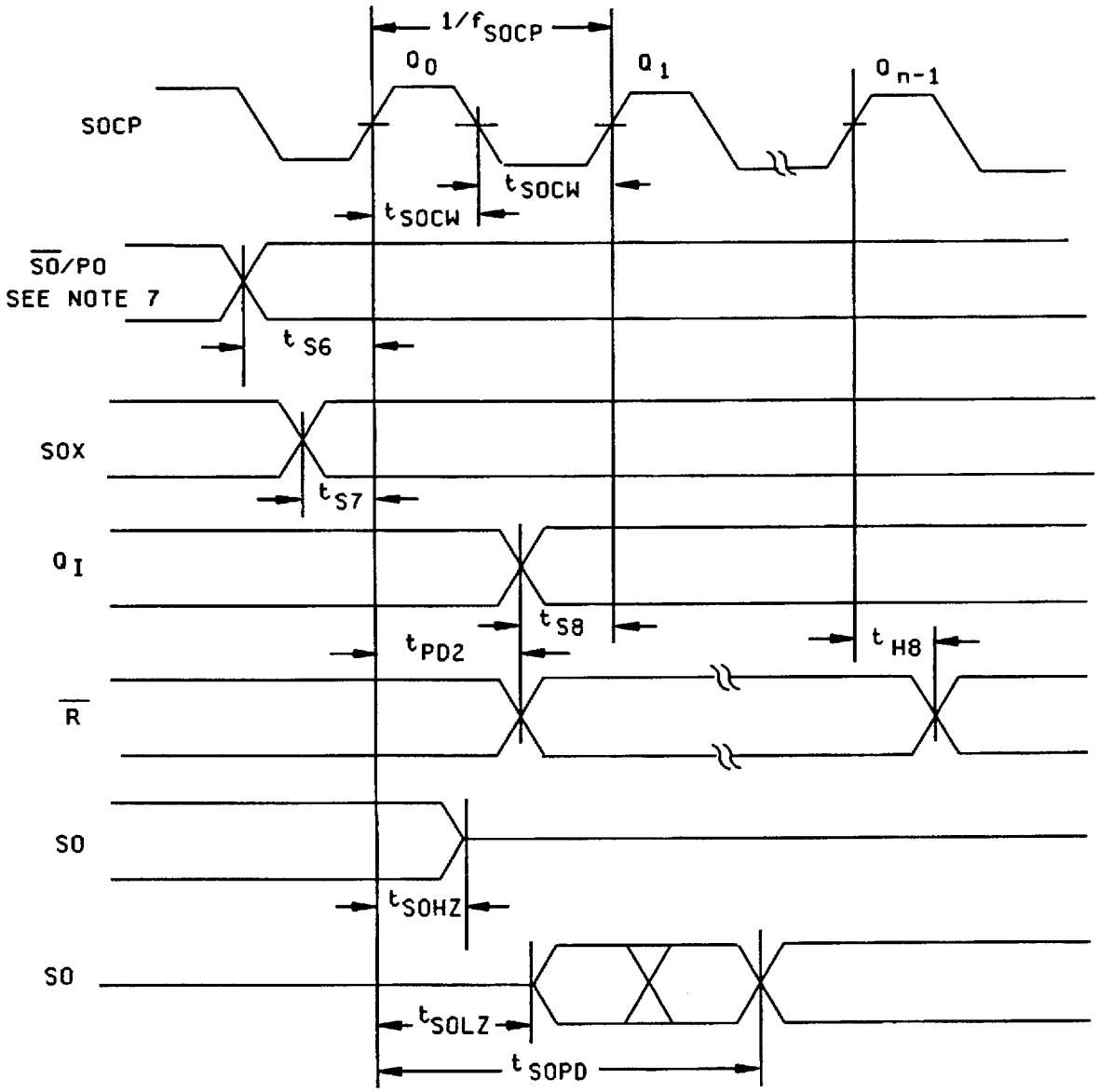


FIGURE 4. Timing waveforms - Continued.

| STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444 | SIZE A | | 5962-89943 |
|---|---|---|---|
| | | REVISION LEVEL A | SHEET 25 |

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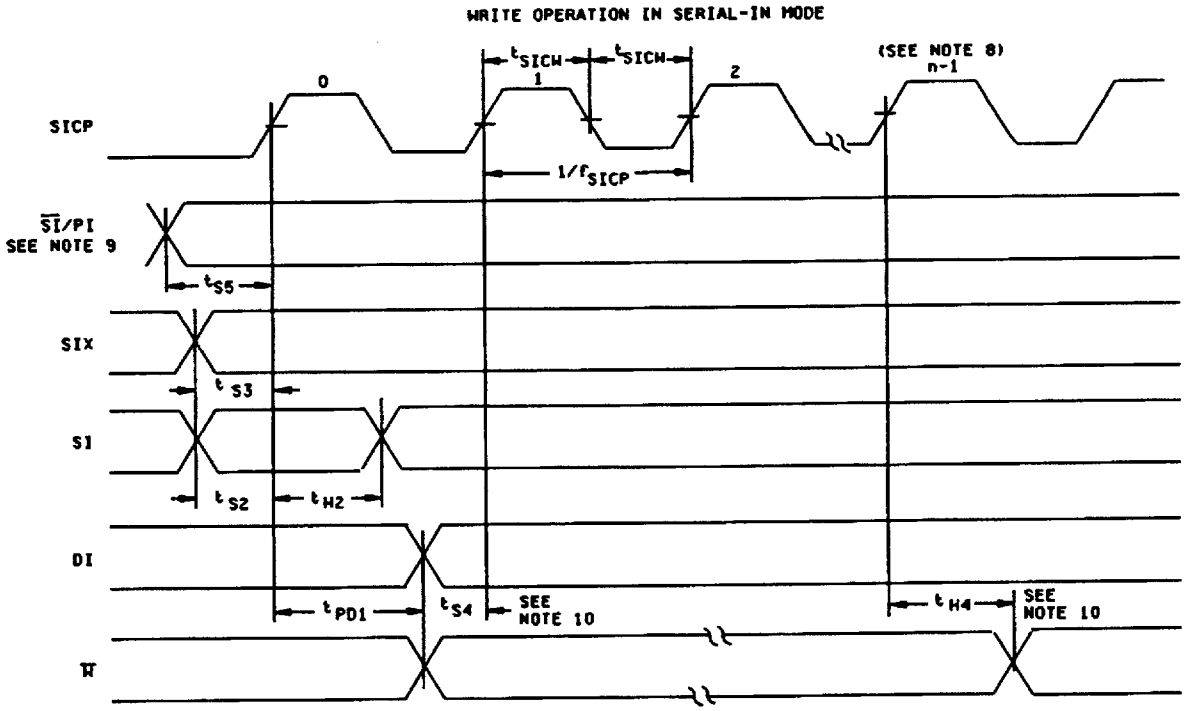


FIGURE 4. Timing waveforms - Continued.



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FULL FLAG AND FULL-1 FLAG DEASSERTION IN SERIAL-OUT MODE

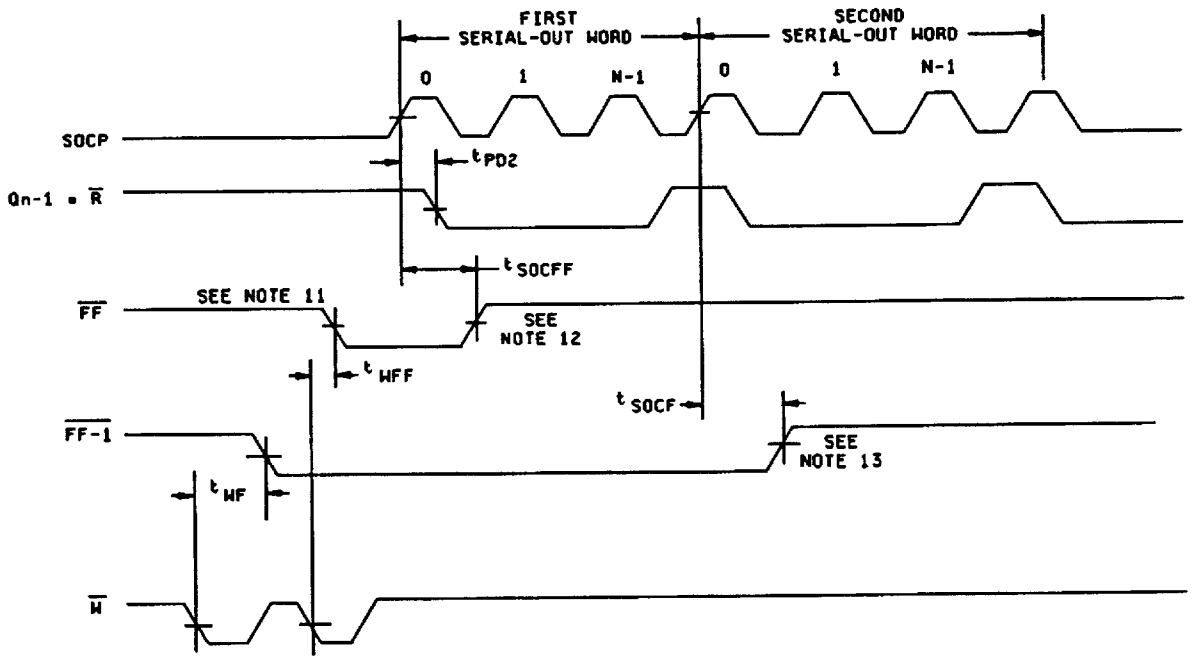


FIGURE 4. Timing waveforms - Continued.

| STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444 | SIZE A | | 5962-89943 |
|---|---|---|---|
| | | REVISION LEVEL A | SHEET 27 |

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EMPTY FLAG AND EMPTY + 1 FLAG ASSERTATION IN THE SERIAL MODE.

FIFO BEING EMPTIED

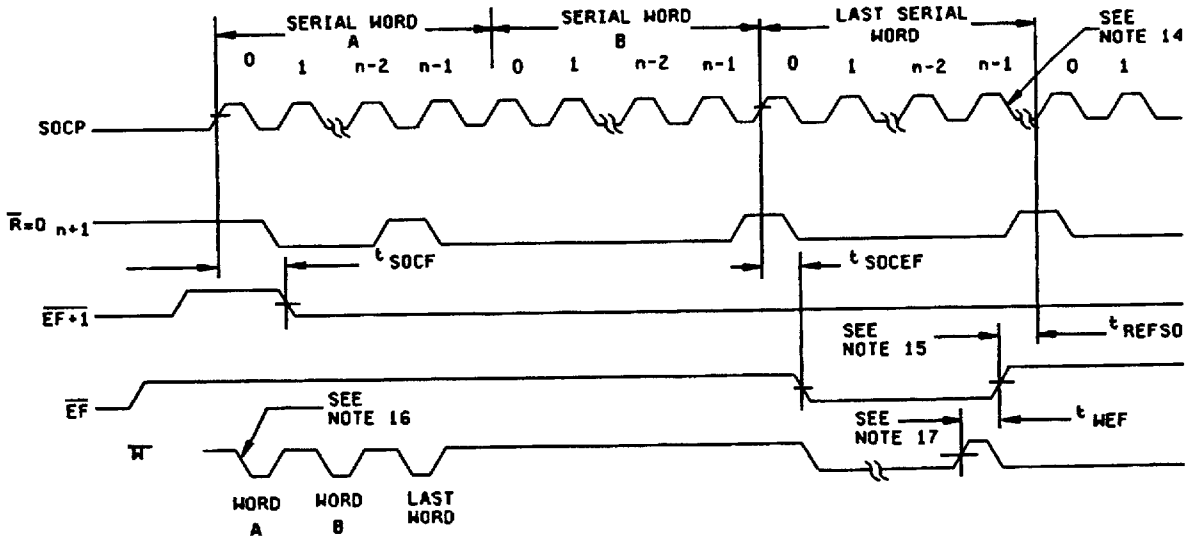


FIGURE 4. Timing waveforms - Continued.



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Full flag and full - 1 flag assertion in the serial-in mode,
FIFO being filled

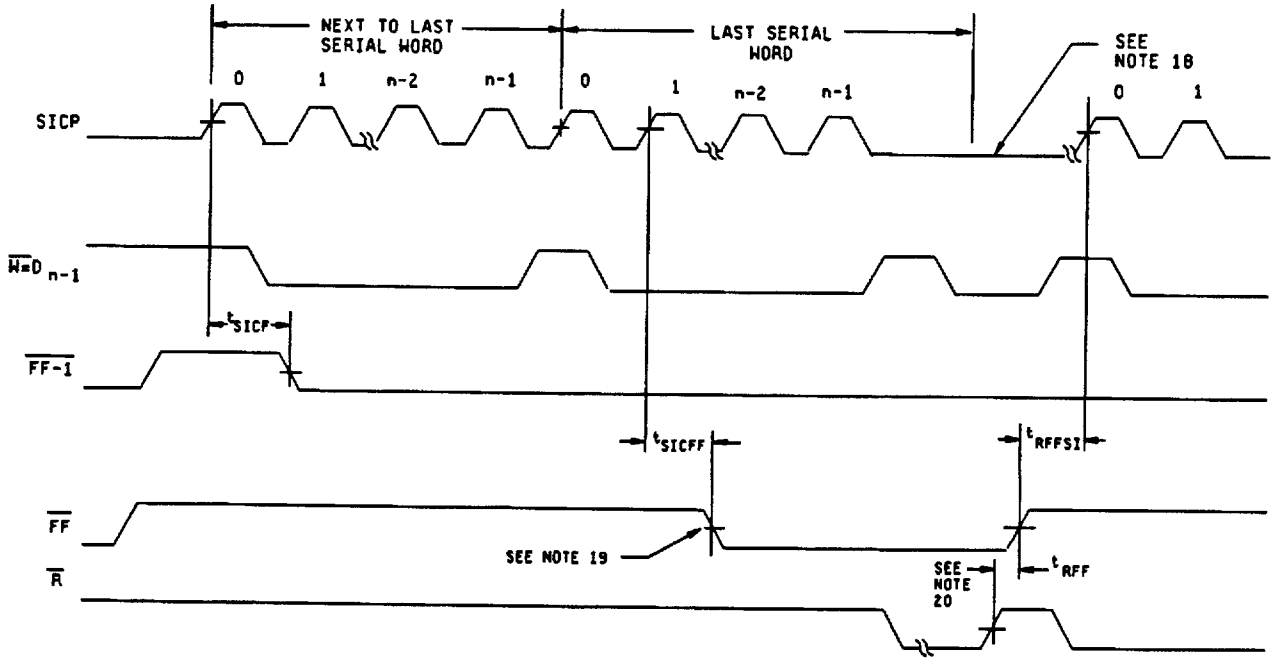


FIGURE 4. Timing waveforms - Continued.

| STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444 | SIZE A | | 5962-89943 |
|---|---|---|---|
| | | REVISION LEVEL A | SHEET 29 |

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EMPTY FLAG AND EMPTY+1 FLAG DEASSERTION IN SERIAL-IN MODE

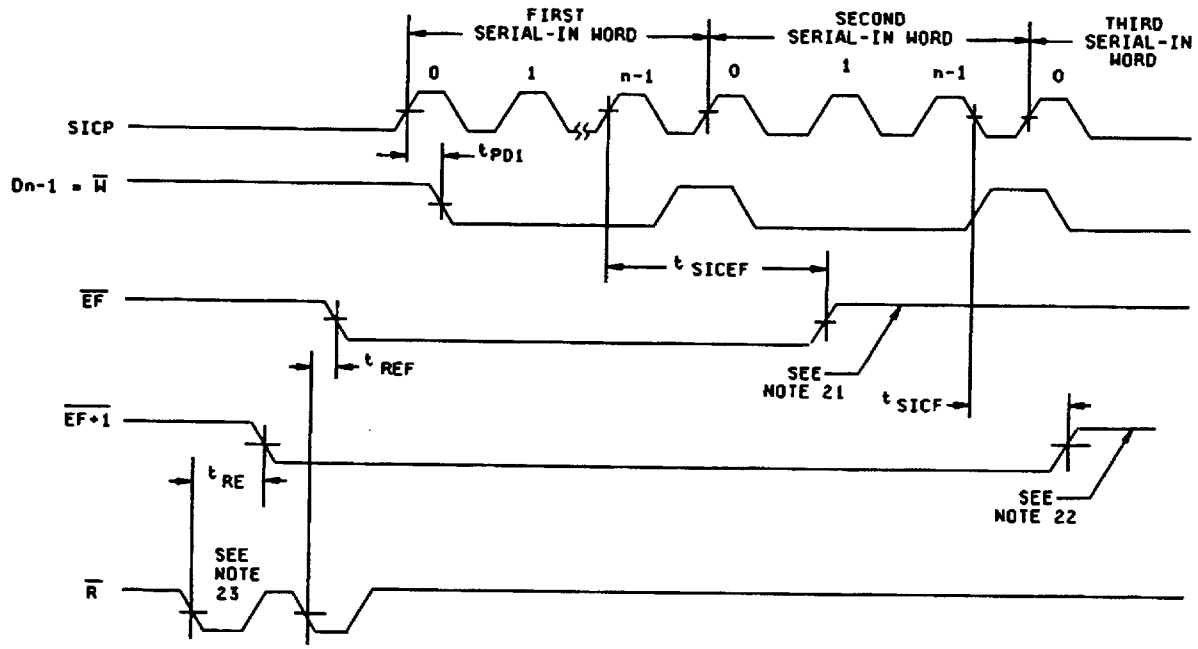


FIGURE 4. Timing waveforms - Continued.



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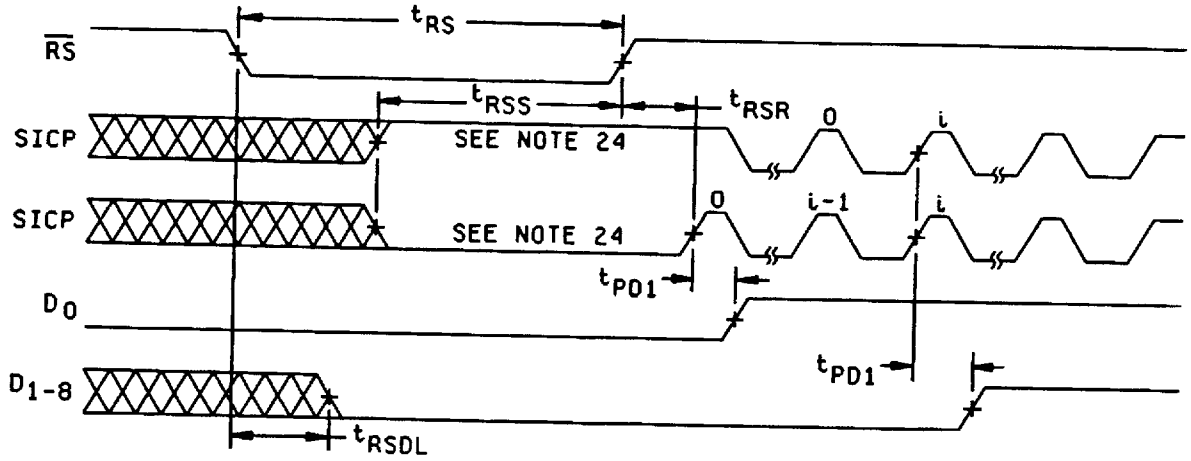
Reset timing for serial-in mode




Reset timing for serial-out mode

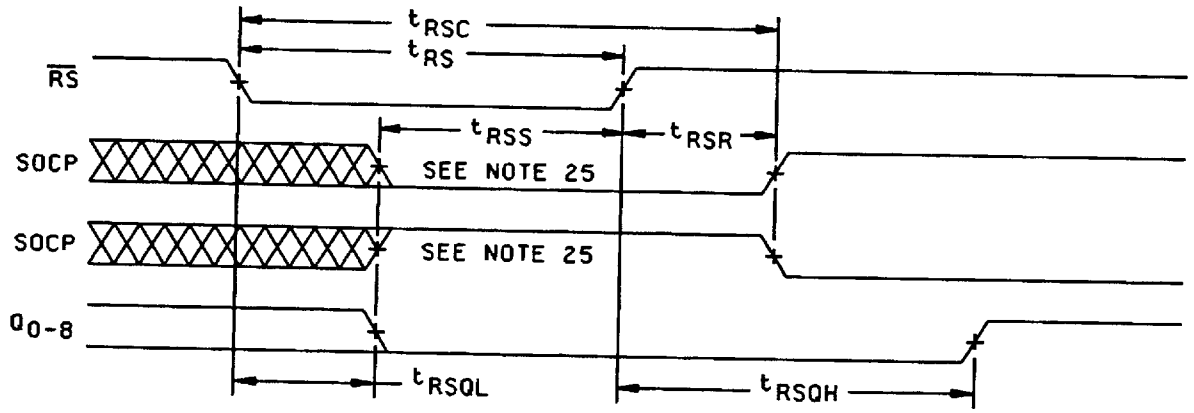



FIGURE 4. Timing waveforms - Continued.



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NOTES:
1. $\overline{EF}$, $\overline{FF}$ and $\overline{HF}$ may change status during reset, but flags will be valid at $t_{RSC}$.
2. EF, FF and HF, AEF, FF-1, and EF+1 may change status during retransmit, but flags will be valid at $t_{RTC}$.
3. Data is valid on this edge.
4. The empty flag is asserted by $\overline{R}$ in the parallel-out mode and is specified by $t_{REF}$. The $\overline{EF}$ flag is deasserted by the rising edge of W.
5. First rising edge of write after $\overline{EF}$ is set.
6. For the assertion time, $t_{WFF}$ is used when data is written in the parallel mode. The $\overline{FF}$ is deasserted by the rising edge of R.
7. After SO/PO has been setup, it cannot be dynamically changed; it can only be changed after a reset operation.
8. For the stand alone mode, $n \geq 4$ and the input bits are numbered 0 to n-1.
9. After SI/PI has been setup, it cannot be dynamically changed; it can only be changed after a reset operation.
10. For the recommended interconnections, $D_I$ is to be directly tied to W and the $t_{S4}$ and $t_{H4}$ requirements will be satisfied. For users that modify W externally, $t_{S4}$ and $t_{H4}$ have to be met.
11. The FIFO is full and a new read sequence is starting.
12. On the first rising edge of SOCP, the FF is deasserted. In the serial-in mode, a new write operation can begin after $t_{RFFS1}$ after FF goes HIGH. In the parallel-in mode, a new write operation can occur immediately after FF flag goes HIGH.
13. The FF-1 flag is deasserted after the first SOCP of the second serial word.
14. SOCP should not be clocked until EF goes HIGH.
15. The empty flag is asserted in the serial-out mode by using the $t_{SOCEF}$ parameter. This parameter is measured in the worst case from the rising edge of the SOCP used to clock data bit 0. Whenever EF goes LOW, there is only one word to be shifted out. In the parallel-in mode, the EF flag is deasserted by the rising edge of W. In the serial-in mode, the EF flag is deasserted by the rising edge of W.
16. Parallel write shown for reference only. Can also use serial input mode.
17. First write rising edge after EF is set.
18. SICP should not be clocked until FF goes HIGH.
19. The full flag is asserted in the serial-in mode by using the $t_{SICFF}$ parameter. This parameter is measured in the worst case from the rising edge of SICP followed by a $(t_{PD1} + t_{WFF})$ delay from the first rising edge of SICP of the last word.
20. First read rising edge after $\overline{FF}$ is set.
21. The empty flag is deasserted when an entire word has been loaded into the internal RAM. It can occur after the first rising edge of SICP of the second serial-in word. In the serial-out mode, a new read operation can begin $t_{REFSO}$ after EF goes HIGH. In the parallel-out mode, a new read operation can occur immediately after FF goes HIGH.
22. The $\overline{EF+1}$ flag is deasserted after the N-1 rising edge of SICP of the third serial-in word.
23. Parallel read shown for reference only. Can also use serial output mode.
24. SICP should be steady low or high during $t_{RSS}$. The first low to high or high to low transition can begin after $t_{RSR}$.
25. SOCP should be steady low or high during $t_{RSS}$. The first low to high or high to low transition can begin after $t_{RSR}$.

FIGURE 4. Timing waveforms - Continued.



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TABLE II. Electrical test requirements.

| MIL-STD-883 test requirements | Subgroups (per method 5005, table I) |
|---|---|
| Interim electrical parameters (method 5004) | --- |
| Final electrical test parameters (method 5004) | 1*,2,3,7*,8A, 8B,9,10,11 |
| Group A test requirements (method 5005) | 1,2,3,4**,7,8A, 8B,9,10,11 |
| Groups C and D end-point electrical parameters (method 5005) | 2,3,7,8A,8B |

* PDA applies to subgroups 1 and 7.
** See 4.3.1c

3.8 Notification of change. Notification of change to DESC-EC shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) $T_A$ = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.



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c. Subgroup 4 ($C_{IN}$ and $C_{OUT}$ measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance.

d. Subgroups 7 and 8 shall include verification of the truth table.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2) $T_A$ = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-STD-883 (see 3.1 herein).

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.5 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444-5270, or telephone (513) 296-5377.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.



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