674219

FIFO RAM Controller
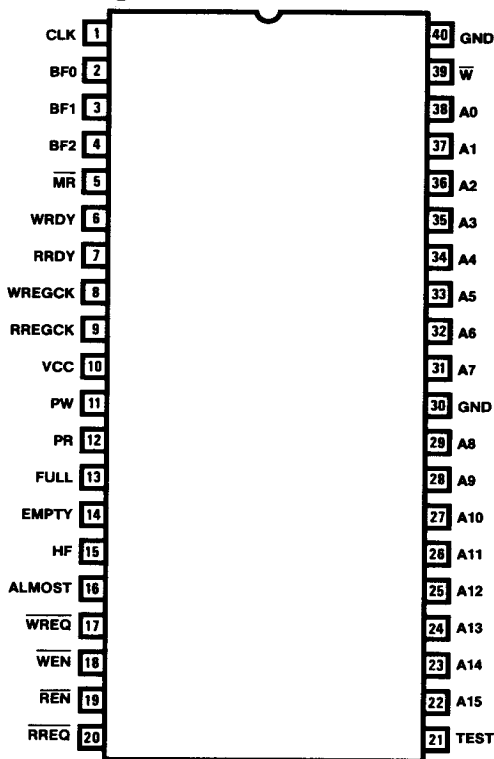
Advanced
Micro
Devices

Features/Benefits

- High-speed, no fall-through time
- Deep FIFOs—16-bit SRAM address
- Arbitration read/write
- Control signals for data latching
- Full, Half-Full, Empty, Almost flags for buffer sizes from 512 to 64 K
- Three-state outputs

Applications

- LAN equipment
- Data communication
- Disk/tape controllers
- Host-to-dedicated-processor interface

Pin Configuration

Pin	Signal		Pin	Signal
1	CLK		40	GND
2	BF0		39	$\overline{W}$
3	BF1		38	A0
4	BF2		37	A1
5	$\overline{MR}$		36	A2
6	WRDY		35	A3
7	RRDY		34	A4
8	WREGCK		33	A5
9	RREGCK		32	A6
10	VCC		31	A7
11	PW		30	GND
12	PR		29	A8
13	FULL		28	A9
14	EMPTY		27	A10
15	HF		26	A11
16	ALMOST		25	A12
17	$\overline{WREQ}$		24	A13
18	$\overline{WEN}$		23	A14
19	$\overline{REN}$		22	A15
20	$\overline{RREQ}$		21	TEST

Ordering Information

Part Number	Package		Temperature
	Pins	Type	
674219	40	CD 040	Com

Description

The 674219 FIFO RAM Controller provides addressing control, status, and arbitration for a static RAM array used as a First-In-First-Out (FIFO) buffer. The sixteen address lines can address a FIFO buffer area ranging from 512 to 65,536 static RAM words. Control signals including W (the write enable signal for the static RAMs), handshaking signals for the read and write ports, and strobes for external data latching.

The 674219 allows single-port static RAMs to resolve read and write request conflicts according to priority rules selected via the Priority-on-Read (PR) and Priority-on-Write (PW) inputs. If priority is given to either port, or if only one port is used, the maximum data rate through that port is 10 MHz.

Block Diagram

BUFFER SIZE SELECT (BF2-BF0)
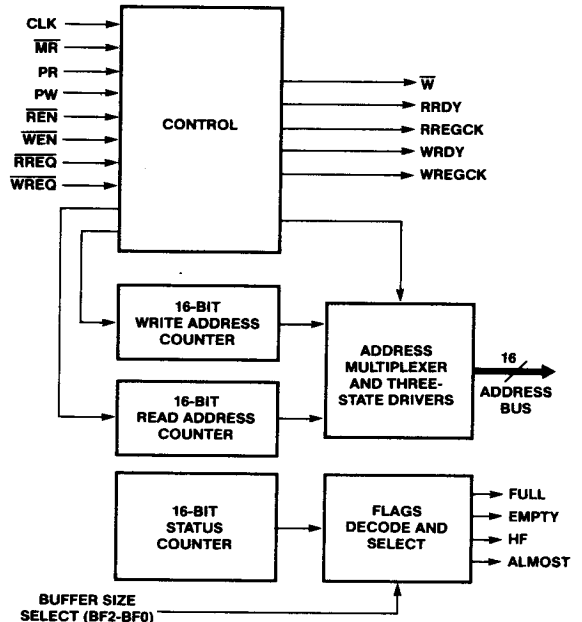
Definition of Terms

LATCHED A request has been received by the 674219 on one of its ports. The request has been internally latched, but not sampled.

SAMPLED The state of a latched request when it has been internally synchronized.

PROCESSED A decision to perform a sampled request.

PERFORMED When the processed request is executed as a memory cycle.

PENDING REQUEST A sampled request that has been held until the FIFO completes its current operation(s).

WRITE DATA PORT The register(s) where the system places the data that is to be written into the FIFO.

READ DATA PORT The register(s) where the system reads the FIFO data.

WRITE DATA REGISTER The register(s) which serves as the data input to the FIFO.

READ DATA REGISTER The register(s) where the FIFO leaves the read data for the system to take.

Architecture

The 674219 FIFO RAM Controller, together with an array of static RAMs and two registers, comprises a First-In-First-Out (FIFO) memory. (See Figure 1.)
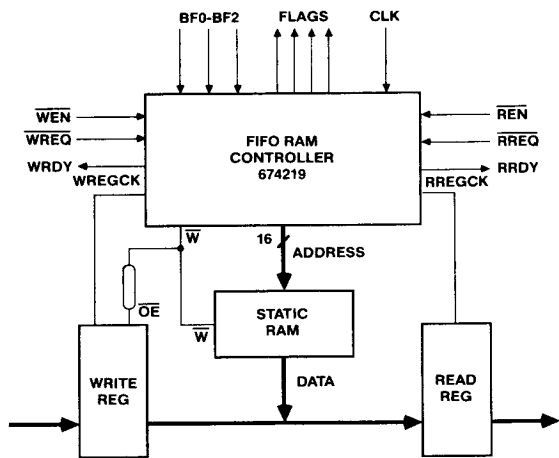

Figure 1. 57/674219 In and Implementation of a FIFO Buffer

The 674219 provides addresses and control signals to the static RAMs, and interfaces with the system via a write port, a read port, and status flags. The 674219 includes three 16-bit counters: a write-address counter, a read-address counter, and a status counter. The status flags are generated as a function of the state of the status counter and the buffer length selected. The write port has a Write REQuest ($\overline{\text{WREQ}}$) input, a Write ENable ($\overline{\text{WEN}}$) input, and a Write ReaDY (WRDY) output. The read port has a Read REQuest ($\overline{\text{RREQ}}$) input, a Read ENable ($\overline{\text{REN}}$) input, and a

Read ReaDY (RRDY) output. Two priority-control inputs, Priority-on-Write (PW) and Priority-on-Read (PR), determine the priority rules by which the 674219 arbitrates between simultaneous read and write requests. The 674219 provides two clock signals (RREGCK, WREGCK) to the Read Data Register and the Write Data Register, as well as a Write signal ($\overline{\text{W}}$) to be connected to the Write Enable ($\overline{\text{WE}}$) inputs of the static RAMs. Sixteen address outputs provide the read and write addresses to the static RAMs. When both $\overline{\text{REN}}$ and $\overline{\text{WEN}}$ are HIGH, the address outputs go into high-impedance (Hi-Z) state, so that the static RAMs can be accessed externally.

A Master Reset ($\overline{\text{MR}}$) input allows initializing the part by clearing the three counters and presetting the flags. (See Table 1.)

FLAG	CONDITION
Empty	High
Full	Low
Almost	High
Half	Low

Table 1. Condition of Flags After Master Reset

Pin Definitions

VCC 5.0 V ± 10%

GND Ground

CLK CLOCK—Controls synchronous operation of the device. All requests are sampled internally on every other LOW-to-HIGH transition of the clock. These transitions are called sampling clock edges. The first sampling clock edge is the first LOW-to-HIGH transition of the clock after master reset.

BF2-BF0 BUFFER SIZE CONTROLS—Determine the desired buffer size. (See Table 3.) Setting the buffer size is essential for correct operation of the status flags.

$\overline{\text{MR}}$ MASTER RESET—Clears all counters when LOW. The first LOW-to-HIGH transition of the clock, following a LOW-going Master Reset pulse, is the first sampling clock edge; the first request to be serviced is a write request. (See Figure 7.)

A15-A0 ADDRESS OUTPUTS—Three-state outputs which provide a read address when $\overline{\text{W}}$ is HIGH, or a write address when $\overline{\text{W}}$ is LOW. A15-A0 are in the Hi-Z state only when both $\overline{\text{REN}}$ and $\overline{\text{WEN}}$ are HIGH.

TEST An input used during manufacturing final test. For normal operation, TEST should be tied to GND.

$\overline{\text{W}}$ WRITE CONTROL—Used to control the SRAM arrays Write Enable pin and to output enable the write data register.

$\overline{\text{WREQ}}$ WRITE REQUEST—A LOW-going pulse on this pin requests a write to the FIFO. A write request can only be latched if the write port is enabled ($\overline{\text{WEN}}$ is LOW), and the previous write request has been processed (WRDY is HIGH).

$\overline{\text{RREQ}}$ READ REQUEST—A LOW-going pulse on this pin requests a read from the FIFO. A read request can only be latched if the read port is enabled ($\overline{\text{REN}}$ is LOW), and the previous read request has been processed (RRDY is HIGH).

WEN WRITE ENABLE—When this input is HIGH, all write requests are ignored. When WEN is LOW and WRDY is HIGH, a write request (WREQ = LOW-going pulse) will be latched by the 674219. If both WEN and REN are HIGH, the address outputs A15-A0 go into the Hi-Z state, permitting external access to the SRAM array.

REN READ ENABLE—When this input is HIGH, all read requests are ignored. When REN is LOW and RRDY is HIGH, a read request (RREQ = LOW-going pulse) will be latched by the 674219. If both WEN and REN are HIGH, the address outputs A15-A0 go into the Hi-Z state, permitting external access to the SRAM array.

PW, PR WRITE PRIORITY and READ PRIORITY—These two inputs determine the rules governing the arbitration between write and read requests. (See Table 2.) *These inputs must not both be HIGH simultaneously.*

WRDY WRITE READY—When this output is HIGH, and WEN is LOW, a write request may be sent to the WREQ pin.

WRDY goes LOW on the sampling clock edge which samples the write request. WRDY will go HIGH on the non-sampling clock edge which starts the write cycle. WRDY will stay LOW if the FIFO is full.

Write requests should be made only when WRDY is HIGH.

RRDY READ READY—When this output is HIGH, and REN is LOW, a read request may be sent to the RREQ pin.

RRDY goes LOW on the sampling clock edge which samples the read request. RRDY will go HIGH on the non-sampling clock edge which starts the read cycle. RRDY will stay LOW if the FIFO is empty.

Read requests should be made only when RRDY is HIGH.

WREGCK WRITE REGISTER CLOCK—This output is used to clock the write data register.

RREGCK READ REGISTER CLOCK—This output is used to clock the read data register.

EMPTY EMPTY FLAG—When HIGH, indicates that the FIFO is empty. Read requests are not permitted when the FIFO is EMPTY.

FULL FULL FLAG—When HIGH, indicates that the FIFO is full. Write requests are not permitted when the FIFO is FULL.

HF HALF-FULL FLAG—When HIGH, indicates that the FIFO has half, or more, of its locations occupied.

ALMOST ALMOST FLAG—When HIGH, indicates that one of the following conditions exists:

1. The FIFO is almost empty (less than sixteen words in the FIFO), if ALMOST is HIGH and HF is LOW.

2. The FIFO is almost full (sixteen or less locations are available) if ALMOST is HIGH and HF is HIGH.

Requests, Arbitration and Data Capture

A clock, supplied via the CLK input of the 57/674219, generates the internal sequence of events which constitutes a single FIFO operation. The read and write ports recognize and latch read and write requests asynchronously, provided that the respective enable (REN or WEN) is LOW, and the request window setup time is observed.

The FIFO *write* operation is as follows (see Figure 2):

Stage 1 A write request is sent to the 674219 by a LOW-going pulse on the WREQ pin.

Stage 2 The write request is latched internally, asynchronous to the clock.

Stage 3 WRDY goes LOW on the sampling clock edge that latched the request to indicate to the system that the request has been latched and synchronized internally. WRDY also indicates to the system that the write port is no longer accepting write requests. In order to guarantee that a request is properly synchronized, the request must not occur during the window stated by the tWRQC specifications.

Stage 4a Regardless of whether the write cycle is started or not, WREGCK will go HIGH for one clock cycle on the non-sampling clock edge that follows WRDY going LOW. The transition from LOW-to-HIGH on the WREGCK pin clocks data into the write data port, reading the data for writing to the SRAM.

Stage 4b A decision to wait, or to perform the write cycle is made based on the following:

Case 1 If read priority is set, the 674219 will process all pending read requests first. The write cycle will be delayed until all of the read cycles have been performed. Then, and only then, will the pending write cycle be performed.

Case 2 If write priority is set, regardless if there is a pending read request or not, the write cycle will start on the next non-sampling clock edge that follows WRDY going LOW. If there was a pending read request, the read cycle will not be started until the write cycle has been completed.

Case 3 If no priority is set, and there is no pending read request, the FRC will start the write cycle on the next non-sampling clock edge that follows WRDY going LOW.

Case 4 If no priority is set, and there are simultaneous requests (i.e., a read request and a write request have both been latched before the same sampling clock edge), the FIFO will decide which is to be processed first according to the following:

If the last case of simultaneous requests (with no priority) performed a read cycle first, the write request will be processed first, followed by the read request.

If the last case of simultaneous requests (with no priority) performed a write cycle first, the read request will be processed first, followed by the write request.
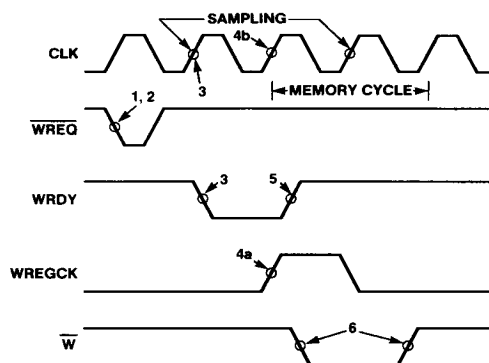

Figure 2. The Stages of a FIFO Write Operation

Stage 5 WRDY will go HIGH on the non-sampling edge that starts the write cycle.

Stage 6 Once a request has been granted, the memory cycle takes place over two clock cycles, starting with the non-sampling clock edge on which the request is granted (WRDY going from LOW-to-HIGH). The Write line ($\overline{W}$) goes LOW at tCWL after the clock edge starting the memory cycle and stays low until tCWH after the clock edge terminating the memory cycle.

The FIFO *read* operation is as follows (see Figure 3):

Stage 1 A read request is sent to the 674219 by a LOW-going pulse on the $\overline{RREQ}$ pin.

Stage 2 The read request is latched internally, asynchronous to the clock.

Stage 3 RRDY goes LOW on the sampling clock edge that latched the request to indicate to the system that the request has been latched and synchronized internally. RRDY also indicates to the system that the read port is no longer accepting read requests. In order to guarantee that a request is properly synchronized, the request must not occur during the window stated by the tRRQC specifications.

Stage 4 A decision to wait, or to perform the read cycle is made based on the following:

Case 1 If write priority is set, the 674219 will process all pending write requests first. The read cycle will be delayed until all of the write cycles have been performed. Then, and only then, will the pending read cycle be performed.

Case 2 If read priority is set, regardless if there is a pending write request or not, the read cycle will start on the next non-sampling clock edge that follows RRDY going LOW. If there was a pending write request, the write cycle will not be started until the read cycle has been completed.

Case 3 If no priority is set, and there is no pending write request, the FRC will start the read cycle on the next non-sampling clock edge that follows RRDY going LOW.

Case 4 If no priority is set, and there are simultaneous requests (i.e., a read request and a write request have both been latched before the same sampling clock edge), the FIFO will decide which is to be processed first according to the following:

1. If the last case of simultaneous requests (with no priority) performed a read cycle first, the write request will be processed first, followed by the read request.

2. If the last case of simultaneous requests (with no priority) performed a write cycle first, the read request will be processed first, followed by the write request.

Stage 5 RRDY will go HIGH on the non-sampling edge that starts the write cycle.

Stage 6 Once a request has been granted, the memory cycle takes place over two clock cycles, starting with the non-sampling clock edge on which the request is granted (RRDY going from LOW-to-HIGH). Read REGister Clock (RREGCK) goes LOW for one clock cycle, starting with the sampling clock edge that occurred within the read memory cycle. RREGCK clocks data from the SRAM array to the read data port on the LOW-to-HIGH transition, which terminates the read cycle.
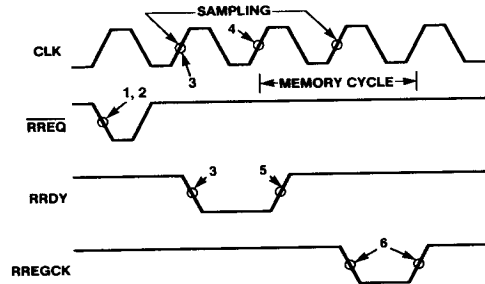

Figure 3. The Stages of a FIFO Read Operation

Priority

Two input signals, Priority-on Read (PR) and Priority -on-Write (PW), determine the arbitration rule which sequences the read and write cycles, for various cases as follows: (see Table 2):

PW	PR	PRIORITY
0	0	No priority
0	1	Priority on READ
1	0	Priority on WRITE
1	1	(Not allowed)

**Table 2. Priority Encoding**

No-Priority Case

If no priority is selected (PR = PW = LOW), each request is processed in the order it came into the FRC.

If no priority is set and both a read and write request are latched before the same sampling clock edge, the 674219 will perform read and write cycles alternately. (See Figure 4.)

Write Priority Case

If write priority is selected (PR = LOW, PW = HIGH) write requests are always processed before read requests (assuming that the requests meet the setup time).

If write priority is set and both a read and write request are latched before the same sampling clock edge, (i.e., a simultaneous request), the write cycle will take place first. If, before the next sampling clock edge, another write request is latched, another write cycle will take place, and the pending read request will not be processed. Only when the sampling clock edge encounters no further write requests will the pending read request be processed. At this time the read cycle will start and the RRDY output will go HIGH. (See Figure 5.)
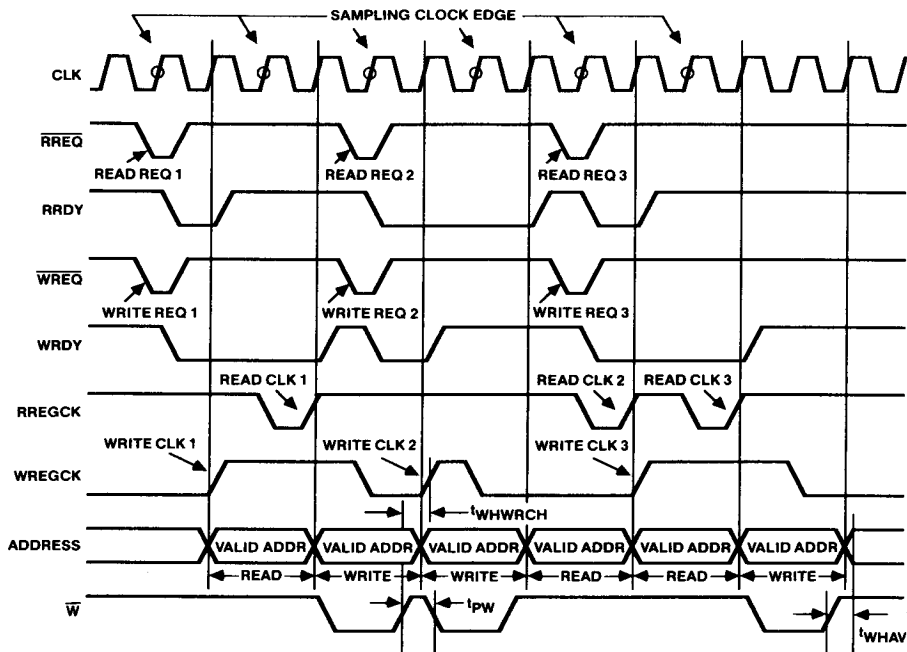
Notes: 1. Assumes not at FULL and not at EMPTY.
2. Assumes last case of simultaneous requests processed a write first.
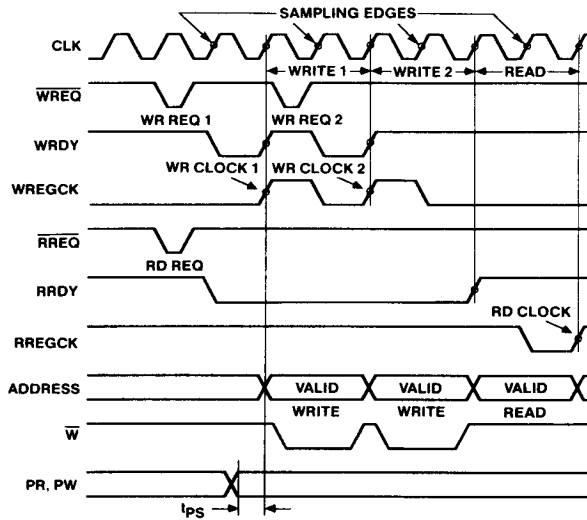
Figure 4. Operation With No Priority

Figure 5. Operation With Write Priority

Read Priority Case

If read priority is selected (PR = HIGH, PW = LOW) read requests are always processed before write requests assuming that the requests meet the setup time).

If read priority is set and both a read and write request are latched before the same sampling clock edge, (i.e., a simultaneous request), the read cycle will take place first. If, before the next sampling clock edge, another read request is latched, another read cycle will take place and the pending write request will not be processed. Only when the sampling clock edge encounters no further read requests will the pending write requests be processed. At this time, the write cycle will start and the WRDY output will go HIGH. (See Figure 6.)
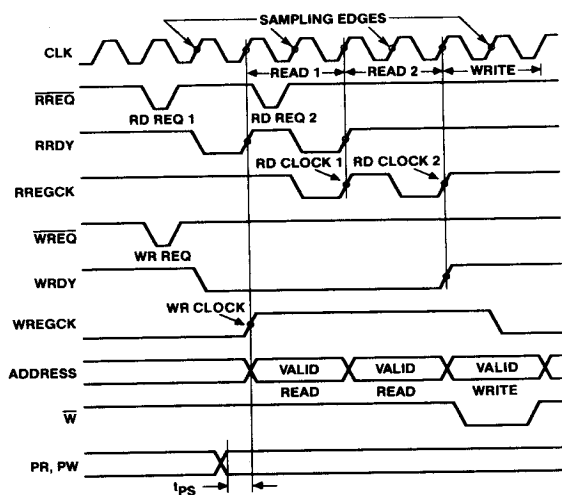

Figure 6. Operation With Read Priority

Buffer Length

A three-bit input control field, BF2-0, selects the buffer length ("depth") of the FIFO. Any power of 2 from 512 to 65,536 may be chosen as the buffer length. (See Table 3.)

BF2	BF1	BF2	BUFFER SIZE
0	0	0	512
0	0	1	1024
0	1	0	2048
0	1	1	4096
1	0	0	8192
1	0	1	16384
1	1	0	32768
1	1	1	65536

Table 3. Buffer Length

Status Flags

The flags are generated as a function of the buffer length, selected via inputs BF2-BF0, and the state of the status counter. The status flags are:

EMPTY   When HIGH, the EMPTY flag indicates that the FIFO is empty. The EMPTY flag goes HIGH on the first sampling clock edge during the memory cycle which empties out the FIFO.

FULL   When HIGH, the FULL flag indicates that the FIFO is full, and no more data can be written into it until a read cycle takes place. The FULL flag goes HIGH on the first sampling clock edge during the memory write cycle which fills up the FIFO.

HF   When HIGH, the Half-Full flag indicates that the FIFO is filled to half its depth, or more.

ALMOST   When HIGH, the ALMOST flag indicates that one of the following conditions exists:

1. The FIFO is almost empty (less than sixteen words in the FIFO), if ALMOST is HIGH and HF is LOW.

2. The FIFO is almost full (sixteen or less locations are available) if ALMOST is HIGH and HF is HIGH.

The flags Master Reset to the states shown in Table 1.

First Write Cycle (After a Master Reset or When FIFO is Empty)

The first LOW-to-HIGH clock edge, following Master Reset ($\overline{MR}$) going LOW-to-HIGH, is the first sampling clock edge. The sampling clock edge occurs every other positive-going transition of the clock. The LOW pulse on $\overline{MR}$ clears the three internal 16-bit counters (status, read and write). The FIFO is set to the EMPTY state, and no read requests are allowed (RRDY = LOW).

After an interval of at least tMRS after $\overline{MR}$ goes HIGH, a LOW-going pulse on the $\overline{WREQ}$ pin tells the 674219 that a write to the FIFO is requested. The write request is latched by the write port, provided that $\overline{WEN}$ is LOW. (See Figure 7.) The following sampling clock edge samples the request, and causes WRDY to go LOW. WRDY goes HIGH again on the next (non-sampling) positive clock edge, regardless of priority. The write cycle takes place over two clock periods, starting on the positive non-sampling clock edge following the sampling clock edge which brought WRDY HIGH. The data is clocked into the external Write Data Register on the same non-sampling clock edge, and into the external Read Data Register on the second sampling clock edge, to allow minimal fall-through time. (See again Figure 7.) EMPTY will go LOW to indicate that there is valid data in the FIFO. RRDY goes HIGH indicating that there is data to be read from the FIFO. The same sequence of events occurs for the first write request that is initiated when the FIFO is empty.

Methodology for Reading

In order to maintain a consistent system level architecture, the 674219 has been constructed such that the system should read the data port *before* a read request is sent. (See Figure 8.)

This ability allows the FIFO a zero fall-through time on all cycles. The system is able to get the data from the FIFO right away, without having to wait for the FRC to perform a read cycle of the SRAMs.

On the read port, a positive-going edge of RREGCK signals to the system that the read data register is being updated. The system should read the data first and then send a request to obtain the next word from memory to the read data register.
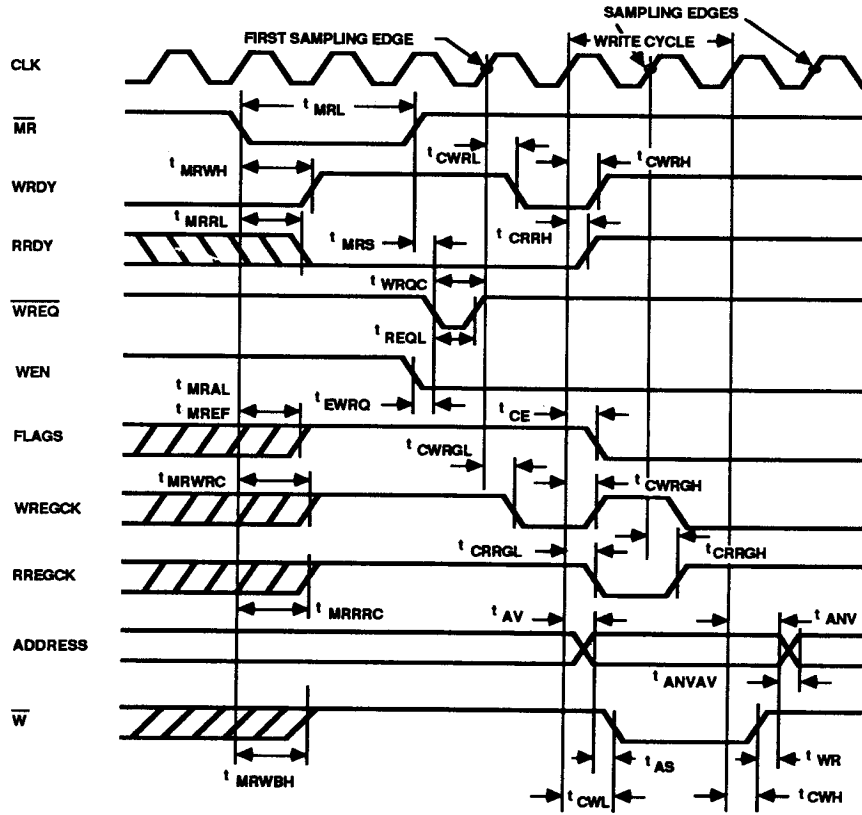
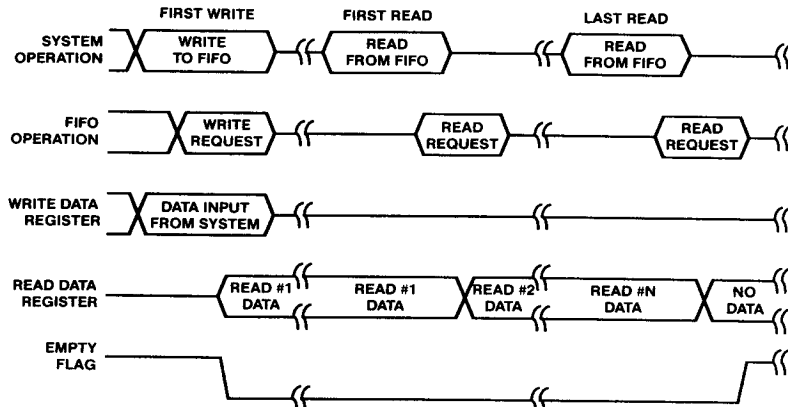Figure 7. First Write After Master Reset or When FIFO is Empty

Figure 8. Methodology for Reading From the FIFO

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Write Cycle (Figure 9)

A write request, indicated by a LOW-going pulse on the $\overline{WREQ}$ pin, is latched by the 674219, provided that $\overline{WEN}$ is LOW and WRDY is HIGH. The request is sampled internally on the sampling clock edge. WRDY goes LOW on the same sampling clock edge, to indicate to the system that a write request has been latched and synchronized internally. In addition, WREGCK will go HIGH for one clock cycle on the non-sampling clock edge that follows WRDY going LOW, regardless of whether the write request is processed. The write request will be processed only if one of the following sets of conditions is true:

1. Write Priority has been selected.

   If write priority has been selected, the FRC will process all write requests before any pending read requests.

2. No read request has been latched.

   If no read request has been latched, regardless of priority, the FRC will process the write request immediately and will start the write memory cycle on the non-sampling clock edge that follows WRDY going LOW.

3. No priority has been selected, both a read and a write request occur before the same sampling clock edge (simultaneous request), and in the last case of a simultaneous request, the FRC processed the read request first.

   In this case, the 674219 will process the write request first, and then process the read request.

4. No priority has been selected, both a read and a write request occur before the same sampling clock edge (simultaneous request), and in the last case of a simultaneous request, the FRC processed the write request first.

   In this case the 674219 will process the read request first, and then process the write request.

Once the write request has been processed, a write cycle takes place over two clock cycles starting with the non-sampling clock edge on which WRDY goes HIGH. $\overline{W}$ will go LOW, tCWL after the start of the write cycle. $\overline{W}$ is used to Write Enable the SRAM array and to Output Enable the write data register. Two clocks later (tCWH) $\overline{W}$ will go HIGH again, terminating the write cycle.

In order to avoid the bus contention inherent in shared-I/O memory systems, a delay line and an OR gate may be required (see Memory Interface Design Guidelines).
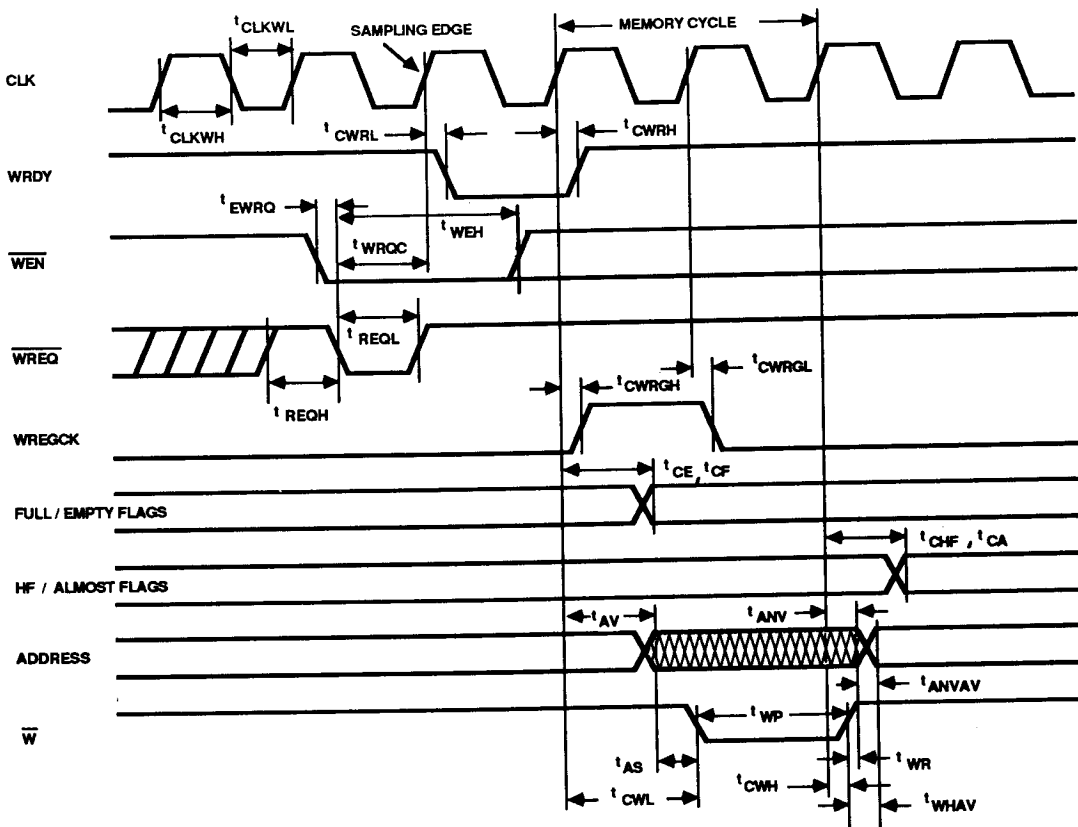

Figure 9. Write Cycle Timing

Read Cycle (Figure 10)

A read request, indicated by a LOW-going pulse on the $\overline{RREQ}$ pin, is latched by the 674219, provided that $\overline{REN}$ is LOW and RRDY is HIGH. The request is sampled internally on the sampling clock edge. RRDY goes LOW on the same sampling clock edge to indicate to the system that a read request has been latched and synchronized internally. The read request is processed only if one of the following sets of conditions is true:

1. Read Priority has been selected.

   If read priority has been selected, the FRC will process all read requests before any pending write request.

2. No write request has been latched.

   If no write request has been latched, regardless of priority, the FRC will process the read request immediately and will start the read memory cycle on the non-sampling clock edge that follows RRDY going LOW.

3. No priority has been selected, both a read and a write request occur before the same sampling clock edge (simultaneous request), and in the last case of a simultaneous request, the FRC processed the write request first.

   In this case, the 674219 will process the read request first.

4. No priority has been selected, both a read and a write request occur before the same sampling clock edge (simultaneous request), and in the last case of a simultaneous request, the FRC processed the read request first.

   In this case, the 674219 will process the write request first, and then process the read request.

Once the read request has been processed, a read cycle takes place over two clock cycles starting with the non-sampling clock edge on which the RRDY goes HIGH. RREGCK goes LOW on the next sampling clock edge, stays LOW for one clock cycle, and goes HIGH on the following non-sampling clock edge, thus clocking the data which appears at the SRAM array's data outputs into the Read Data Register. RREGCK going HIGH terminates the read cycle.
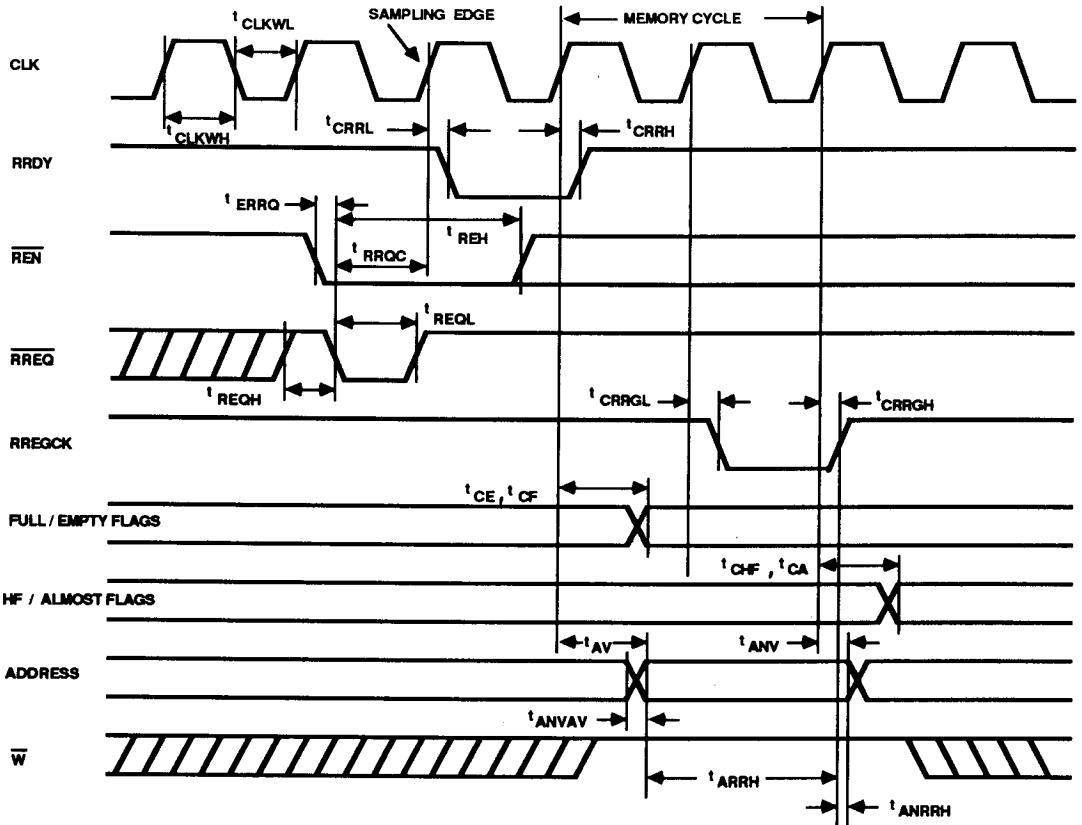

Figure 10. Read Cycle Timing

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Memory Interface Design Guidelines

Introduction

The purpose of the memory interface design guideline is to aid the engineer in interfacing the 674219 FIFO RAM Controller (FRC) to an array of static RAMs. This guideline will be broken down into three separate sections. The first section is a timing analysis of the read cycle. The second section is a timing analysis of the write cycle. The final section will guide the designer through a real design.

Figure 11 shows a typical SRAM interface schematic.

Section One: Read Cycle Timing Analysis

Figure 12 shows the basic timings which are critical to the read cycle. Some of these parameters apply to the FRC, some to the SRAM array, and others to external logic. For convenience, these parameters are broken up below:

FRC Parameters:

t_{AV} Clock to Address Valid Time
t_{ANV} Clock to Address Not Valid Time

SRAM Parameters

t_{RC} Read Cycle Time
t_{ACS} Chip Select Access Time
t_{AA} Address Access Time
t_{OH} Output Data Hold Time from Address Change
t_{HZ} Chip Deselect to Output in High-Z

External Logic:

Chip Select Decoder Parameters:

t_{DECODE} t_{PD} through Decoder

Read Data Register Parameters:

t_S Data Setup Time
t_H Data Hold Time

Other Parameters (See Text):

t_{RDREGH} Clock to RDCLK High [RDCLK is the clock input of the Read Data Register]

(This parameter is normally t_{CRRGH} of the FRC)

There are six separate equations which must each be met in order to determine what speed of SRAM the designer will need. It is assumed that the user has already specified a speed of operation and the external components needed. The equations listed can be used at any frequency, up to a maximum of a 20-MHz clock rate.

Since every read cycle consists of two physical clock cycles, all equations are with respect to 2T (2 x Cycle Time).

The first equation which should be satisfied is the read cycle time (tRC). This identifies what speed SRAM is required. The equation is based on the total time that the address is valid minus the decoder time. Since the decoder has some minimum skew on the negating edge, this time is ADDED to the equation. The equation thus becomes:
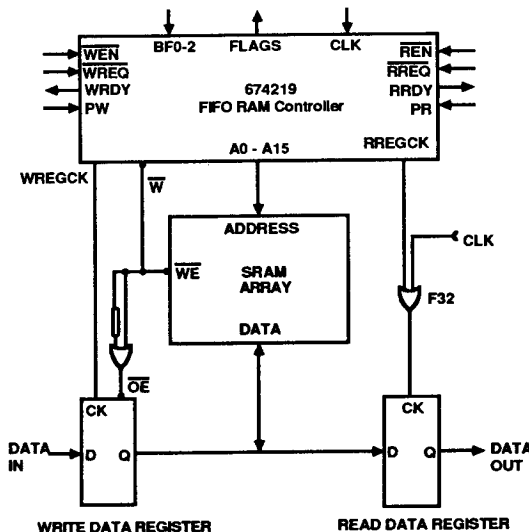

Figure 11. A Typical SRAM Interface

Equation 1-1

$$t_{RC} \leq 2T - t_{DECODE(max)} + t_{DECODE(min)} - t_{ANVAV(max)}$$

The access time must be looked at next. There are actually two separate equations that help determine the access time.

Equation 1-2 determines the address access time (tAA). tAA is based on the time that the address is valid before the read register gets clocked. The equation takes into account the setup time of the read data register (tS) as well. The equation is:

Equation 1-2

$$t_{AA} \leq 2T - MAX(t_{AV} - t_{RDREGH}) - t_{S(min)}$$

Where $MAX(t_{AV} - t_{RDREGH})$ is the maximum difference between t_{AV} and t_{RDREGH}

Equation 1-3 determines the chip select access time (tACS). This time is based on the time the address is valid before the read register gets clocked MINUS the maximum skew through the chip select decoder. This is done to ensure that the decoder delay is taken into consideration. Again, the read register setup time is considered. The modified equation thus becomes:

Equation 1-3

$$t_{ACS} \leq 2T - t_{DECODE(max)} - MAX(t_{AV} - t_{RDREGH}) - t_{S(min)}$$

Where $MAX(t_{AV} - t_{RDREGH})$ is the maximum difference between t_{AV} and t_{RDREGH}

The next two equations take into consideration the read data hold time with respect to the address (tOH), and the chip deselect to data outputs in High-Z time (tHZ). We will consider the more critical tOH. tOH can easily be determined by comparing the data hold time PLUS the clock to address not valid (tANV) time with the sum of the clock to RDCLK HIGH time (tRDREGH) and the data register hold time (tH). The equation for this becomes:

Equation 1-4

$$t_{OH}(min) + t_{ANV}(min) \geq t_{RDREGH}(max) + t_H(min)$$

If the SRAM has an extraordinarly long read data hold time (tOH), the above equation must be modified to include the now more critical chip deselect to data outputs in High-Z time (tHZ). This is done by simply substituting tHZ for tOH. The modified equation is:

Equation 1-5

$$t_{HZ}(min) + t_{ANV}(min) \geq t_{RDREGH}(max) + t_H(min)$$

In addition to the above equations, one more is necessary in certain cases. In Figure 12, the read cycle is shown. At the very end of a read cycle, the read data register is clocked. The normal clocking signal for the FRC is RREGCK. Since the read data register's clock is normally connected to RREGCK, if RREGCK goes HIGH after the data from the SRAMs goes away, the data will be lost. This is only true if the SRAMs have a low tOH(min). Normally, in all of the above equations, the clock to RREGCK HIGH (tCRRGH) is substituted in place of tRDREGH. In the cases where a low tOH does not guarantee the data will be properly clocked, the user has another alternative.

By adding an external OR gate between the clock and RREGCK, the user can effectively shorten tCRRGH(max). The gate "ANDs" the active LOW RREGCK with the clock when it is LOW. This produces an active LOW output signal called RDCLK (see Figure 12). This will bring the edge of read register clock into specification for any tOH, even one of zero. Figure 11 shows a typical example of a SRAM interface, including this gate, should it be necessary.

Because the OR gate inherently has some delay, an equation is necessary to calculate the new tCRRGH. (This "new" parameter is called tRDREGH). It should be noted that if the designer finds it necessary to implement this logic, due to a low tOH, he/she must replace the tRDREGH in Equation 1-1 through 1-5 with the result from the following equation, rather than the normal tCRRGH. The equation for the gate is:

Equation 1-6

$$t_{RDREGH}(max) = t_{PDOR}(max)$$

Where $t_{PDOR}(max)$ is the maximum t_{PD} through the OR gate.

Since the clock will bring RDCLK low some tPDOR(max) later, the setup time of the read data register is automatically achieved.

The above equations complete the timing analysis for a read cycle. Once the user has gone through both the read and write cycle timings, an appropriate Static RAM may be chosen.
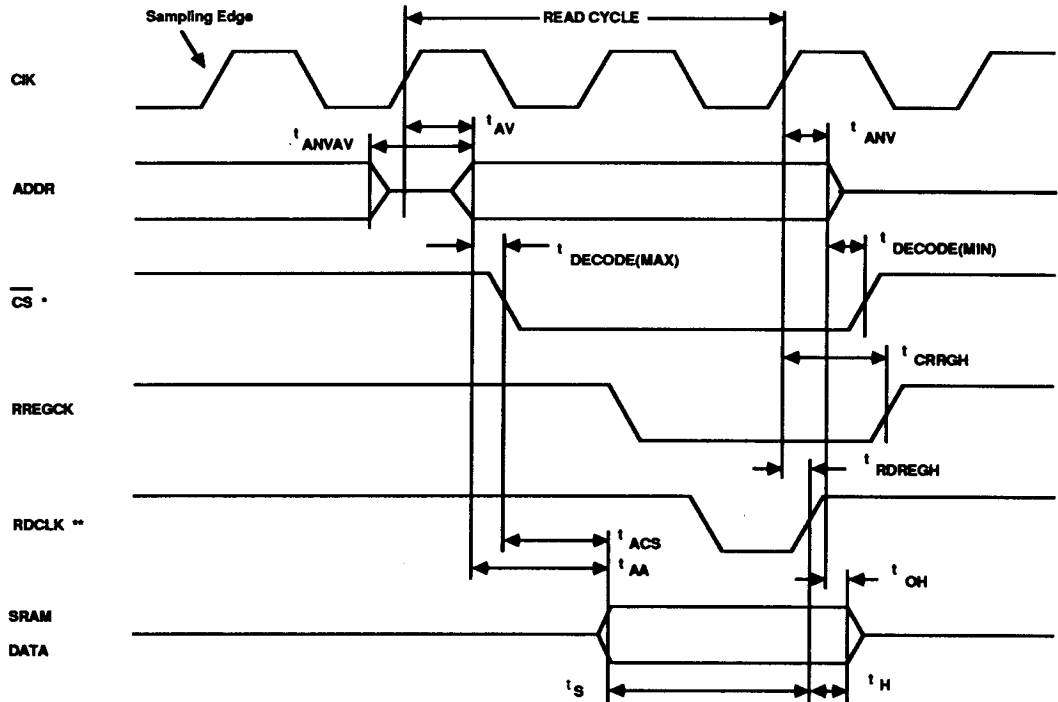
* CS to the Static RAM bank
** Actual clock input to the Read Data Register. This may be the same as RREGCK or may be the output of the OR-gate shown in Figure 1

Figure 12. Read Cycle Timing

Section Two:
Write Cycle Timing Analysis

Figure 13 shows the basic timings which are critical to the write cycle. Some of these parameters apply to the FRC, some to the Static RAM array, and others to external logic. The parameters that are unique to the write cycle will be summarized below:

FRC Parameters:

t_{PW}	Write Pulse Width HIGH
t_{WHAV}	$\overline{W}$ HIGH to Address Valid
t_{ANVAV}	Address Not Valid to Address Valid
t_{WHWRCH}	$\overline{W}$ HIGH to WREGCK HIGH

SRAM Parameters

t_{WC}	Write Cycle Time
t_{AW}	Address Valid to End of Write
t_{CW}	$\overline{CS}$ to End of Write
t_{WP}	$\overline{WE}$ Pulse Width LOW
t_{DW}	Data Valid to End of Write
t_{WZ}	$\overline{WE}$ LOW to Outputs in High-Z

External Logic:

Write Data Register Parameters:

t_{PZ}	$\overline{OE}$ to Outputs in Low-Z
t_{CP}	Clock to Outputs Valid

Other Parameters (See Text):

t_{WOE}	$t_{DLY(max)}$ + $t_{ORSKEW(max)}$

There are six equations which must determine the write cycle specifications for the Static RAM. It is assumed that the user has already selected the frequency of operation and the external components needed for his/her system.

Since every write cycle consists of two physical clock cycles, all equations are with respect to 2T (2 x Cycle Time).

The first equation which should be looked at is the write cycle time (t_{WC}). This equation will determine what speed of SRAM is required for proper operation. This parameter is the same as the total time that the address is valid. This is calculated with the following equation:

Equation 2-1

$$t_{WC} \leq 2T - t_{ANVAV(max)}$$

There are three basic areas to be looked at once the write cycle time has been determined. The first is the access time of the SRAM. There are two separate equations in this area.

The first parameter to be analyzed is the time from address valid to the end of write (t_{AW}). This parameter can be calculated by taking the total write cycle time (2T) and subtracting from it, the time from $\overline{W}$ going HIGH to the next address becoming valid. The equation is:
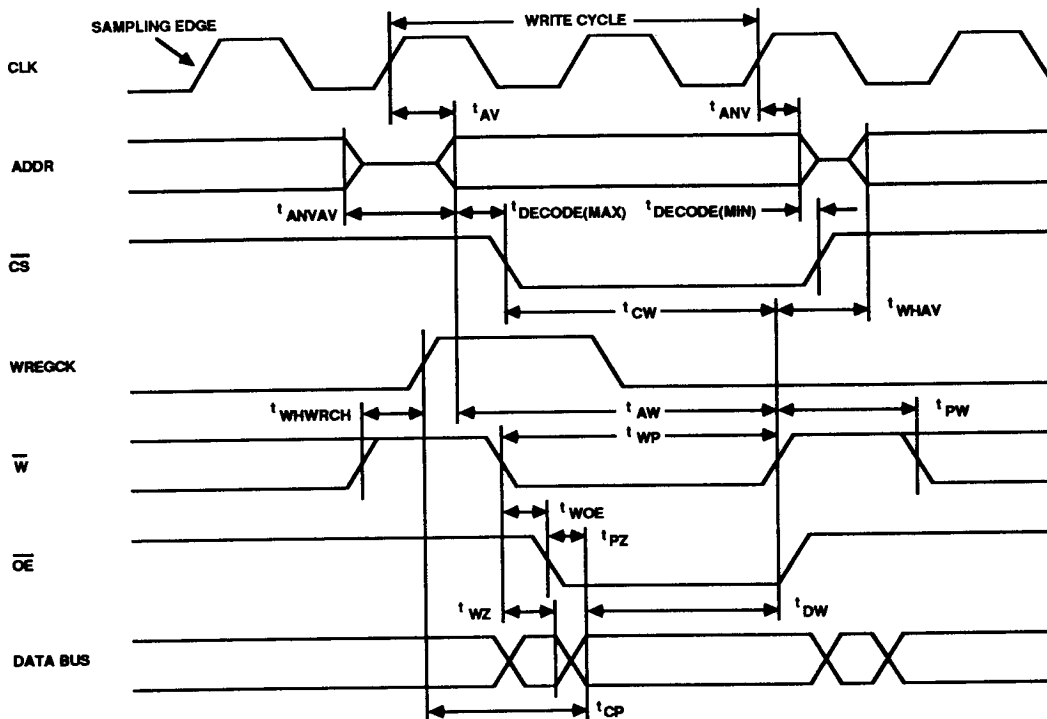

Figure 13. Write Cycle Timing

Equation 2-2

$t_{AW} \leq 2T - t_{WHAV}(max)$

The designer must also check the chip select to end of write time (tCW). This is often more critical than tAW in determining which SRAM to use in the system. The tCW parameter can be obtained in the same way as tAW except that the decode time is also included in the equation. The modified equation is:

Equation 2-3

$t_{CW} \leq 2T - t_{WHAV}(max) - t_{DECODE}(max)$

In addition to the various access times of the write cycle, the user must next look at the pulse width of the write signal (tWP). This is basically the difference between 2T and the FRC's write time HIGH (tPW). The equation is:

Equation 2-4

$t_{WP} \leq 2T - t_{PW}(max)$

The last area that needs to be analyzed is the data setup time of the SRAM. The data setup time is specified as the time data is valid before write goes HIGH (tDW).

There are three separate equations which determine the required tDW of the SRAM.

The write register has a certain propagation delay from its clock input pulse before the data becomes valid. Data must be valid at least tDW before $\overline{WE}$ goes HIGH or it will be lost. The equation takes into account the clock to output time (tCP) of the write register. The equation is:

Equation 2-5

$t_{DW} \leq 2T - t_{CP}(max) - t_{WHWRCH}(max)$

The write data register is enabled by the $\overline{W}$ signal of the FRC. The register takes some minimum time before it enables its outputs from the High-Z state (tPZ).

The SRAMs have some maximum time in which they disable their outputs when the $\overline{WE}$ signal goes LOW. This parameter is the time from $\overline{WE}$ LOW to the data outputs in High-Z (tWZ).

If tWZ(max) is greater than tPZ(min), bus contention will result. To counter this problem a delay must be introduced between the W signal of the FRC and the $\overline{OE}$ input of the write data register. In addition, an OR gate is used to bring $\overline{OE}$ HIGH shortly after $\overline{W}$ goes HIGH. This is illustrated in Figure 11. tWOE(max) is the total delay between $\overline{W}$ going LOW and $\overline{OE}$ going LOW. It is calculated by the following equation:

Equation 2-6

$t_{WOE}(max) = t_{DLY}(max) + t_{PDOR}(max)$

Where $t_{DLY}(max)$ is the maximum delay through the delay line.

$t_{PDOR}(max)$ is the maximum propagation delay through the OR gate.

Equation 2-5 dictated the tDW based on the clock to output time of the register. In most cases though, this time is automatically guaranteed. Since the data will not be valid (Low-Z) until some tPZ after $\overline{OE}$ goes LOW, even though it has been clocked properly, a new equation is necessary to determine the tDW of the SRAM. This equation must take into account the delay that was added in to prevent bus contention. It must also take into

account the tPZ time of the register. The equation is very similar to Equation 2-5 with those exceptions. The equation thus becomes:

Equation 2-7

$t_{DW} \leq 2T - t_{PW}(max) - t_{PZ}(max) - t_{WOE}(max)$

One additional equation is required to determine the delay line required to prevent bus contention. The equation for the delay line takes into account the maximum tPD through the OR gate. The equation is based on the tWZ of the SRAM and the tPZ of the write data register. The equation is:

Equation 2-8

$t_{DLY}(min) = t_{WZ}(max) - t_{PZ}(min) - t_{OR}(min)$

The above equations complete the timing analysis of the write cycle. Once the user has gone through both the read and write cycle timings, an appropriate Static RAM may be chosen.

An Example Interface

In order to determine any Static RAM parameters, the user must know several things. He/she must identify the frequency of operation, the read and write data registers, the chip select decoder, and any other logic which may be necessary.

As an example, assume that a 5-MHz data throughput is desired. This will allow a 10-MHz all read or all write data rate. This data rate dictates a 20-MHz clock speed for the FRC.

For worst case design, assume that the selected SRAM has a tOH of zero. Since tOH = 0 ns, there must be an external OR-gate to clock the read register. In addition, assume that the selected SRAM has a tWZ(max) ≤ 20 ns.

In order to resolve any bus contention a delay line and another OR gate will be added.

74F series parts are used to keep the design clean. It should be noted that the user can use any kind of logic. Because of the particular worst case SRAM parameters that were chosen, this design contains the maximum number of parts that are required for any design.

Given the above considerations, this 20-MHz design requires the following parts:

Parts List:

QTY	PART	DESCRIPTION
1	674219	FIFO RAM Controller
1	74F138	Address Decoder
2	74F374	8-bit Register
1	74F32	OR-Gate
1	20 ns ±10%	Delay Line

The following is a step-by-step analysis of the read and write equations to determine the required SRAM parameters. The equations will also show the delay line needed to avoid bus contention.

Read Equations:

Equation 1-1

$$t_{RC} \leq 2T - t_{DECODE(max)} + t_{DECODE(min)} - t_{ANVAV(max)}$$

$$\underset{[FRC]}{100} - \underset{[F138]}{9.0} + \underset{[F138]}{3.0} - \underset{[FRC]}{12}$$

$$t_{RC} \leq 82.0 \text{ ns}$$

Equation 1-6

$$t_{RDREGH(max)} = t_{ANV(min)} - t_{ORSKEW(max)}$$

$$\underset{[FRC]}{15} - \underset{[F32]}{6.6}$$

$$t_{RDREGH(max)} = 6.6 \text{ ns}$$

Equation 1-2

$$t_{AA} \leq 2T - MAX(t_{AV} - t_{RDREGH}) - t_{S(min)}$$

$$\underset{[FRC]}{100} - \underset{[FRC]}{(40} - \underset{[F32]}{8.4)} - \underset{[F374]}{2.0}$$

$$t_{AA} \leq 66.4 \text{ ns}$$

Equation 1-3

$$t_{ACS} \leq 2T - t_{DECODE(max)} - MAX(t_{AV} - t_{RDREGH}) - t_{S(min)}$$

$$\underset{[FRC]}{100} - \underset{[F138]}{9.0} - \underset{[FRC]}{(40} - \underset{[F32]}{8.4)} - \underset{[F374]}{2.0}$$

$$t_{ACS} \leq 57.4 \text{ ns}$$

Equation 1-4

$$t_{OH(min)} + t_{ANV(min)} \geq t_{RDREGH(max)} + t_{H(min)}$$

$$\underset{[SRAM]}{0} + \underset{[FRC]}{15} \geq \underset{[F32]}{8.4} + \underset{[F374]}{2.0}$$

$$15 \text{ ns} \geq 10.4 \text{ ns}$$

Equation 1-5

$$t_{HZ(min)} + t_{ANV(min)} \geq t_{RDREGH(max)} + t_{H(min)}$$

$$\underset{[SRAM]}{0} + \underset{[FRC]}{15} \geq \underset{[F32]}{8.4} + \underset{[F374]}{2.0}$$

$$15 \text{ ns} \geq 10.4 \text{ ns}$$

Write Equations:

Equation 2-1

$$t_{WC} \leq 2T - t_{ANVAV(max)}$$

$$\underset{[FRC]}{100} - \underset{[FRC]}{12}$$

$$t_{WC} \leq 88.0 \text{ ns}$$

Equation 2-2

$$t_{AW} \leq 2T - t_{WHAV(max)}$$

$$\underset{[FRC]}{100} - \underset{[FRC]}{25}$$

$$t_{AW} \leq 75.0 \text{ ns}$$

Equation 2-3

$$t_{CW} \leq 2T - t_{WHAV(max)} - t_{DECODE(max)}$$

$$\underset{[FRC]}{100} - \underset{[FRC]}{25} - \underset{[F138]}{9.0}$$

$$t_{CW} \leq 66.0 \text{ ns}$$

Equation 2-4

$$t_{WP} \leq 2T - t_{PW(max)}$$

$$\underset{[FRC]}{100} - \underset{[FRC]}{25}$$

$$t_{WP} \leq 75.0 \text{ ns}$$

Equation 2-5

$$t_{DW} \leq 2T - t_{CP(max)} - t_{WHWRCH(max)}$$

$$\underset{[FRC]}{100} - \underset{[F374]}{12.5} - \underset{[FRC]}{18}$$

$$t_{DW} \leq 69.5 \text{ ns}$$

Equation 2-8

$$t_{DLY(min)} = t_{WZ(max)} - t_{PZ(min)} - t_{OR(min)}$$

$$\underset{[SRAM]}{20} - \underset{[F374]}{2.0} - \underset{[F32]}{3.0}$$

$$t_{DLY(min)} = 15 \text{ ns (USE 20 ns ' 10\%}$$

Equation 2-6

$$t_{WOE(max)} = t_{DLY(max)} + t_{OR(max)}$$

$$\underset{[DELAY]}{22} + \underset{[F32]}{6.6}$$

$$t_{WOE(max)} = 28.6 \text{ ns}$$

Equation 2-7

$$t_{DW} \leq 2T - t_{PW(max)} - t_{PZ(max)} - t_{WOE(max)}$$

$$\underset{[FRC]}{100} - \underset{[FRC]}{25} - \underset{[F374]}{12.5} - \underset{[delay]}{28.6}$$

$$t_{DW} \leq 33.9 \text{ ns}$$

RESULTS

READ PARAMETERS:

Minimum t_{RC} = 82.0 ns
Minimum t_{AA} = 66.4 ns
Minimum t_{ACS} = 57.4 ns
Minimum t_{OH} = 0 ns (Assumed)
Minimum t_{HZ} = 0 ns (Assumed)

WRITE PARAMETERS:

Minimum t_{WC} = 88.0 ns
Minimum t_{AW} = 75.0 ns
Minimum t_{CW} = 66.0 ns
Minimum t_{WP} = 75.0 ns
Minimum t_{DW} = 33.9 ns (Equation 2-7 used for $t_{DW(min)}$)
Minimum t_{WR} = 0 ns (Because FRC's t_{WR} = 0 ns)

DELAY LINE:

20 ns Delay Line ('10%)

Based on those results, the Hitachi HM6168H-45 was selected. This is a 4096 x 4-bit Static RAM with a 45-ns access time. Its specifications are:

READ PARAMETERS:

Minimum t_{RC} = 45.0 ns
Minimum t_{AA} = 45.0 ns
Minimum t_{ACS} = 45.0 ns
Minimum t_{OH} = 5.0 ns
Minimum t_{HZ} = 0 ns

WRITE PARAMETERS:

Minimum t_{WC} = 45.0 ns
Minimum t_{AW} = 40.0 ns
Minimum t_{CW} = 40.0 ns
Minimum t_{WP} = 35.0 ns
Minimum t_{DW} = 20.0 ns
Minimum t_{WR} = 0 ns

Sixteen 4K x 4-bit SRAMs are required to complete a 32K x 8-bit FIFO buffer. The complete design is shown in Figure 14. This illustrates the two OR-gates, the delay line, the decoder, the two registers, the Static RAM array and the 674219 FIFO RAM Controller in a 20-MHz design.
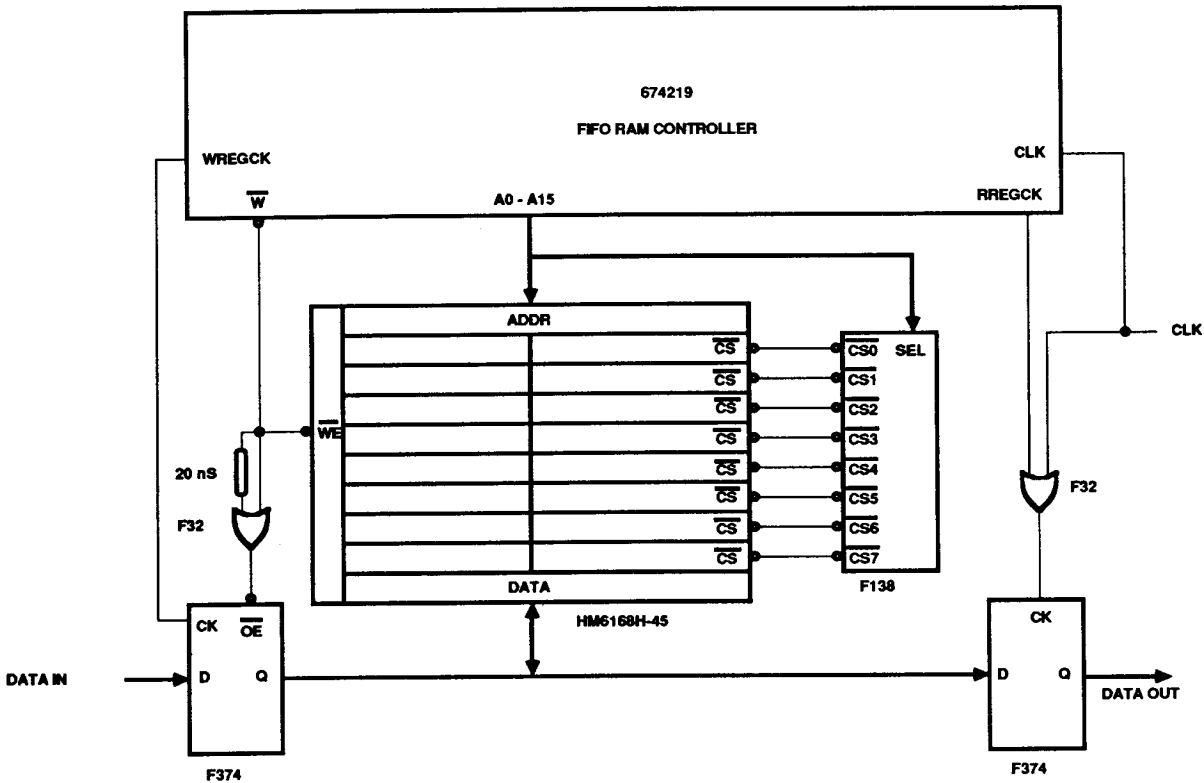

Figure 14. Worst Case Design for 20 MHz

Absolute Maximum Ratings

Supply voltage V_{CC} .... –0.5 V to 7.0 V
DC input voltage V_I .... –0.5 V to 5.5 V
DC output voltage, V_O .... –0.5 V to 5.5 V
Off-state output voltage .... –0.5 V to 5.5 V
Storage termperature .... –65° to +150° C

Operating Conditions

SYMBOL	PARAMETER	FIG.	MILITARY			COMMERCIAL			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage	N/A	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	N/A	-55		125	0		75	°C
t_{CLKWH}	Clock width HIGH	9,10	45			31			ns
t_{CLKWL}	Clock width LOW	9,10	34			18			ns
f_{CLK}	Clock frequency	N/A			12.5			20	MHz
t_{REQL}	Request LOW time	7,9,10	12			12			ns
t_{REQH}	Request HIGH time	9,10	25			25			ns
t_{MRL}	Master Reset width LOW	7	60			50			ns
t_{MRS}	Master Reset HIGH to WREQ LOW	7	25			25			ns
t_{PS}	Priority to non-sampling clock setup time	5,6	30			25			ns
t_{EWRQ}	WEN to WREQ setup time	7,9	0			0			ns
t_{ERRQ}	REN to RREQ setup time	10	0			0			ns
t_{WEH}	WREQ to WEN hold time	9	15			15			ns
t_{REH}	RREQ to REN hold time	10	15			15			ns
t_{WRQC}	WREQ LOW to sampling clock setup time	7,9	5*		30*	10*		25*	ns
t_{RRQC}	RREQ low to sampling clock setup time	10	5*		30*	10*		25*	ns

* The request window must be observed to guarantee proper operation, between min and max values are not allowed.

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITION		COMMERCIAL			UNIT
				MIN	TYP	MAX	
V_{IL}	Low-Level input voltage					0.8	V
V_A	High-level input voltage			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = –18 mA			–1.5	V
I_{IL}^*	Low-level input current	V_{CC} = MIN	V_I = 0.45 V			–250	µA
I_{IH}^*	High-level input current	V_{CC} = MIN	V_I = 2.4 V			50	µA
I_I	Maximum input current	V_{CC} = MIN	V_I = 5.5 V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN V_{CC} = MIN V_{CC} = MIN	I_{OL} (Address) = 16 mA I_{OL} (Control) = 8 mA I_{OL} (Flag) = 8 mA			0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN V_{CC} = MIN V_{CC} = MIN	I_{OH} (Address) = –3 mA I_{OH} (Control) = –3 mA I_{OH} (Flag) = –3 mA	2.4			V
I_{OS}^{**}	Output short-circuit current	V_{CC} = MAX	V_{OH} = 0 V	–20		–90	mA
I_{OZH} I_{OZL}	Off-state output currents	V_{CC} = MAX V_{CC} = MAX	V_O = 2.4 V V_O = 0.4 V			+40 –350†	µA
I_{CC}	Supply current	V_{CC} = MAX				350	mA

*Except TEST pin, which should always be grounded.

**No more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

†I_{OZL} is Output leakage current plus I_{IL}.

Switching Characteristics

SYMBOL	PARAMETER	FIG.	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
t_{MRWH}	Master Reset LOW to WRDY HIGH	7			50			50	ns
t_{MRRL}	Master Reset LOW to RRDY LOW	7			50			50	ns
t_{MREF}	Master Reset LOW to EMPTY flag HIGH	7			50			50	ns
t_{MRAL}	Master Reset LOW to Almost HIGH	7			60			55	ns
t_{MRWRC}	Master Reset LOW to WREGCK HIGH	7			40			35	ns
t_{MRRRC}	Master Reset LOW to RREGCK HIGH	7			40			35	ns
t_{MRWBH}	Master Reset LOW to W HIGH	7			50			50	ns
t_{AV}	Clock to address valid	7,9,10,12,13			50			40	ns
t_{ANV}	Clock to address not valid	7,9,10,12,13	15			15			ns
t_{ANVAV}	Address not valid to address valid	7,9,10,12,13			20			12	ns
t_{CWRL}	Clock to WRDY LOW	7,9			35			35	ns
t_{CWRH}	Clock to WRDY HIGH	7,9			40			35	ns
t_{CWRGL}	Clock to WREGCK LOW	7,9			35			30	ns
t_{CWRGH}	Clock to WREGCK HIGH	7,9			35			30	ns
t_{CWL}	Clock to W LOW	7,9			50			45	ns
t_{CWH}	Clock to W HIGH	7,9			25			25	ns
t_{AS}	Address valid to W LOW	7,9	0		12	0		12	ns
t_{WR}	Address not valid to W HIGH	7,9			0			0	ns
t_{WP}	W pulse width LOW at f_{CLK}(max)	9,13	100*			50**			ns
t_{PW}	W pulse width HIGH	4,13	12		30	12		25	ns
t_{WHAV}	W HIGH to address valid	4,9,13			35			25	ns
t_{WHWRCH}	W HIGH to WREGCK HIGH	4,13			25			18	ns
t_{CRRL}	Clock to RRDY LOW	10			35			30	ns
t_{CRRH}	Clock to RRDY HIGH	7,10			40			35	ns
t_{CRRGL}	Clock to RREGCK LOW	7,10			35			30	ns
t_{CRRGH}	Clock to RREGCK HIGH	7,10,12			35			30	ns
t_{ARRH}	Address valid to RREGCK HIGH at f_{CLK}(max)	10	110*			60**			ns
t_{ANRRH}	Address not valid to RREGCK HIGH	10			10			8	ns
t_{CE}	Clock to EMPTY flag	7,9,10			40			35	ns
t_{CF}	Clock to FULL flag	9,10			40			35	ns
t_{CHF}	Clock to Half-Full flag	9,10			50			45	ns
t_{CA}	Clock to Almost flag	9,10			60			55	ns
t_{LZ}	Address bit LOW to Hi-Z	15			30			30	ns
t_{HZ}	Address bit HIGH to Hi-Z	15			30			30	ns
t_{ZL}	Address bit Hi-Z to LOW	15			30			30	ns
t_{ZH}	Address bit Hi-Z to HIGH	15			30			30	ns

* f_{CLK}(max) = 12.5 MHz (Military).
** f_{CLK}(max) = 20 MHz (Commercial).

Standard Test Load

CL = 30 pF
RL = 600 Ω
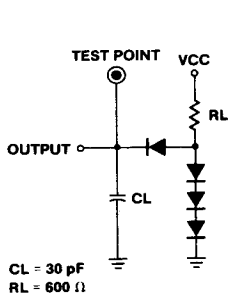
**Load Circuit
for Bi-State Outputs
(Control and Flag Outputs)**

CL = 5 pF (THREE-STATE)
30 pF (NORMAL OPERATION)
RL = 300 Ω
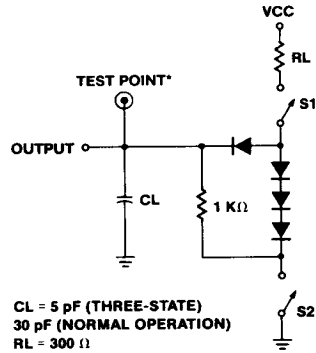
**Load Ciruit
for Three-State Outputs
(Address Outputs)**
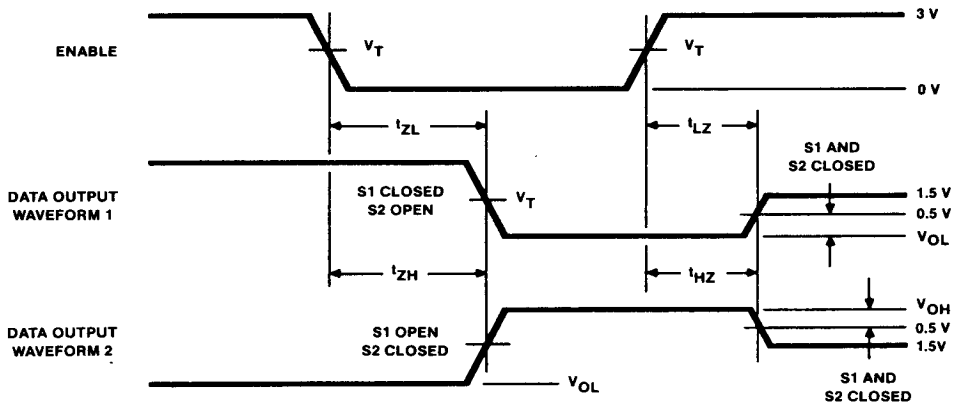
Waveform 1 is for an output with internal conditions such that the output is LOW except when disabled.
Waveform 2 is for an output with internal conditions such that the output is HIGH except when disabled.

Figure 15. Enable and Disable Timing

Notes: A. C_L includes probe and jig capacitance.
   B. All diodes are 1N916 or 1N306A.
   C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
      Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
   D. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
   E. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz. Z_{out} = 50 Ω and t_R ≤ 2.5 ns t_F ≤ 2.5 ns.
   F. When measuring propagation delay times of three-state outputs, switches S1 and S2 are closed.