

6-bit 40MSPS High Speed D/A Converter

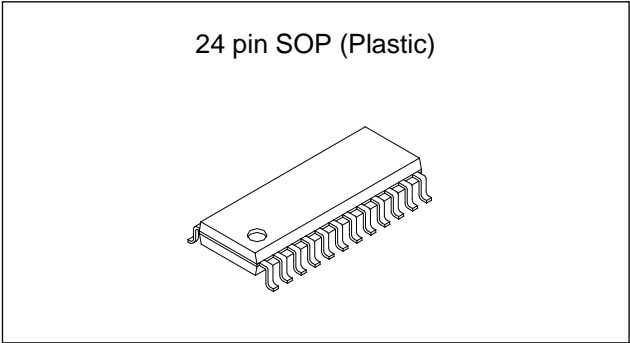
Description

The CXD1170M is a 6-bit 40MHz high speed D/A converter. The adoption of a current output system reduces power consumption to 80mW (200Ω load at 2Vp-p output).

This IC is suitable for digital TV and graphic display applications.

Features

- Resolution 6-bit
- Max. conversion speed 40MSPS
- Non linearity error within $\pm 0.1\text{LSB}$
- Low glitch noise
- TTL CMOS compatible input
- +5V single power supply
- Low power consumption 80mW (200Ω load at 2Vp-p output)



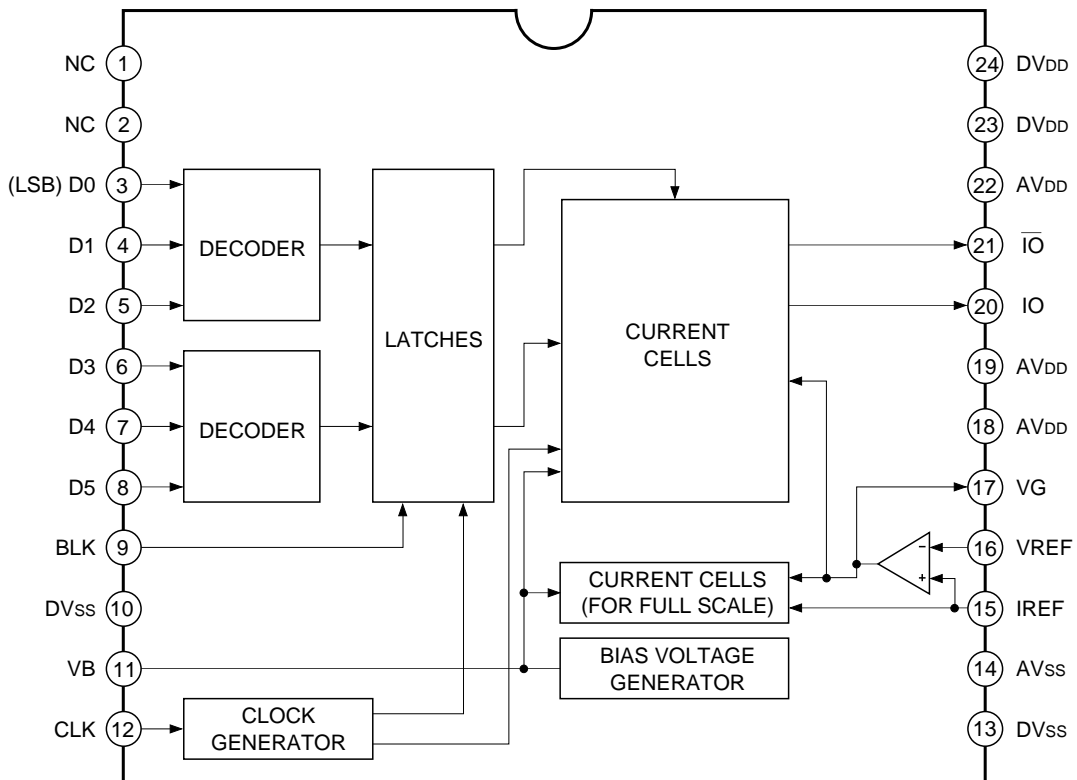
Structure

Silicon gate CMOS IC

Function

6-bit 40MHz D/A converter

Block Diagram and Pin Configuration



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Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	V _{DD}	7	V
• Input voltage	V _{IN}	V _{DD} to V _{SS}	V
• Output current	I _{OUT}	15	mA
• Storage temperature	T _{stg}	-55 to +150	°C

Recommended Operating Conditions

• Supply voltage	AV _{DD} , AV _{SS}	4.75 to 5.25	V
	DV _{DD} , DV _{SS}	4.75 to 5.25	V
• Reference input voltage	V _{REF}	2.0	V
• Clock pulse width	T _{pw1}	12.5 (Min)	ns
	T _{pw0}	12.5 (Min)	ns
• Operating temperature	T _{opr}	-20 to +75	°C

Pin Description and I/O Pins Equivalent Circuit

No.	Symbol	Equivalent circuit	Description
3 to 8	D0 to D5		Digital input
9	BLK		Blanking pin No signal at "H" (Output 0V) Output condition at "L"
11	VB		Connect a capacitor of about 0.1μF
12	CLK		Clock pin Moreover all input pins are TTL-CMOS compatible
10, 13	DV _{SS}		Digital GND
14	AV _{SS}		Analog GND

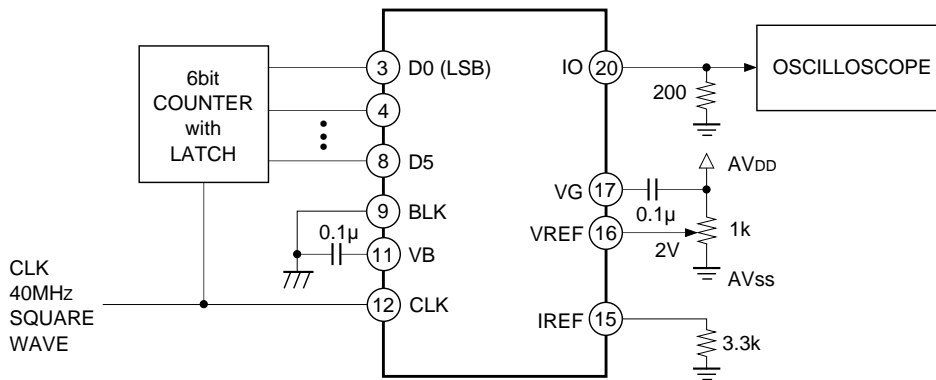
No.	Symbol	Equivalent circuit	Description
15	IREF		Connect a resistance 16 times "16R" that of output resistance value "R"
16	VREF		Set full scale output value
17	VG		Connect a capacitor of about 0.1μF
18, 19, 22	AVDD		Analog VDD
20	IO		Current output pin Voltage output can be obtained by connecting a resistance
21	\overline{IO}		Inverted current output pin Normally dropped to analog GND
23, 24	DVDD		Digital VDD

Electrical Characteristics

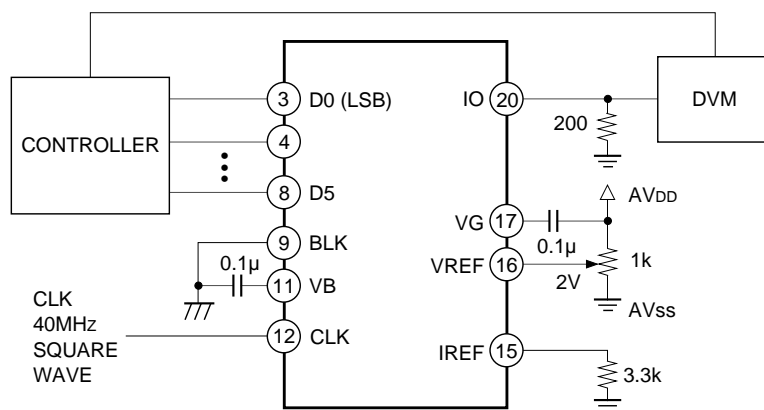
(f_{CLK} = 40MHz, V_{DD} = 5V, R_{OUT} = 200Ω, V_{REF} = 2.0V, T_a = 25°C)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Resolution	n			6		bit
Maximum conversion speed	f _{MAX}				40	MSPS
Minimum conversion speed	f _{MIN}		0.5			MHz
Linearity error	E _L		-0.3		0.5	LSB
Differential linear error	E _D		-0.1		0.1	LSB
Full scale output voltage	V _{FS}		1.85	1.95	2.05	V
Full scale output current	I _{FS}			10	15	mA
Offset output voltage	V _{OS}				1	mV
Power supply current	I _{DD}	14.3MHz, at COLOR BAR DATA input	13	14.5	16	mA
Digital input current	High level	I _{IH}			5	μA
	Low level	I _{IL}	-5			μA
Setup time	t _S		5			ns
Hold time	t _H		10			ns
Propagation delay time	t _{PD}			10		ns
Glitch energy	GE	R _{OUT} = 75Ω		30		pV-s

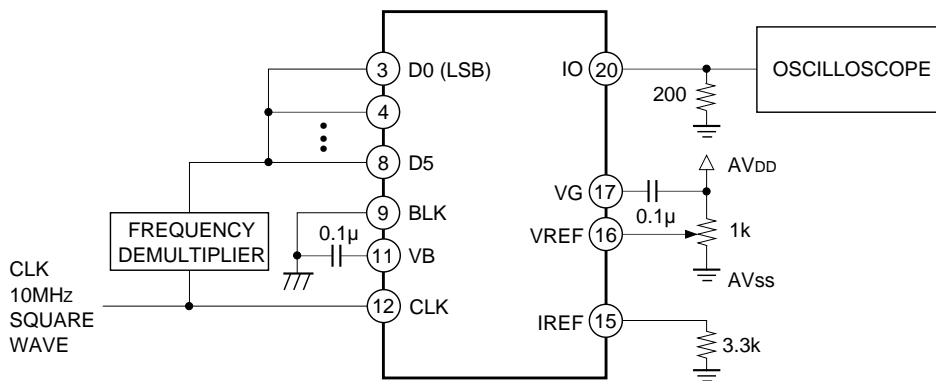
Maximum conversion speed test circuit



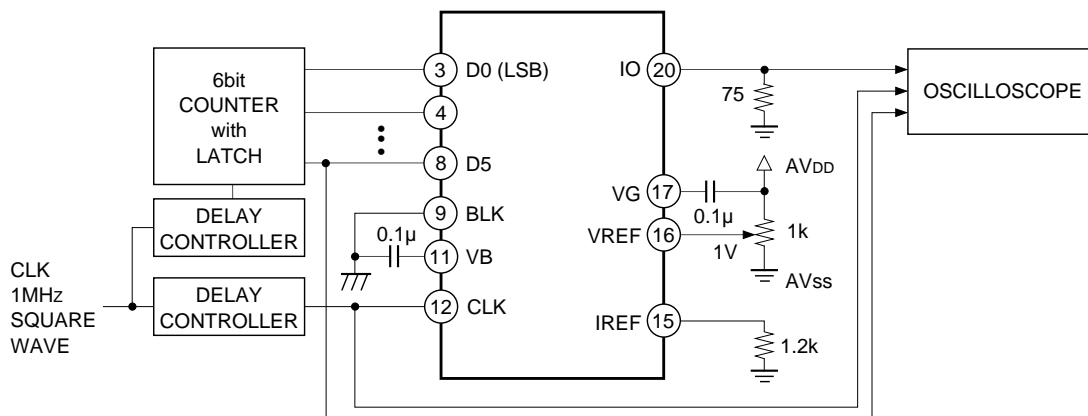
DC characteristics test circuit



Propagation delay time test circuit

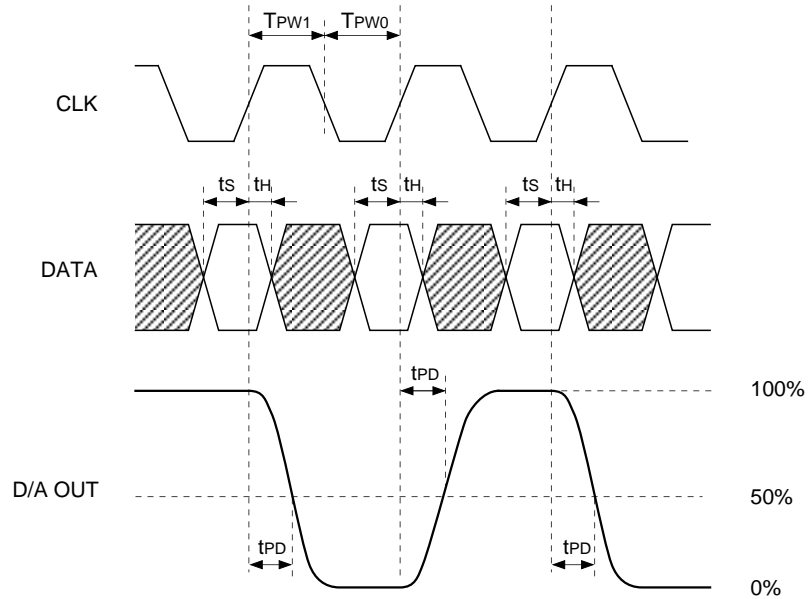


Setup hold time and glitch energy test circuit

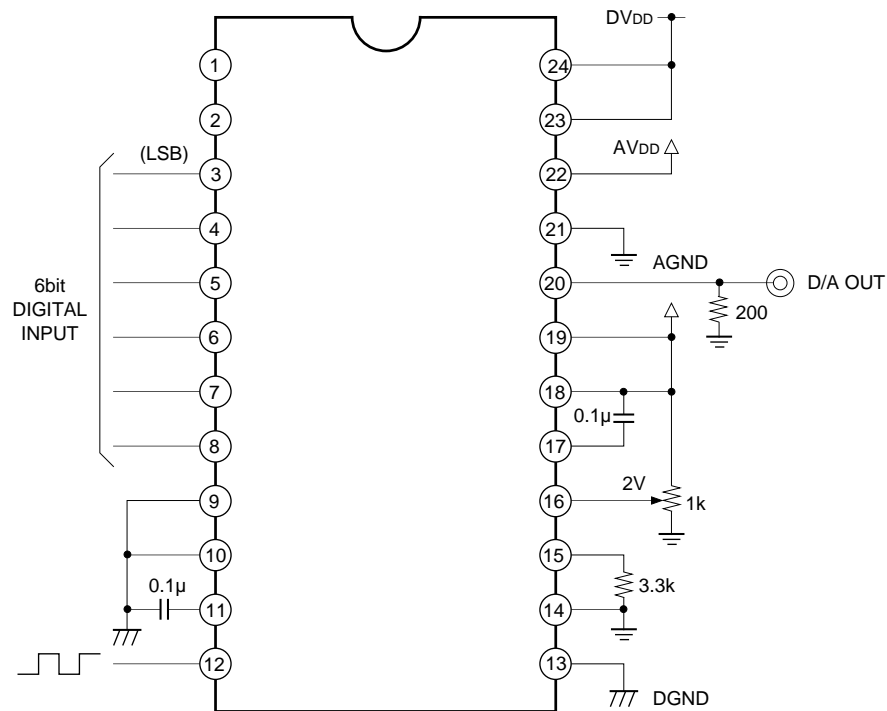


Operation

Timing Chart



Application Circuit



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I/O Chart (when full scale output voltage at 2.00V)

Input code		Output voltage
MSB	LSB	
1	1 1 1 1 1 1	2.0V
	⋮	
1	0 0 0 0 0 0	1.0V
	⋮	
0	0 0 0 0 0 0	0V

Notes on Operation

- How to select the output resistance

The CXD1170M is a D/A converter of the current output type. To obtain the output voltage connect the resistance to IO pin. For specifications we have:

Output full scale voltage $V_{FS} = \text{less than } 2.0 \text{ [V]}$

Output full scale current $I_{FS} = \text{less than } 15 \text{ [mA]}$

Calculate the output resistance value from the relation of $V_{FS} = I_{FS} \times R$. Also, 16 times resistance of the output resistance is connected to reference current pin I_{REF} . In some cases, however, this turns out to be a value that does not actually exist. In such a case a value close to it can be used as a substitute. Here please note that V_{FS} becomes $V_{FS} = V_{REF} \times 16R/R'$. R is the resistance connected to IO while R' is connected to I_{REF} . Increasing the resistance value can curb power consumption. On the other hand glitch energy and data settling time will inversely increase. Set the most suitable value according to the desired application.

- Phase relation between data and clock

To obtain the expected performance as a D/A converter, it is necessary to set properly the phase relation between data and clock applied from the exterior. Be sure to satisfy the provisions of the setup time (t_s) and hold time (t_H) as stipulated in the Electrical Characteristics.

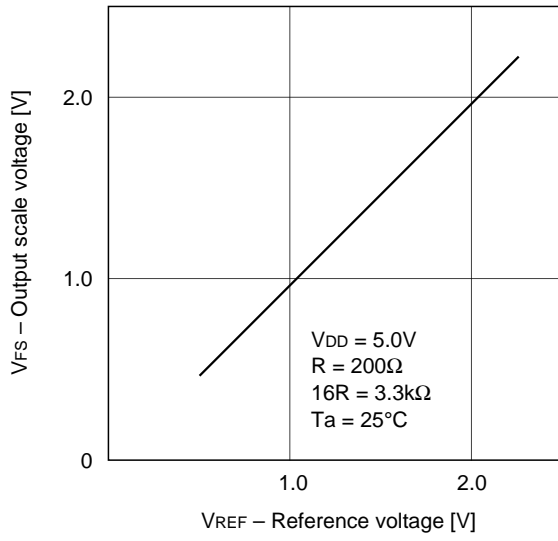
- V_{DD} , V_{SS}

To reduce noise effects separate analog and digital systems in the device periphery. For V_{DD} pins, both digital and analog, bypass respective GNDs by using a ceramic capacitor of about $0.1\mu\text{F}$, as close as possible to the pin.

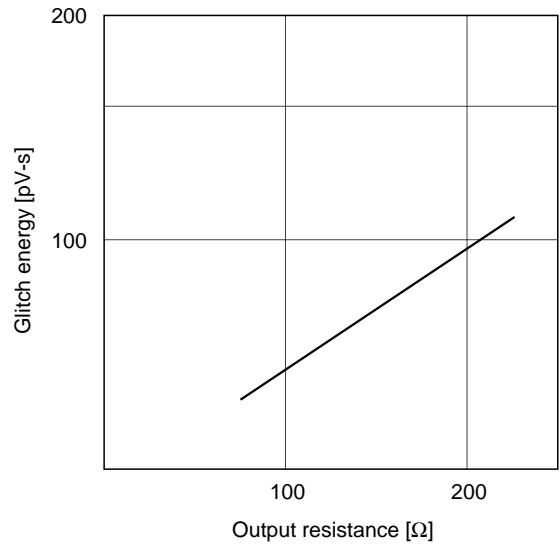
- Latch up

AV_{DD} and DV_{DD} have to be common at the PCB power supply source. This is to prevent latch up due to voltage difference between AV_{DD} and DV_{DD} pins when power supply is turned ON.

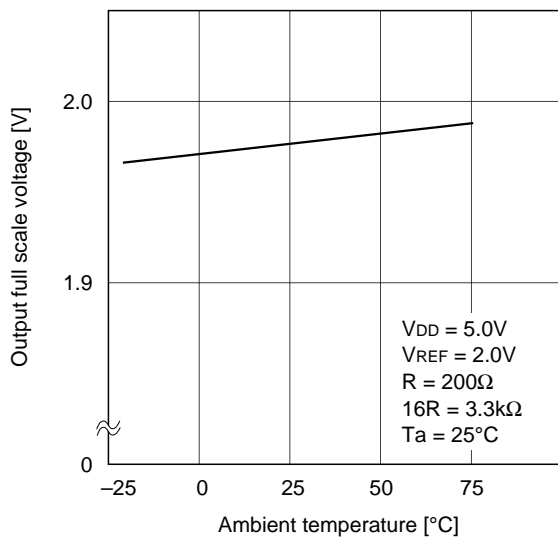
Output full scale voltage vs. Reference voltage



Output resistance vs. Glitch energy



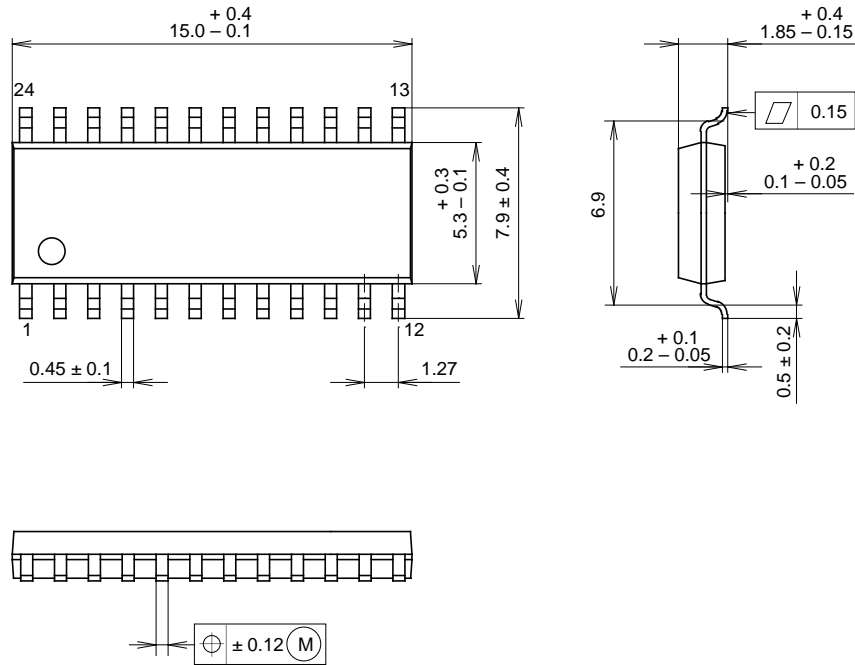
Output full scale voltage vs. Ambient temperature



Package Outline

Unit: mm

24PIN SOP (PLASTIC)



PACKAGE STRUCTURE

SONY CODE	SOP-24P-L01
EIAJ CODE	*SOP024-P-0300-A
JEDEC CODE	—

MOLDING COMPOUND	EPOXY/PHENOL RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY / 42ALLOY
PACKAGE WEIGHT	0.3g