SONY

CXD1171M

8-bit 40MSPS High Speed D/A Converter

Description

The CXD1171M is a 8-bit 40 MHz high speed D/A converter. The adoption of a current output system reduces power consumption to 80 mW (200 Ω load at 2 Vp-p output).

This IC is suitable for digital TV and graphic display applications.

Features

- Resolution 8-bit
- Max. conversion speed 40MSPS
- Non linearity error within ±0.25 LSB
- Low glitch noise
- TTL CMOS compatible input
- +5 V single power supply
- Low power consumption 80 mW
  (200 Ω load at 2 Vp-p output)

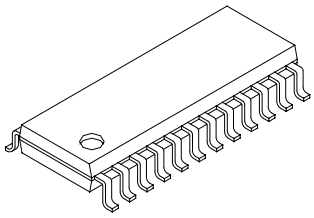
Function

8-bit 40 MHz D/A converter

Structure

Silicon gate CMOS IC

24 pin SOP (Plastic)



Absolute Maximum Ratings (Ta=25 °C)

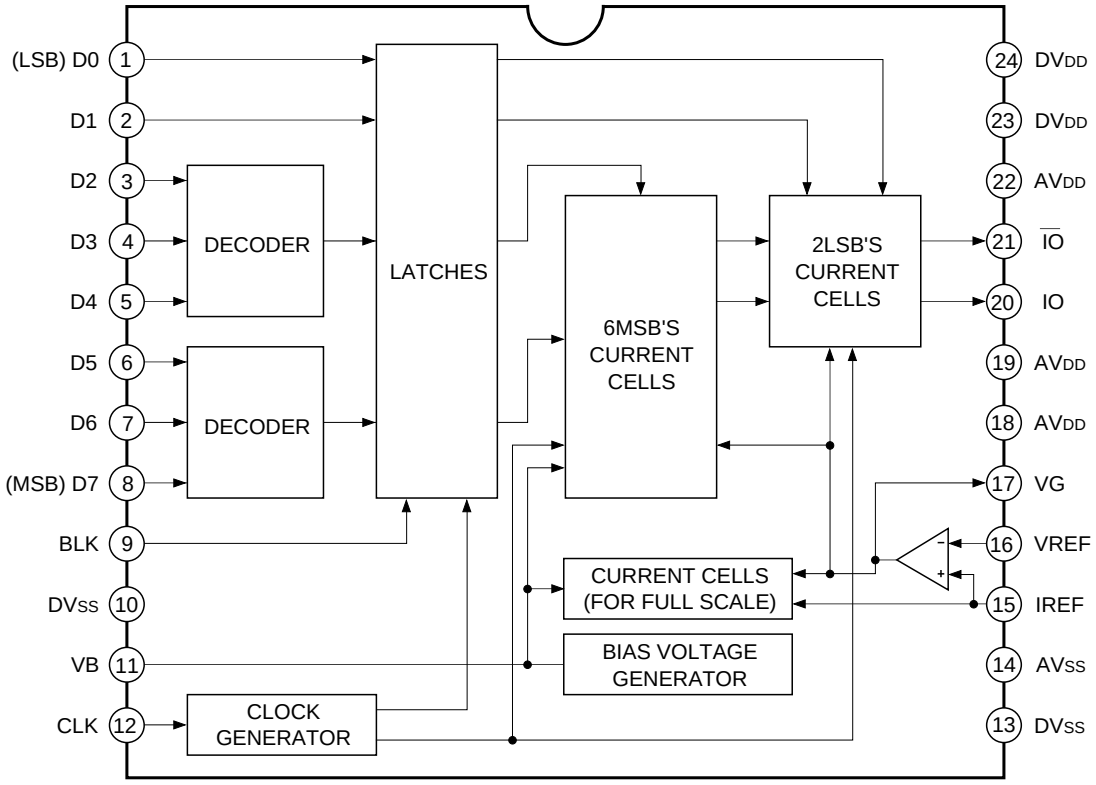
• Supply voltage	AV_{DD}, DV_{DD}	7	V
• Input voltage (All pins)	V_{IN}	V_{DD} +0.5 to V_{SS} –0.5	V
• Output current	I_{OUT}	15	mA
• Storage temperature	Tstg	–55 to +150	°C

Recommended Operating Conditions

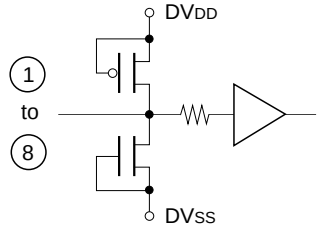
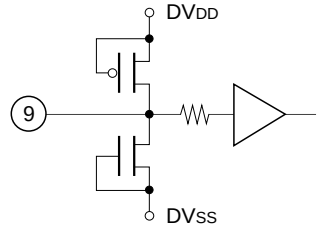
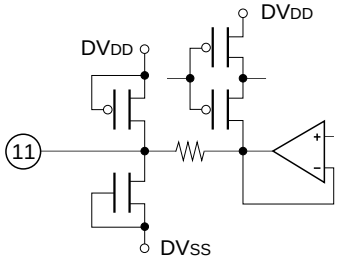
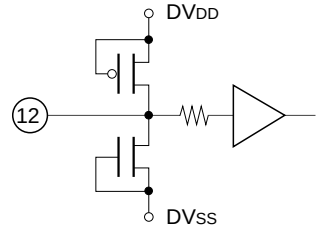
• Supply voltage	AV_{DD}, AV_{SS}	4.75 to 5.25	V
	DV_{DD}, DV_{SS}	4.75 to 5.25	V
• Reference input voltage	V_{REF}	2.0	V
• Clock pulse width	Tpw_1,Tpw_0	11.2 ns (min) to 1.1 µs (max)	
• Operating temperature	Topr	–40 to +85	°C

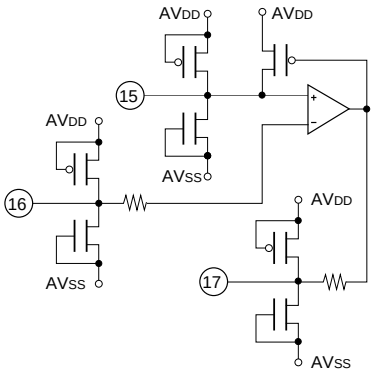
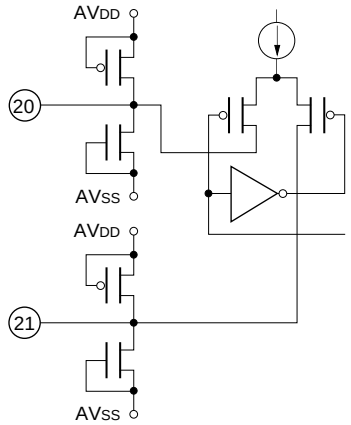
E89X38G13-PS

Block Diagram and Pin Configuration



Pin Description and I/O Pins Equivalent Circuit

No.	Symbol	I/O	Equivalent circuit	Description
1 to 8	D0 to D7	I		Digital input. D0 (LSB) to D7 (MSB) D0 and D1 have a pull-down resistor.
9	BLK	I		Blanking input. This is synchronized with the clock signal. No signal at “H” (Output 0 V). Output condition at “L”.
11	VB	O		Connect a capacitor of about 0.1 µF.
12	CLK	I		Clock input.
10, 13	DVSS	—		Digital ground.
14	AVSS	—		Analog ground.

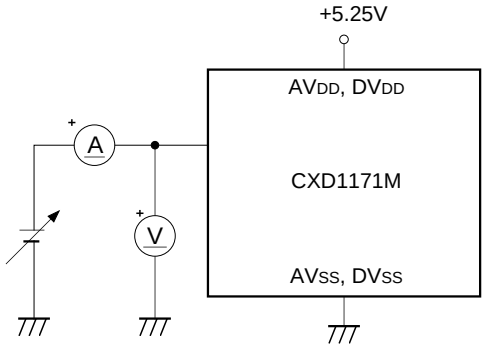
No.	Symbol	I/O	Equivalent circuit	Description
15	IREF	O		Connect a resistor "RIR" 16 times against the output resistance value "ROUT" connected to Pin 20 (IO).
16	VREF	I		Set full-scale output value.
17	VG	O		Connect a capacitor of about 0.1 µF.
18, 19, 22	AVDD	—		Analog power supply.
20	IO	O		Current output. Voltage output can be obtained by connecting a resistance.
21	$\overline{IO}$			Inverted current output. Normally connected to analog GND.
23, 24	DVDD	—		Digital power supply.

Electrical Characteristics (F_{CLK}=40 MHz, AV_{DD}=DV_{DD}=5 V, R_{OUT}=200 Ω, V_{REF}=2.0 V, Ta=25 °C)

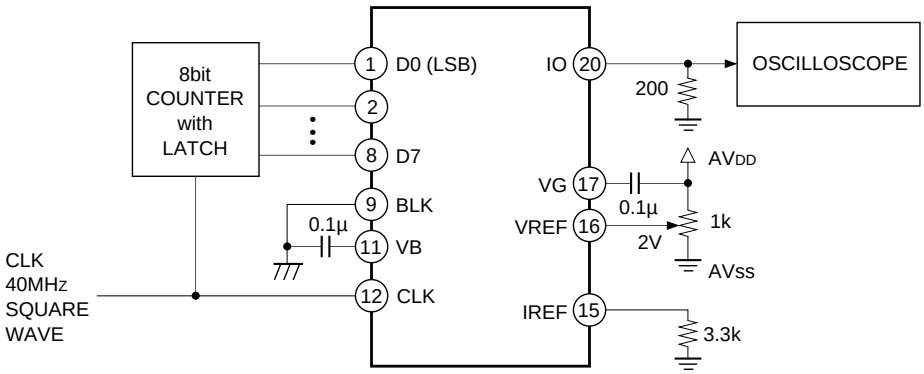
Item	Symbol	Measurement conditions		Min.	Typ.	Max.	Unit
Resolution	n				8		bit
Conversion speed	F_{CLK}	AV_{DD}=DV_{DD}=4.75 to 5.25 V Ta=–40 to 85 °C		0.5		40	MSPS
Integral non-linearity error	E_L	Endpoint		–0.5		1.3	LSB
Differential non-linearity error	E_D			–0.25		0.25	LSB
Output full-scale voltage	V_{FS}			1.9	2.0	2.1	V
Output full-scale current	I_{FS}				10	15	mA
Output offset voltage	V_{OS}	When D0 to D7=00000000 input				1	mV
Glitch energy	GE	R_{OUT}=75 Ω			30		pV·s
Supply current	I_{DD}	When 14.3 MHz color bar data input		13	14.5	16	mA
Analog input resistance	R_{IN}	V_{REF}		1			MΩ
Input capacitance	C_I					9	pF
Digital input voltage	V_{IH}	AV_{DD}=DV_{DD}=4.75 to 5.25 V		2.4			V
	V_{IL}	Ta=–20 to +75 °C				0.8	
Digital input current	I_{IH} I_{IL}	AV_{DD}=DV_{DD}=4.75 to 5.25 V Ta=–20 to +75 °C	D0, D1	–5		240	µA
			D2 to 7, BLK, CLK	–5		5	
Setup time	t_S	R_{OUT}=75 Ω		5			ns
Hold time	t_H	R_{OUT}=75 Ω		10			ns
Propagation delay time	t_{PD}				10		ns

Electrical Characteristics Measurement Circuit

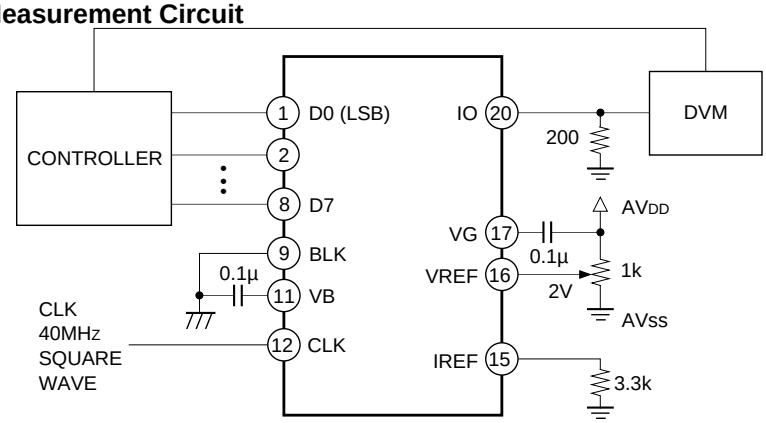
Analog Input Resistance
Digital Input Current } **Measurement Circuit**



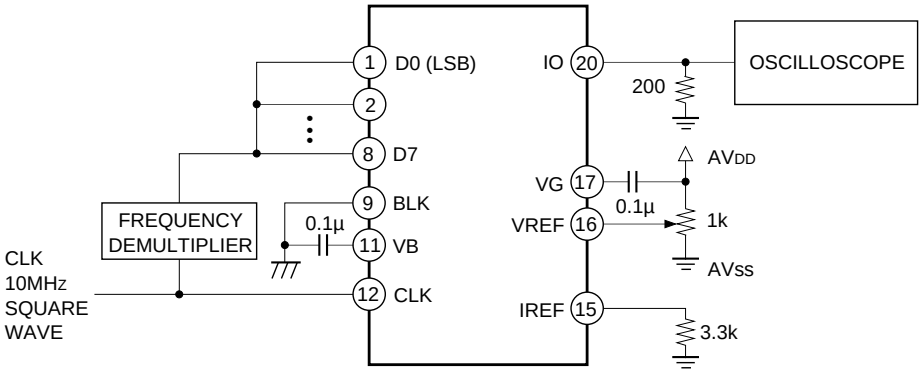
Maximum Conversion Speed Measurement Circuit



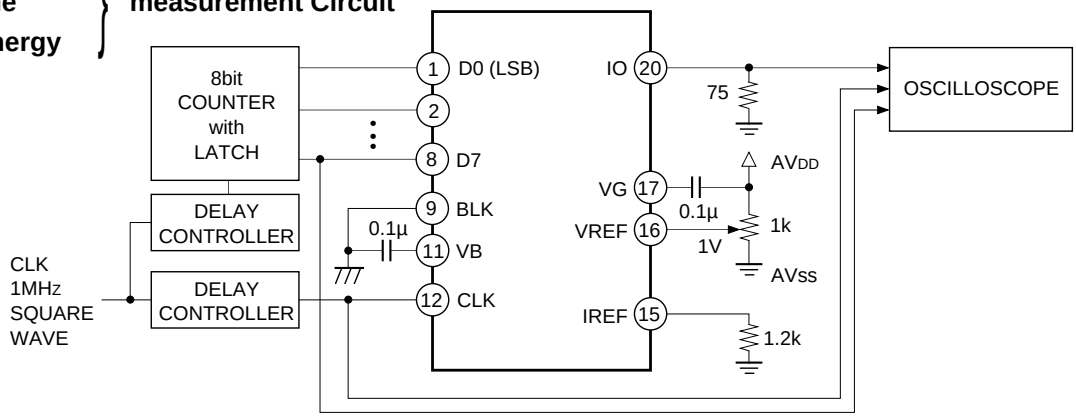
DC Characteristics Measurement Circuit



Propagation Delay Time Measurement Circuit

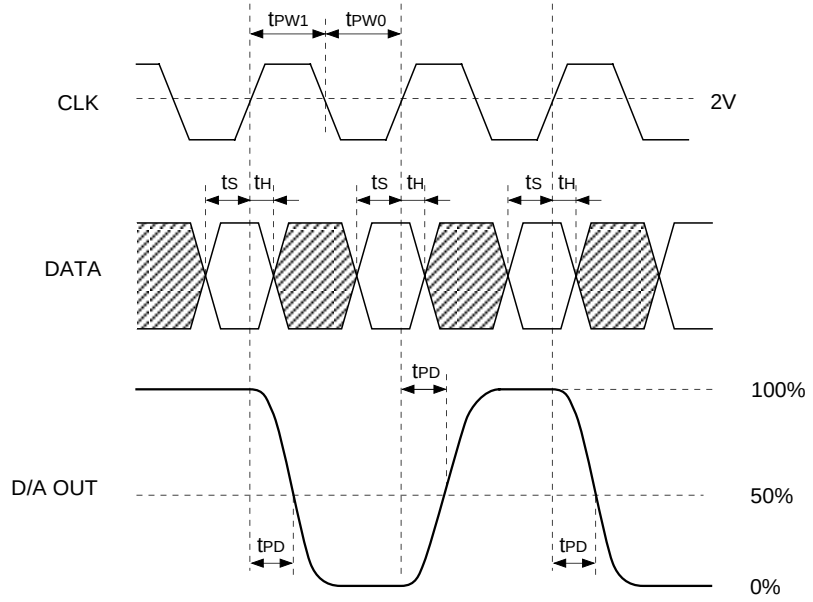


Setup Time / Hold Time / Glitch Energy measurement Circuit



Operation

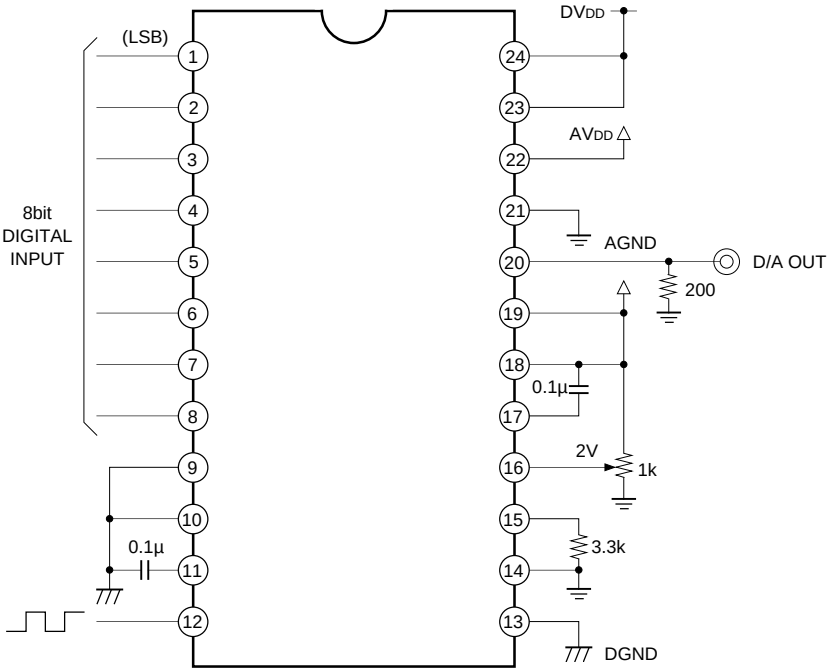
Timing Chart



I/O Chart (when full-scale output voltage at 2.00 V)

Input code	Output voltage
MSB LSB	
1 1 1 1 1 1 1 1	2.0 V
:	
1 0 0 0 0 0 0 0	1.0 V
:	
0 0 0 0 0 0 0 0	0 V

Application Circuit



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Notes on Operation

- How to select the output resistance

  The CXD1171M is a D/A converter of the current output type. To obtain the output voltage connect the resistance to the current output pin IO. For specifications we have:

  Output full scale voltage V_{FS} = 1.9 to 2.1 [V]

  Output full scale current I_{FS} = less than 15 [mA]

  Calculate the output resistance value from the relation of $V_{FS} = I_{FS} \times R_{OUT}$. Also, 16 times resistance of the output resistance is connected to reference current pin IREF. In some cases, however, this turns out to be a value that does not actually exist. In such a case a value close to it can be used as a substitute. Here please note that V_{FS} becomes $V_{FS} = V_{REF} \times 16R_{OUT}/R_{IR}$. R_{OUT} is the resistance connected to IO while R_{IR} is connected to IREF. Increasing the resistance value can curb power consumption. On the other hand glitch energy and data settling time will inversely increase. Set the most suitable value according to the desired application.

- Phase relation between data and clock

  To obtain the expected performance as a D/A converter, it is necessary to set properly the phase relation between data and clock applied from the exterior. Be sure to satisfy the provisions of the setup time (t_S) and hold time (t_H) as stipulated in the Electrical Characteristics.

- Power supply and ground

  To reduce noise effects separate analog and digital systems in the device periphery. For the power supply pins, both digital and analog, bypass respective grounds by using a ceramic capacitor of about 0.1 µF, as close as possible to the pin.

- Latch up

  AV_{DD} and DV_{DD} have to be common at the PCB power supply source. This is to prevent latch up due to voltage difference between AV_{DD} and DV_{DD} pins when power supply is turned ON.

- $\overline{IO}$ pin

  The $\overline{IO}$ pin is the inverted current output pin described in the Pin Description. The sum of the currents output from the $\overline{IO}$ pin and the $\overline{IO}$ pin becomes the constant value for any input data.

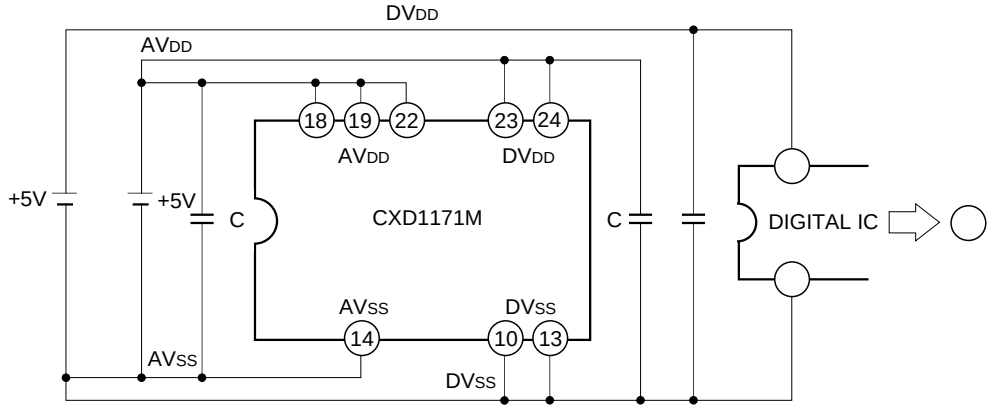
  However, the performances such as the linearity error of the $\overline{IO}$ pin output current is not guaranteed.

Latch Up Prevention

The CXD1171M is a CMOS IC which requires latch up precautions. Latch up is mainly generated by the lag in the voltage rising time of AV_{DD} (Pins 18, 19 and 22) and DV_{DD} (Pins 23 and 24), when power supply is ON.

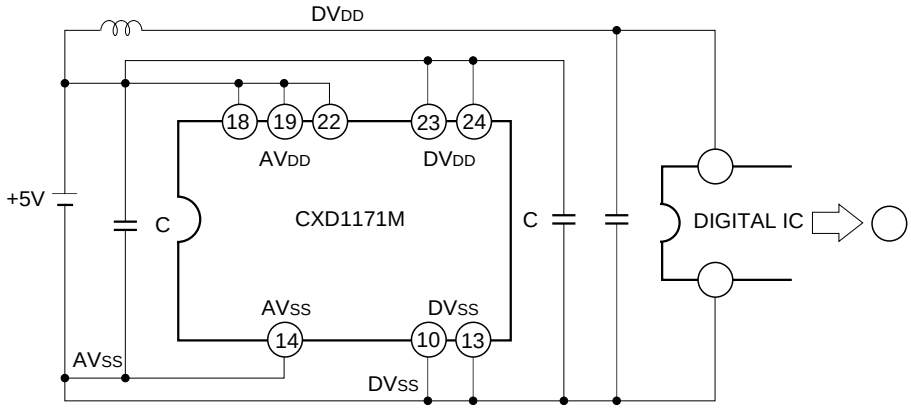
1. Correct usage

a. When analog and digital supplies are from different sources

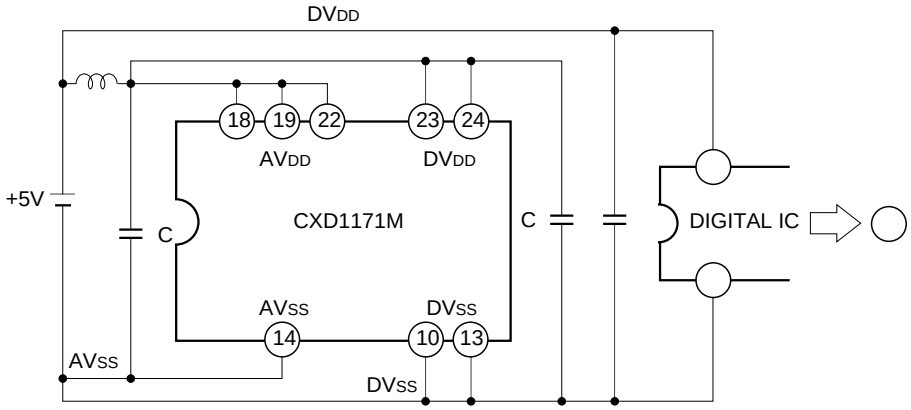


b. When analog and digital supplies are from a common source

(i)

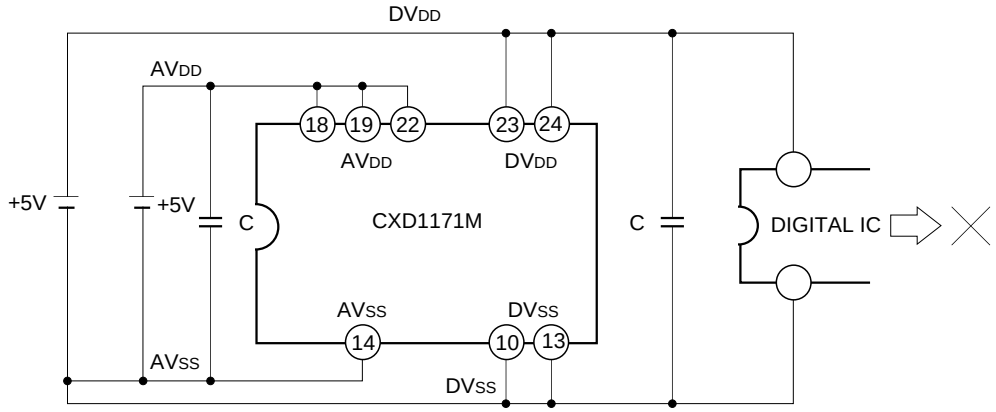


(ii)



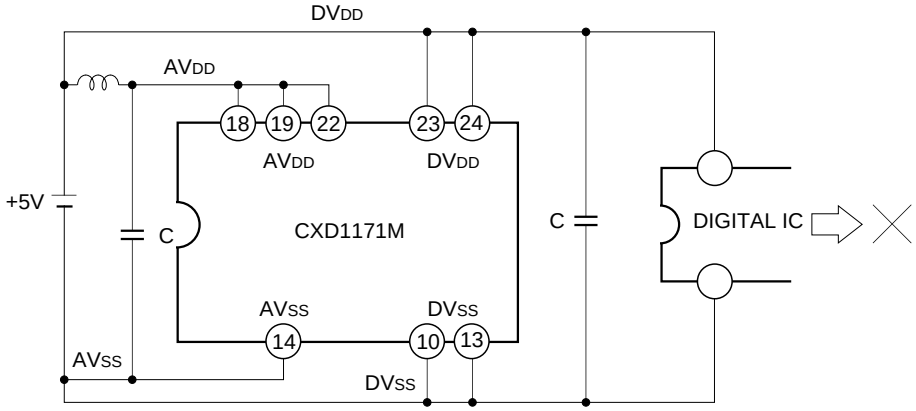
2. Example when latch up easily occurs

a. When analog and digital supplies are from different sources

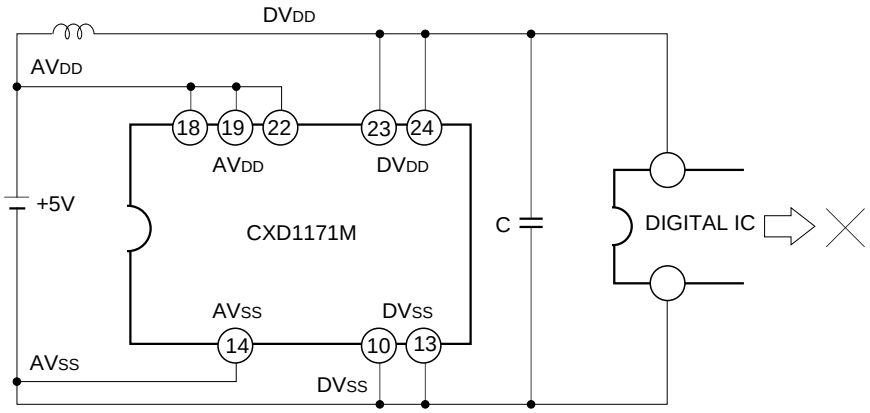


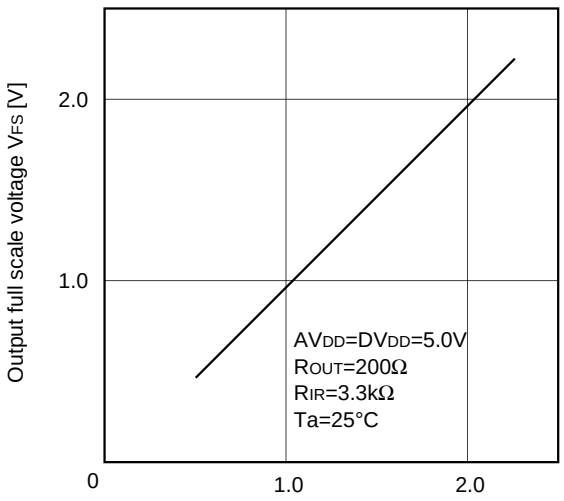
b. When analog and digital supplies are from common source

(i)

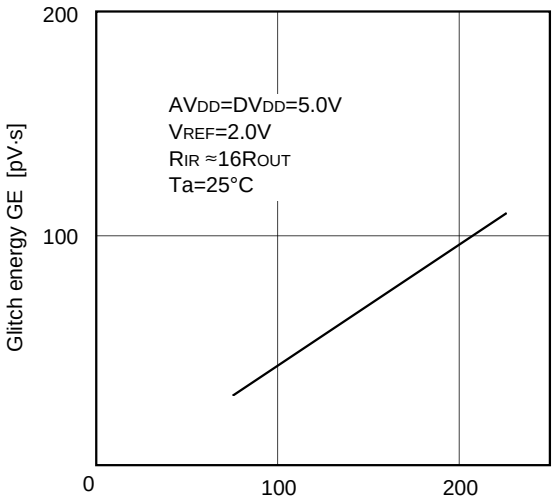


(ii)

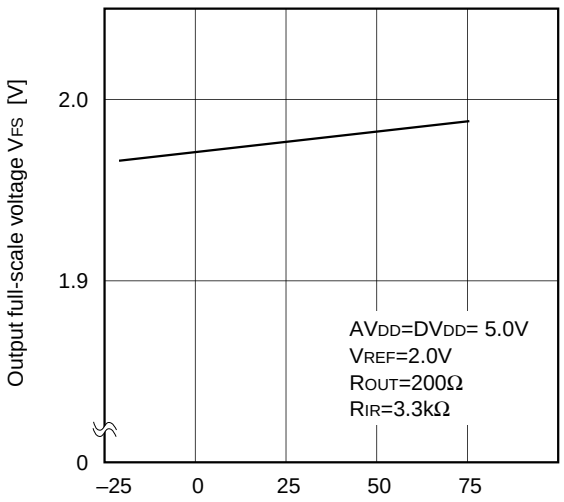




Reference voltage vs. Output full scale voltage



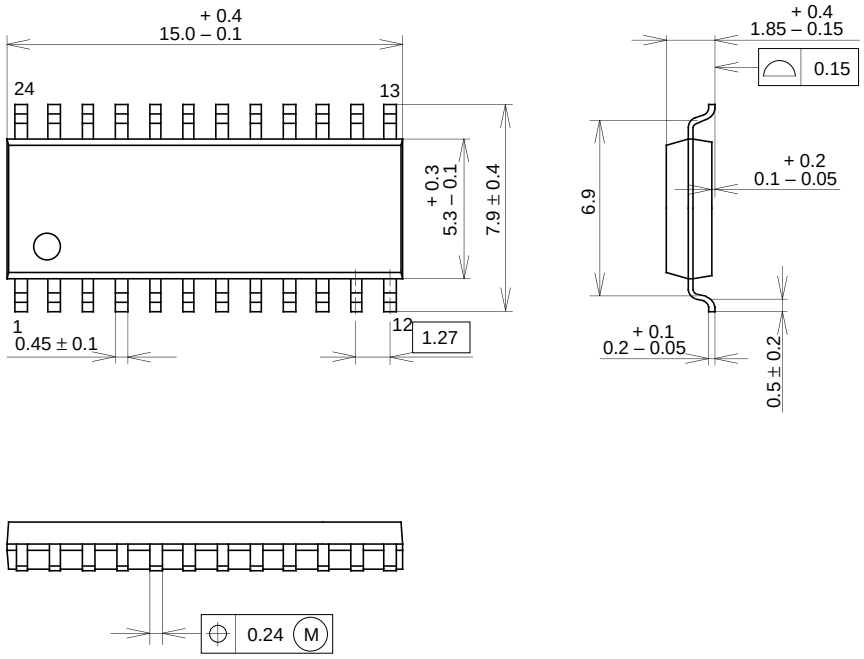
Output resistance vs. Glitch energy



Ambient temperature vs. Output full scale voltage

Package Outline Unit : mm

24PIN SOP (PLASTIC)



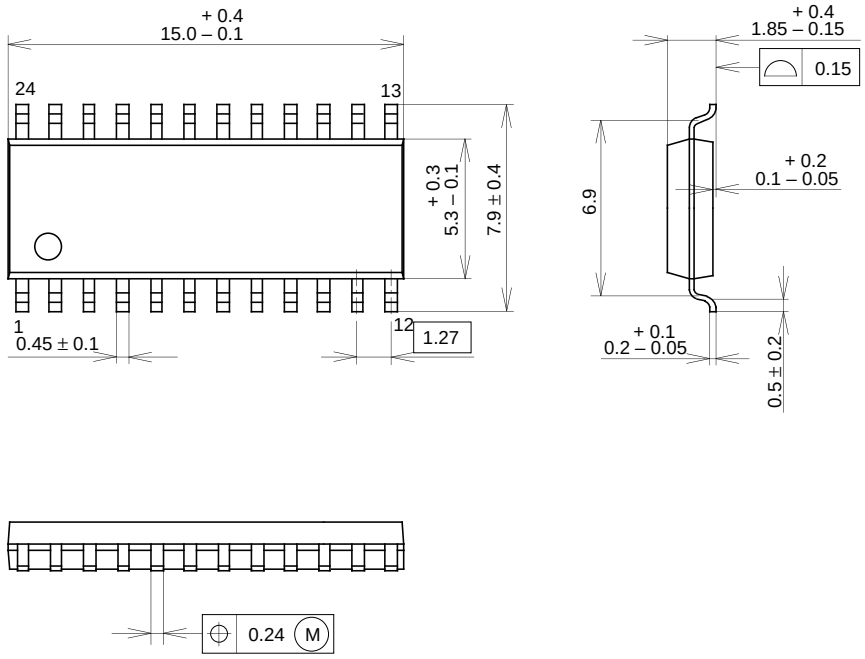
SONY CODE	SOP-24P-L01
EIAJ CODE	SOP024-P-0300
JEDEC CODE	————

PACKAGE STRUCTURE

MOLDING COMPOUND	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	0.3g

Package Outline Unit : mm

24PIN SOP (PLASTIC)



PACKAGE STRUCTURE

MOLDING COMPOUND	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	0.3g

SONY CODE	SOP-24P-L01
EIAJ CODE	SOP024-P-0300
JEDEC CODE	————

LEAD SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	COPPER ALLOY
LEAD TREATMENT	Sn-Bi 2.5%
LEAD TREATMENT THICKNESS	5-18µm