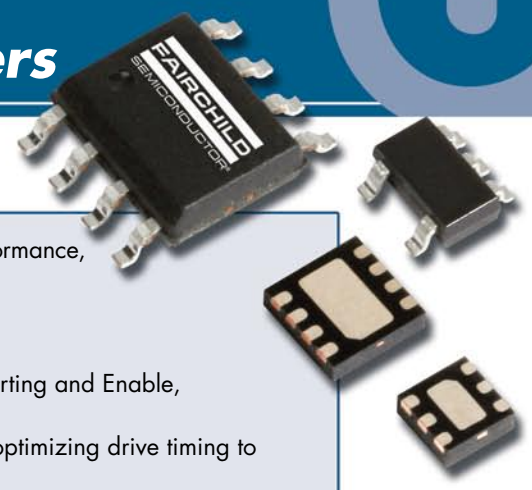
FAIRCHILD
SEMICONDUCTOR®

High-Speed, Low-Side Gate Drivers



Fairchild's Offering

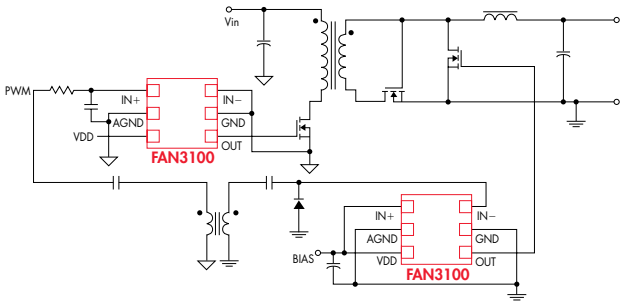
The FAN3000 series low-side gate drivers offer an unequaled combination of higher performance, smaller size, and more input options for driving N-channel power MOSFETs and IGBTs:

- Industry's smallest packages (2×2 and 3×3mm MLP)
- Choice of TTL or CMOS input thresholds for all devices for best compatibility
- 2 inputs for each channel for design flexibility: either Dual-input (+ and − logic), Inverting and Enable, or Non-inverting and Enable
- Short and well-controlled time delays for 1MHz+ switching, paralleling drivers, and optimizing drive timing to maximize efficiency
- Part of Fairchild's total silicon solution for power supplies, backed by the Global Power Resource™, a worldwide network of power supply design experts

40 different devices provide choices of 2A, 4A or 9A current ratings in single or dual-channel versions. In addition to the specifications below, these drivers deliver fast switching and accurate timing to maximize efficiency in high frequency power converter designs.

- MillerDrive™ architecture for the output stage, a bipolar–MOSFET combination that provides the highest current during the Miller plateau of the MOSFET switching transition to minimize switching losses
- Fail-Safe Inputs to hold the output low if an input signal is absent
- Under-Voltage Lockout for predictable startup
- "Enable" inputs which default to "ON" if not connected
- Industry-standard pin-outs
- Thermal pads for heat removal (MLP packages)
- Lead(Pb)-free finish

Forward Converter with Hybrid Synchronous Rectifier



Typical Applications

- Switch-Mode Power Supplies
- Synchronous Rectifier Circuits
- Line Drivers
- DC–DC Power Converters
- Digital Audio Amplifiers
- Any switching power MOSFET or IGBT

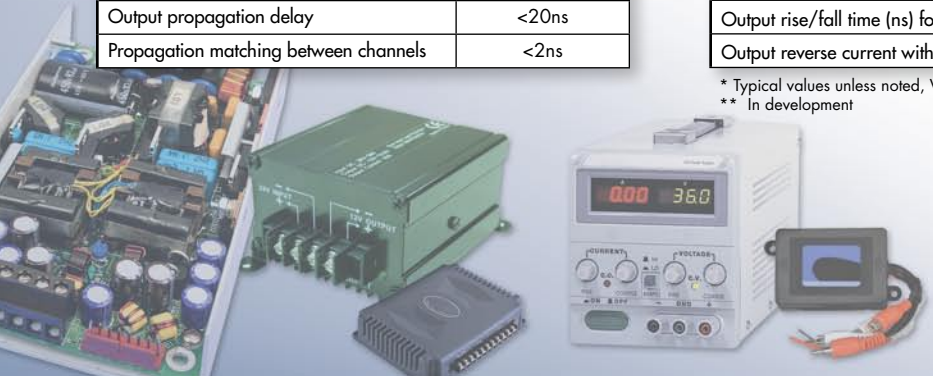
Specifications for All*

Parameter	Value
V_{DD} to GND, abs max	20V
Recommended V_{DD} range	4.5V – 18V
Junction Temperature, abs max	150°C
Recommended ambient temperature	–40°C – 125°C
UVLO Turn-ON voltage	4V
Output propagation delay	<20ns
Propagation matching between channels	<2ns

Specifications by Current Rating*

Parameter	2A	4A	9A**
Mid-voltage sink current/channel (Amps)	2.5	4.3	9
Mid-voltage source current/channel (Amps)	1.7	2.8	6
Peak sink current/channel (Amps)	3	5	12
Peak source current/channel (Amps)	3	5	10
Quiescent current, inputs disconnected (mA)	0.7	0.7	1.0
Output rise/fall time (ns) for [load capacitance, nF]	13/9 [1]	12/9 [2.2]	20/18 [10]
Output reverse current withstand (mA)	500	500	1500

* Typical values unless noted, VDD = 12V, TJ = –40°C to 125°C
** In development



the power franchise™

FAIRCHILD SEMICONDUCTOR®

High-Speed, Low-Side Gate Drivers

Selection Guide

Channels	Current	Inputs per Channel	Gnd Pins	Package	$R_{\theta JL}$ (°C/W)	Part Number (a)
Single	2A	Dual-input (+ and −)	2	SOT23-5	55	FAN3100xSX
			2, 5	2x2mm MLP-6	3	FAN3100xMPX
Dual (b)	2A	Inverting and Enable	3	SOIC-8	39	FAN3226xMX
				3x3mm MLP-8	2	FAN3226xMPX
		Non-inverting and Enable		SOIC-8	39	FAN3227xMX
				3x3mm MLP-8	2	FAN3227xMPX
		Dual-input (+ and −)		SOIC-8	39	FAN3228xMX
				3x3mm MLP-8	2	FAN3228xMPX
		Dual-input (+ an	8	SOIC-8	39	FAN3229xMX
				3x3mm MLP-8	2	FAN3229xMPX
Dual	4A	Inverting and Enable	3	SOIC-8	37	FAN3223xMX
				3x3mm MLP-8	1	FAN3223xMPX
		Non-inverting and Enable		SOIC-8	37	FAN3224xMX
				3x3mm MLP-8	1	FAN3224xMPX
		Dual-input (+ and −)		SOIC-8	37	FAN3225xMX
				3x3mm MLP-8	1	FAN3225xMPX
Single	9A**	Inverting and Enable	4, 5	SOIC-8	37	FAN3121xMX
				3x3mm MLP-8	1	FAN3121xMPX
		Non-inverting and Enable		SOIC-8	37	FAN3122xMX
				3x3mm MLP-8	1	FAN3122xMPX

(a) x = C or T for CMOS or TTL input thresholds (b) Channels may be paralleled to obtain a single 4A driver
** In development

Current Rating

… is selected to achieve a desired switching time and switching loss for the total gate charge Q_G of the power switch. For each driver current rating, the table to the right shows the approximate minimum turn-on or turn-off time assuming no series gate-drive resistance ($t_{SW,MIN}=(Q_G/I_{RATED})$ x1.5, an empirical constant).

Q_G (nC)	Min. Switching Time (ns) for Driver Current Rating 2A	4A	9A**
5	3.8		
10	7.5	3.8	
20	15	7.5	3.3
50	38	19	8.3
100	75	38	17
200	150	75	33
500	375	188	83
1000	750	375	167

** In development

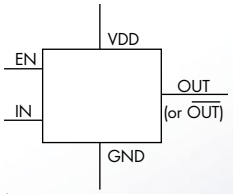
Input Configuration

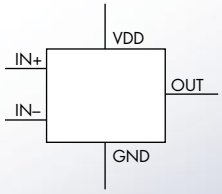
Single Input plus Enable

- Inverting and Enable
- Non-inverting and Enable
- Enable defaults to high = ON

Dual Input

- Inverting operation using IN− (with IN+ held high)
- Non-inverting operation using IN+ (with IN− held low)
- Other input can be Enable



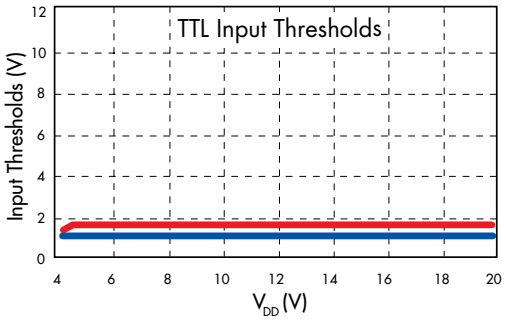


IN+	IN–	OUT
0	0	0
0	1	0
1	0	1
1	1	0

Input Thresholds

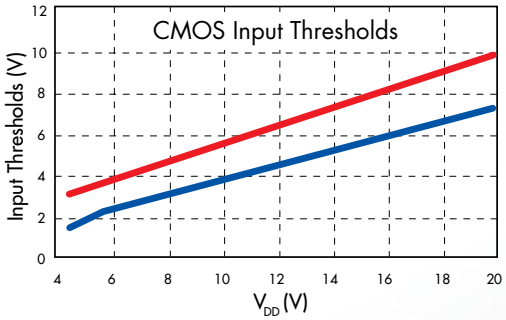
TTL (0.8V, 2.0V)

- For logic-level input signals, e.g., 3.3V or 5V
- For constant input thresholds as V_{DD} varies
- Most common choice



CMOS (~40% and 60% of V_{DD})

- For noisy environments
- For ease of adding R-C time delays at driver input
- For input thresholds proportional to V_{DD}



Package

Select for a maximum junction-to-lead thermal resistance of:

$$R_{\theta JL,\,MAX} = \frac{T_{J,\,MAX,\,OP} - T_{L,\,MAX,\,OP}}{P_{PKG}\,F_{PCB}}$$

where:

$T_{J,\,MAX,\,OP}$ = maximum operating junction temperature ≤150°C

$T_{L,\,MAX,\,OP}$ = maximum operating lead temperature ≤ maximum PCB temperature

P_{PKG} = average power dissipated in the package = $V_{DD}\,Q_G\,f_{SW}$ minus the dissipation in the series gate resistance = $I^2_{G,\,RMS}\,R_G$ (difficult to estimate)

F_{PCB} = fraction of P_{PKG} that flows into the PCB, e.g., 0.9