NXP ARM926EJ-S processors LPC3143 & LPC3141

Lowest Cost ARM9 with HS USB 2.0 OTG & Decryption Engine

Embedded designers can now take advantage of higher performance, lower cost, lower power consumption, and a smaller footprint – while adding flexible USB connectivity and a decryption engine.

Key Features

- CPU Platform
  - 270-MHz, 32-bit ARM926EJ-S
  - 16 KB D-Cache & 16 KB I-Cache
  - Memory Management Unit (MMU)
- Internal Memory
  - 192 KB embedded SRAM
- External Memory Interface
  - NAND Flash Controller with 8-bit ECC
  - 128-bit AES Decryption Engine (LPC3143)
  - 8/16-bit Multi-Port Memory Controller (MPMC): SDRAM and SRAM
- Communication & Connectivity
  - High Speed USB 2.0 OTG with on-chip PHY
  - Two I^2S interfaces
  - Master/Slave PCM
  - Master/Slave SPI
  - Two Master/Slave I^2C
  - Fast UART
  - Memory Card Interface (MCI): MMC/SD/SDIO/CE-ATA
  - Four channel 10-bit ADC
  - Integrated 4/8/16-bit 6800/8080 compatible LCD interface
- System Function
  - Dynamic clock gating & scaling
  - Selectable boot-up: SPI Flash, NAND Flash, SD/MMC cards, UART or USB
  - Secure NAND Flash Boot (LPC3143)
  - 512-bit Secure OTP
  - DMA controller
  - Four 32-bit timers
  - Watchdog timer
  - PWM module
  - Random Number Generator (RNG)
  - General-Purpose I/O pins (GPIO)
  - Event Router
  - Interrupt Controller
  - JTAG interface
- Operating Voltage & Temperature
  - Core Voltage: 1.2 V
  - I/O Voltage: 1.8, 2.8, 3.3 V
  - Temperature: -40 °C to +85 °C
- Package
  - TFBGA180: 12x12 mm2, 0.8 mm pitch

Applications

- Consumer
- Industrial
- Medical
- Communication
- Automotive Infotainment

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The NXP LPC3143/1 family combines a 270-MHz ARM926EJ CPU core, High Speed USB 2.0 OTG, up to 192 KB SRAM, NAND Flash Controller with a 128-bit AES Decryption Engine (LPC3143), flexible external bus interface, four channel 10-bit A/D and a myriad of serial and parallel interfaces. To optimize system power consumption, the LPC3143/1 have multiple power domains and a very flexible Clock Generation Unit (CGU) that provides dynamic clock gating and scaling.

The USB interface contains a UTMI+ compliant transceiver (PHY), a dedicated PLL, and a dedicated DMA engine providing high speed transfer rates (up to 480 Mbps) and supports device, host and On-The-Go (OTG) operations.

The secure One-Time-Programmable (OTP) memory provides a unique ID, the ability to store secure keys/USB product ID, and the option to access JTAG securely.

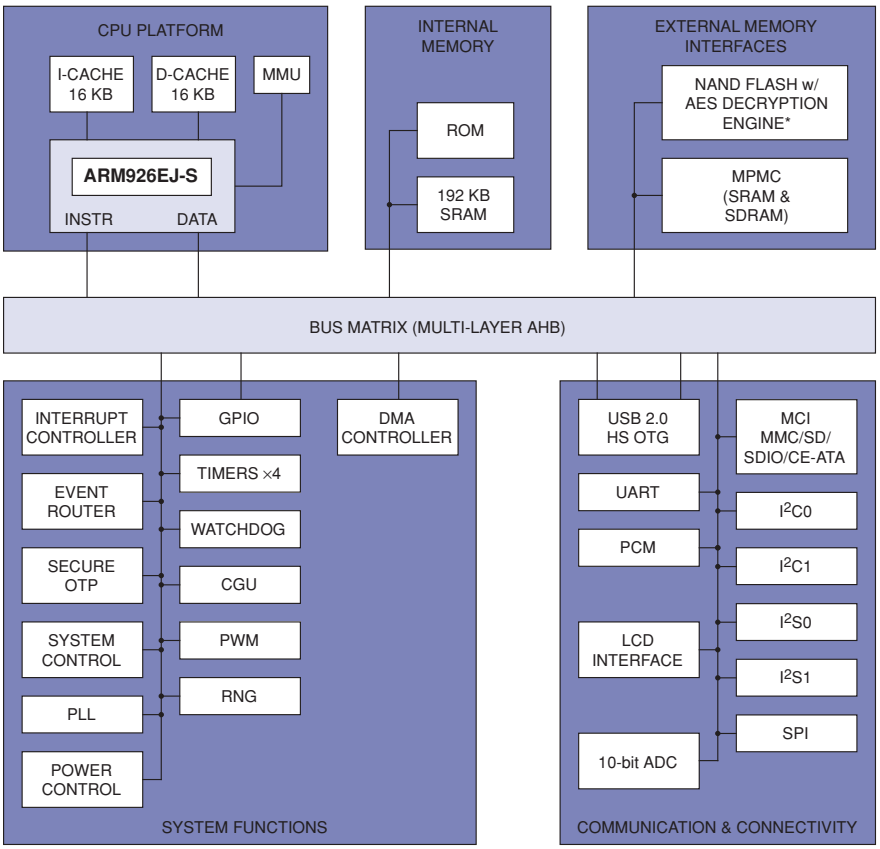
Third-Party Development Tools

Through third-party suppliers we offer a range of development and evaluation tools for our microcontrollers. For the most current listing, please visit www.nxp.com/microcontrollers.

Selection Guide for LPC3143/1 Family

Part Number	SRAM (KB)	HS USB, OTG	A/D Converter (channel x bit)	LCD Interface	MMC, SD, SDIO, CE-ATA	SPI	I^2C-bus	I^2S	Decryption Engine	Secure OTP	Temperature Range (°C)	Package
LPC3143	192	1	4 x 10	1	1	1	2	2	Yes	Yes	-40 to +85	TFBGA180
LPC3141	192	1	4 x 10	1	1	1	2	2	No	Yes	-40 to +85	TFBGA180

LPC3143/1 Block Diagram



*AES available on LPC3143 only

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