National Semiconductor

PRELIMINARY

NMC27C49 Very High Speed Version 65,536-Bit (8k x 8) UV Erasable CMOS PROM Pin Compatible with 64k Bipolar PROMs

General Description

The NMC27C49 is a very high-speed 64k, UV erasable and electrically reprogrammable CMOS EPROM, ideally suited for applications where fast turnaround, pattern experimentation and low power consumption are important requirements.

The NMC27C49 is designed to operate with a single +5V power supply with ±10% tolerance.

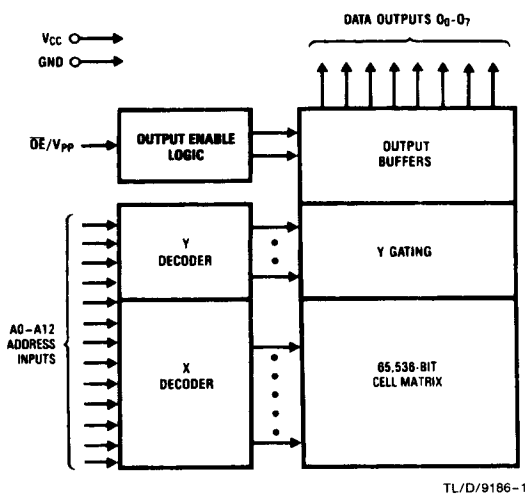
The NMC27C49 is packaged in a 300 mil, 24-pin dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written electrically into the device by following the programming procedure.

This EPROM is fabricated with National's proprietary, time-proven CMOS double-poly silicon gate technology which combines high performance and high density with low power consumption and excellent reliability. A two transistor memory cell is used for speed enhancement.

Features

- Clocked sense amps and a two transistor memory cell for fast acess time down to 35 ns
- Low CMOS power consumption
  —Active power: 275 mW max
- Performance compatible to current high speed microprocessors
- Single 5V power supply
- Fast and reliable programming (100 μs for most bytes)
- Static operation—no clocks required
- TTL, CMOS compatible inputs/outputs
- TRI-STATE® output
- Pin compatible with 64k Bipolar PROMs
- Manufacturer's identification code for automatic programming control
- High current CMOS level output driver

Block Diagram



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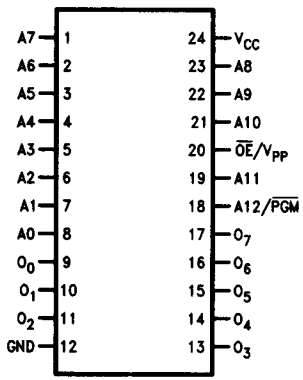
Pin Names

A0–A12	Addresses
$\overline{OE}$	Output Enable
O_0–O_7	Outputs
$\overline{PGM}$	Program

Connection Diagram

27C53	27C51
A9	A9
A8	A8
A7	A7
A6	A6
A5	A5
A4	A4
A3	A3
A2	A2
A1	A1
A0	A0
O_0	O_0
O_1	O_1
O_2	O_2
GND	GND

Dual-In-Line Package



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27C51	27C53
V_{CC}	V_{CC}
A10	A10
A11	A11
A12	A12
A13	A13
$\overline{OE1}/V_{PP}$	A14
$\overline{OE2}/\overline{VFY}$	$\overline{OE1}/V_{PP}$
OE3	OE2/$\overline{PGM}$
$\overline{OE4}/\overline{PGM}$	$\overline{OE3}/\overline{VFY}$
O_7	O_7
O_6	O_6
O_5	O_5
O_4	O_4
O_3	O_3

Note: Socket compatible EPROM pin configurations are shown in the blocks adjacent to the NMC27C49 pins.

Order Number NMC27C49Q
See NS Package Number J24CQ

Commercial Temp Range (0°C to +70°C) V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC27C49Q35	35
NMC27C49Q45	45
NMC27C49Q55	55

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Temperature Under Bias	−10°C to +80°C
Storage Temperature	−65°C to +150°C
V_{CC} Supply Voltage with Respect to Ground	+7.0V to −0.6V
All Input Voltages except A9 and A10 with Respect to Ground (Note 4)	+6.5V to −0.6V
All Output Voltages with Respect to Ground (Note 4)	V_{CC} + 1.0V to GND − 0.6V
$\overline{OE}/V_{PP}$ Supply Voltage, A9 and A10 with Respect to Ground During Programming	+14.0V to −0.6V
Power Dissipation	1.0W
Lead Temperature (Soldering, 10 sec.)	300°C
ESD Rating (Mil Spec 883C, Method 3015.2)	2000V

Operating Conditions (Note 7)

Temperature Range	0°C to +70°C
V_{CC} Power Supply	5V ±10%

READ OPERATION

DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{CC}$ or GND			1.0	μA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or GND, $\overline{OE}/V_{PP} = V_{IH}$			1.0	μA
I_{PP}	V_{PP} Load Current	$V_{PP} = V_{CC}$			10	μA
I_{CC1} (Note 1)	V_{CC} Current (Active) TTL Inputs	$\overline{OE} = V_{IL}$, f = 20 MHz Inputs = V_{IH} or V_{IL}, I/O = 0 mA		30	70	mA
I_{CC2} (Note 1)	V_{CC} Current (Active) CMOS Inputs	$\overline{OE}$ = GND, f = 20 MHz Inputs = V_{CC} or GND, I/O = 0 mA		25	50	mA
V_{IL}	Input Low Voltage	(Note 4)	−0.2		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 1	V
V_{OL1}	Output Low Voltage	I_{OL} = 16 mA			0.4	V
V_{OH1}	Output High Voltage	I_{OH} = −2.5 mA (Note 8)	3.5			V
V_{OL2}	Output Low Voltage	I_{OL} = 10 μA			0.1	V
V_{OH2}	Output High Voltage	I_{OH} = −10 μA (Note 8)	V_{CC} − 0.1			V

AC Electrical Characteristics

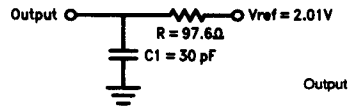
Symbol	Parameter	Conditions	NMC27C49						Units
			Q35		Q45		Q55		
			Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{OE} = V_{IL}$		35		45		55	ns
t_{OE}	OE to Output Delay	$\overline{OE} = V_{IL}$		20		25		25	ns
t_{DF} (Note 3)	OE High to Output Float	$\overline{OE} = V_{IH}$	0	20	0	25	0	25	ns
t_{OH}	Output Hold from Addresses, or $\overline{OE}$ = Enable, Whichever Occurred First	$\overline{OE} = V_{IL}$	0		0		0		ns

Capacitance T_A = +25°C, f = 1 MHz (Note 3)

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	V_{IN} = 0V	6	12	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	9	12	pF

AC Test Conditions

Input Rise and Fall Times	≤5 ns
Input Pulse Levels	0.0V to 3.0V
Output Load (Note 6)	R = 97.6Ω C_L = 30 pF V_{REF} = 2.01V
Timing Measurement Reference Level	
Inputs	0.8V and 2V
Outputs	0.8V and 2V



Output Loading

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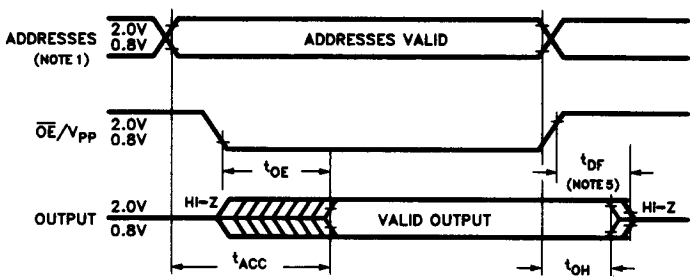
AC Waveforms (Notes 7 & 8)



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Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: Typical values are for T_A = +25°C and nominal supply voltages.

Note 3: This parameter is only sampled and is not 100% tested.

Note 4: Inputs and outputs can undershoot to −2.0V for 20 ns max.

Note 5: The t_{DF} compare level is determined as follows:
High to TRI-STATE, the measured V_{OH1} (DC) − 0.10V;
Low to TRI-STATE, the measured V_{OL1} (DC) + 0.10V.

Note 6: C_L: 30 pF includes fixture capacitance.

Note 7: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND.

Note 8: The outputs must be restricted to V_{CC} + 1.0V to avoid latch-up and device damage.

Programming Characteristics

$T_A = +25°C$, $V_{CC} = 6.25V \pm 0.25V$, $V_{PP} = 12.75V \pm 0.25V$ (Notes 1–4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Setup Time		1			μs
t_{OES}	$\overline{OE}$ Setup Time		1			μs
t_{DS}	Data Setup Time		1			μs
t_{VPS}	V_{PP} Setup Time		1			μs
t_{VCS}	V_{CC} Setup Time		1			μs
t_{LS}	A_{11} Setup Time for Latching		50			ns
t_{LH}	A_{11} Hold Time for Latching		1			μs
t_{AH}	Address Hold Time		0			μs
t_{DH}	Data Hold Time		1			μs
t_{OEH}	$\overline{OE}$ Hold Time		1			μs
t_{DF}	Output Enable to Output Float Delay (Note 5)		0		40	ns
t_{DV}	Data Valid from $\overline{OE}/V_{PP}$	$\overline{OE}/V_{PP} = V_{IH}$ or V_{IL}			100	ns
t_{AV}	Data Valid from Address	$\overline{OE}/V_{PP} = V_{IH}$ or V_{IL}			100	ns
t_{PW}	Program Pulse Width		95	100	105	μs
t_{PRT}	$\overline{OE}/V_{PP}$ Pulse Rise Time During Programming		50			ns
t_{VPW}	V_{PP} Level Pulse Width on A9 or A10		1			μs
I_{PP}	V_{PP} Supply Current During Programming Pulse	$A12/\overline{PGM} = V_{IL}$			60	mA
I_{CC}	V_{CC} Supply Current				60	mA
T_A	Temperature Ambient		20	25	30	°C
V_{CC}	Power Supply Voltage		6.0	6.25	6.5	V
V_{PP}	Programming Supply Voltage		12.5	12.75	13.0	V
t_{FR}	Input Rise, Fall Time		5			ns
V_{IL}	Input Low Voltage			0.0	0.45	V
V_{IH}	Input High Voltage		2.4	4.0		V
t_{IN}	Input Timing Reference Voltage		0.8	1.5	2.0	V
t_{OUT}	Output Timing Reference Voltage		0.8	1.5	2.0	V

Note 1: National's standard product warranty applies only to devices programmed to specifications described herein.

Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The EPROM must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

Note 3: The maximum allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent any overshoot from exceeding this 14V maximum specification. At least a 0.1 μF capacitor is required across V_{PP}, V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Note 4: Programming and program verify are tested at nominal supply voltages.

Note 5: The t_{DF} compare level is determined as follows:
High to TRI-STATE, the measured V_{OH1} (DC) − 0.10V;
Low to TRI-STATE, the measured V_{OL1} (DC) + 0.10V.

Functional Description

DEVICE OPERATION

The modes of operation of the NMC27C49 are listed in Table I. It should be noted that all inputs for the modes may be at TTL levels. The power supplies required are V_{PP} and V_{CC}. The V_{CC} power supply must be at 6.25V during the programming and verify modes, and at 5V in the other modes. The $\overline{OE}/V_{PP}$ pin must be at 12.75V in four of the programming modes, and V_{IL} in the read mode.

READ MODE

The NMC27C49 has one control function, Output Enable ($\overline{OE}/V_{PP}$), which must be logically active in order to obtain data at the outputs. This is only true, however, when the device is not latched into programming mode or verify mode, so care must be taken to be sure the device is not in these modes. The sense amps are clocked for fast access time. V_{CC} should therefore be maintained at operating voltage during read and verify. If V_{CC} temporarily drops below the spec. voltage (but not to ground), an address transition must be performed after the drop to ensure proper output data.

PROGRAMMING

CAUTION: Exceeding 14V on pin 20 ($\overline{OE}/V_{PP}$) will damage the NMC27C49.

The NMC27C49 has a new memory cell which contributes greatly to its speed. The cell has two transistors which supply data to two data lines. When programmed, one or the other of the two transistors is programmed. When accessed, the memory cell will discharge one of the two data lines, providing a differential voltage. This differential voltage is then applied through pass devices to a true differential sense amplifier.

Initially, all memory cells are totally unprogrammed. In an unprogrammed state, both transistors source the same current through the data lines and thus no differential voltage is produced. Because of this, any attempt to read data in the read mode from an unprogrammed device will result in arbitrary outputs.

To verify that a device is totally blank, the verify mode must be entered. This is accomplished by raising A10 to V_{PP} and then back to the proper logic level (less than 5V). In the verify mode, each transistor of the memory cell is checked against a reference cell. By toggling $\overline{OE}/V_{PP}$, both transistors in the cell are checked. For a totally unprogrammed device in the verify mode, all outputs will be at a "1" state for $\overline{OE}/V_{PP} = V_{IH}$ and at a "0" state for $\overline{OE}/V_{PP} = V_{IL}$. The verify mode is exited by either powering down the device, or by raising A9 to V_{PP} and then back to a logic level (less than 5V) with $\overline{OE}/V_{PP}$ at V_{IH}.

The programming mode is entered by raising $\overline{OE}/V_{PP}$ to 12.75V. In this mode, the A12/$\overline{PGM}$ pin functions as the programming control pin. Addressing while in programming mode is accomplished by placing the A12 address on A11 and then latching this into an onboard register when $\overline{OE}/V_{PP}$ is raised to 12.75V. The NMC27C49 is now locked into the programming mode and half of the chip can be programmed. Once half of the device is programmed and verified, the programming mode must be exited and then re-entered with the opposite data for address A12 in order to program the other half of the device. The programming mode is exited by powering down the device, or by dropping $\overline{OE}/V_{PP}$ to V_{IH} and then raising A9 to V_{PP} and then back to a logic level.

It is required that at least a 0.1 μF capacitor be placed across $\overline{OE}/V_{PP}$, V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed are applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the device has been latched into programming mode and the addresses and data are stable, an active low TTL program pulse is applied to the A12/$\overline{PGM}$ input. A program pulse must be applied to each address location that is to be programmed. A memory cell has been completely programmed when, in the verify mode, toggling $\overline{OE}/V_{PP}$ reads back the same data in both modes. The NMC27C49

TABLE I. Mode Selection

Mode \ Pins	$\overline{OE}/V_{PP}$ (20)	A12/$\overline{PGM}$ (18)	A9 (22)	A10 (21)	A11 (19)	V_{CC} (24)	Outputs (9–11, 13–17)
Read	V_{IL}	X	X	X	X	5V	D_{OUT}
Output Disable	V_{IH}	X	X	X	X	5V	Hi-Z
Enter Programming Mode for Addresses with A12 = V_{IL}	12.75V	V_{IH}	X	X	V_{IL}	6.25V	D_{IN}
Enter Programming Mode for Addresses with A12 = V_{IH}	12.75V	V_{IH}	X	X	V_{IH}	6.25V	D_{IN}
Program	12.75V	V_{IL}	X	X	X	6.25V	D_{IN}
Enter Initial Verify Mode	X	X	X	12	X	6.25V	D_{OUT}
Verify (Mode 1)	V_{IH}	V_{IH}	X	X	X	6.25V	D_{OUT} (V_{OH} if Blank)
Verify (Mode 2)	V_{IL}	V_{IH}	X	X	X	6.25V	D_{OUT} (V_{OL} if Blank)
Program Inhibit	12.75V	V_{IH}	X	X	X	6.25V	Hi-Z
Exit Programming Mode and Verify Mode	V_{IH}	V_{IH}	12	X	X	6.25V	Hi-Z

X = Don't Care

Functional Description (Continued)

is programmed with the Fast Programming Algorithm shown in *Figure 1*. Each address is programmed with a series of 100 μs pulses until it verifies good, up to a maximum of 25 pulses. Most memory cells will program with a single 100 μs pulse. The NMC27C49 must not be programmed with a DC signal applied to the A12/$\overline{PGM}$ input.

Programming multiple NMC27C49s in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled NMC27C49s may be connected together when they are programmed with the same data. A low level TTL pulse applied to the A12/$\overline{PGM}$ input programs the paralleled NMC27C49s.

PROGRAM INHIBIT

Programming multiple NMC27C49s in parallel with different data is also easily accomplished. Except for A12/$\overline{PGM}$, all like inputs (including $\overline{OE}/V_{PP}$) of the paralleled NMC27C49s may be common. A TTL low level applied to an NMC27C49's A12/$\overline{PGM}$ input will program that NMC27C49 while keeping the same pin high on the others inhibits programming.

PROGRAM VERIFY

A verify should be performed on the programmed bits to determine whether they were correctly programmed. A verify done in the read mode may not ensure that the bits have been programmed with adequate margins for reliable operation. To guarantee adequate margins the device should be verified in the verify mode, where each transistor of the memory cell is checked against a reference cell. Verify mode can be entered two different ways. The first way is by verifying after programming. When $\overline{OE}/V_{PP}$ is at 12.75V, the device is in programming mode, and when $\overline{OE}/V_{PP}$ is brought back down to V_{IH} or V_{IL}, it is in the verify mode. The second method for entering the verify mode is to apply 12V to address pin A10 with the other pins at V_{IH} or V_{IL}. This method is recommended if possible for an initial verify when the device is totally unprogrammed because power up only needs to be performed once. Independent of how verify mode is entered, $\overline{OE}/V_{PP}$ is biased at V_{IH} and the data is read for verify mode 1 and at V_{IL} for verify mode 2. The data read in both modes must be the same as the expected data for a completely programmed cell. For a totally unprogrammed device, all outputs will be at a "1" state for verify mode 1 and at a "0" state for verify mode 2. As in programming mode, verify mode is exited by powering down the device, or by raising A9 to V_{PP} and then back to a logic level with $\overline{OE}/V_{PP}$ at V_{IH}.

MANUFACTURER'S IDENTIFICATION CODE

The NMC27C49 has a manufacturer's identification code to aid in programming. The code, shown in Table II, is two bytes wide and is stored in a ROM configuration on the chip.

It identifies the manufacturer and the device type. The code for the NMC27C49 is "83C2", where "83" designates that it is made by National Semiconductor, and "C2" designates that it is a 64k part. The code is acessed by applying 12V ±0.5V to address pin A9. Addresses A1–A8, A10–A12, and $\overline{OE}/V_{PP}$ are held at V_{IL}. Address A0 is held at V_{IL} for the manufacturer's code, and at V_{IH} for the device code. The code is read out on the 8 data pins. Proper code access is only guaranteed at 25°C ±5°C.

The primary purpose of the manufacturer's identification code is automatic programming control. When the device is inserted in an EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

ERASURE CHARACTERISTICS

The erasure characteristics of the NMC27C49 are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å–4000Å range. Opaque labels should be placed over the NMC27C49s window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

TABLE II. Manufacturer's Identification Code

Pins	A0 (10)	O_7 (19)	O_6 (18)	O_5 (17)	O_4 (16)	O_3 (15)	O_2 (13)	O_1 (12)	O_0 (11)	Hex Data
Manufacturer Code	V_{IL}	1	0	0	0	0	0	1	1	83
Device Code	V_{IH}	1	1	0	0	0	0	1	0	C2

TABLE III. Minimum NMC27C49 Erasure Time

Light Intensity ($\mu W/cm^2$)	Erasure Time (Minutes)
15,000	20
10,000	25
5,000	50

Functional Description (Continued)

The recommended erasure procedure for the NMC27C49 is exposure to short wave ultraviolet light which has a wavelength of 2537Å. The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of 15W-sec/cm^2.

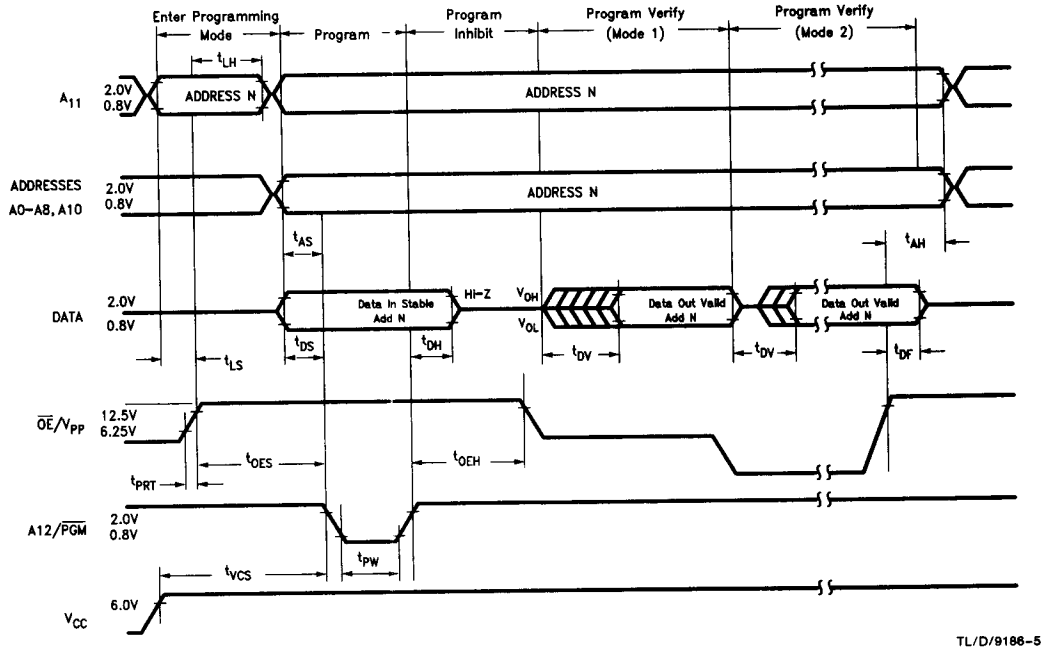
The NMC27C49 should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure. Table III shows the minimum NMC27C49 erasure time for various light intensities.

An erasure system should be calibrated periodically. The distance from lamp to unit should be maintained at one inch. The erasure time increases as the square of the distance. (If distance is doubled the erasure time increases by a factor of 4.) Lamps lose intensity as they age. When a lamp is changed, the distance has changed, or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of devices. The supply current, I_{CC}, has two segments that are of interest to the system designer—the active current level and the transient current peaks that are produced by voltage transitions on the input pins. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

Programming Waveforms (Note 3)



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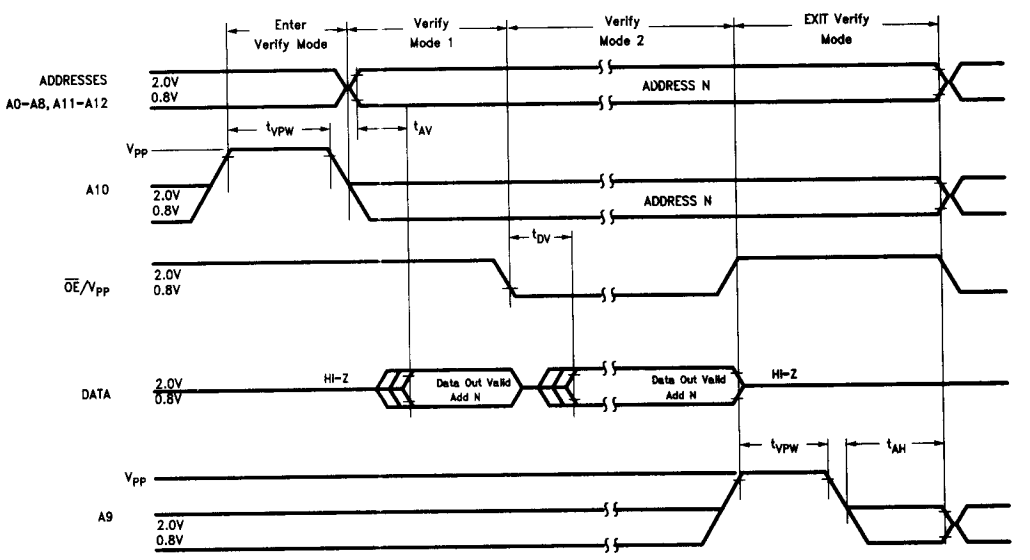
Initial Program Verify Waveforms



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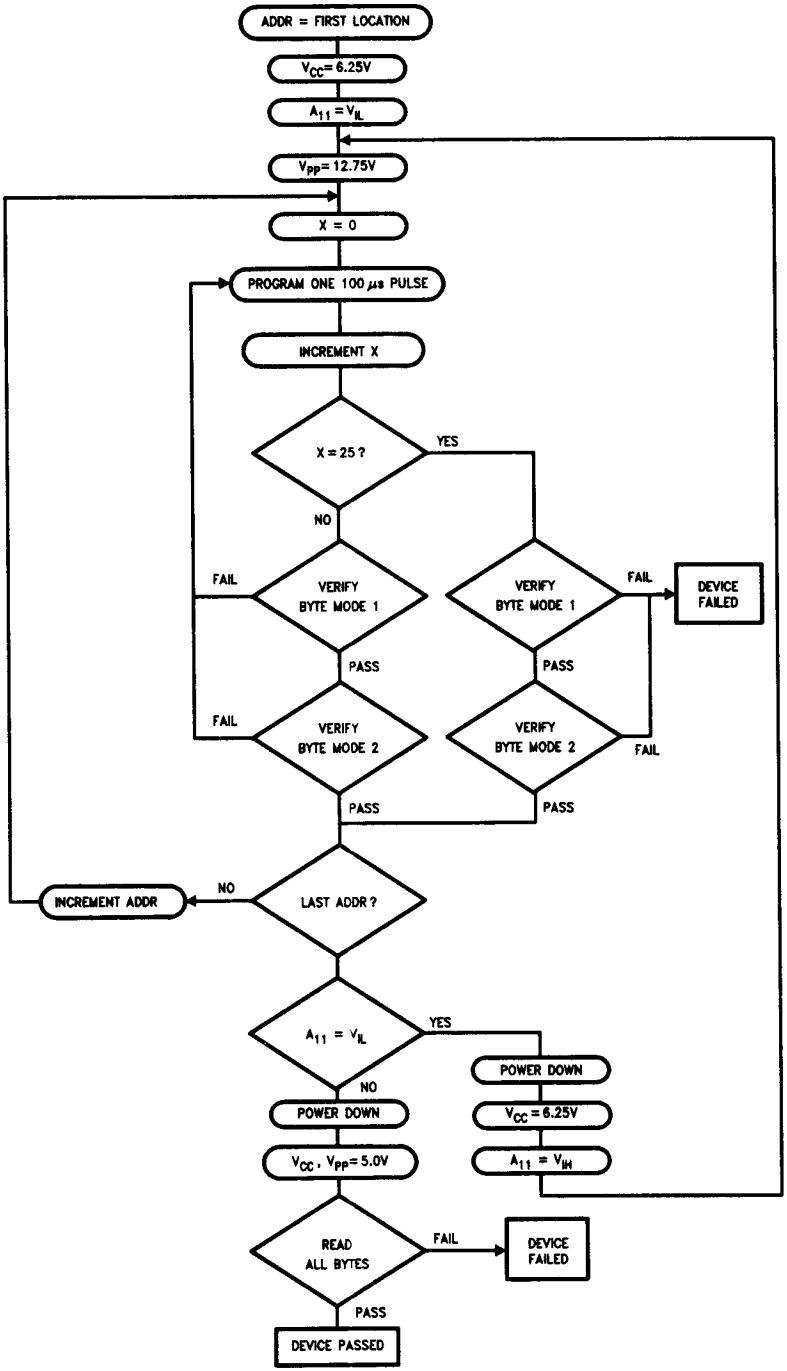

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FIGURE 1. Fast Programming Algorithm Flow Chart