

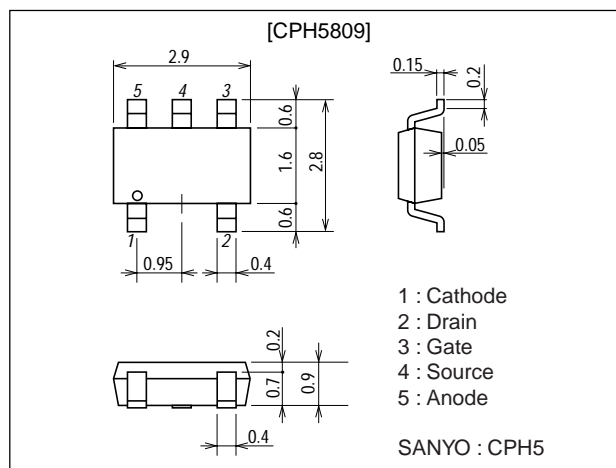
**CPH5809****DC / DC Converter Applications****Features**

- The CPH5809 composite device consists of following two devices to facilitate high-density mounting. One is an N-channel MOSFET that features low ON-resistance, ultrahigh-speed switching, and low driving voltage. The other is a schottky barrier diode that features short reverse recovery time and low forward voltage.
- Each device incorporated in the CPH5809 is equivalent to the MCH3411 and to the SBS005, respectively.

Package Dimensions

unit : mm

2171

**Specifications****Absolute Maximum Ratings** at $T_a=25^{\circ}\text{C}$

| Parameter | Symbol | Conditions | Ratings | Unit |
|--|-----------|--|-------------|--------------------|
| [MOSFET] | | | | |
| Drain-to-Source Voltage | V_{DSS} | | 30 | V |
| Gate-to-Source Voltage | V_{GSS} | | ± 10 | V |
| Drain Current (DC) | I_D | | 3 | A |
| Drain Current (Pulse) | I_{DP} | $PW \leq 10\mu\text{s}$, duty cycle $\leq 1\%$ | 12 | A |
| Allowable Power Dissipation | P_D | Mounted on a ceramic board (600mm ² X0.8mm) 1unit | 0.9 | W |
| Channel Temperature | T_{ch} | | 150 | $^{\circ}\text{C}$ |
| Storage Temperature | T_{stg} | | -55 to +125 | $^{\circ}\text{C}$ |
| [SBD] | | | | |
| Repetitive Peak Reverse Voltage | V_{RRM} | | 30 | V |
| Nonrepetitive Peak Reverse Surge Voltage | V_{RSM} | | 30 | V |
| Average Output Current | I_O | | 1 | A |
| Surge Forward Current | I_{FSM} | 50Hz sine wave, 1 cycle | 10 | A |
| Junction Temperature | T_J | | -55 to +125 | $^{\circ}\text{C}$ |
| Storage Temperature | T_{stg} | | -55 to +125 | $^{\circ}\text{C}$ |

Marking : QK

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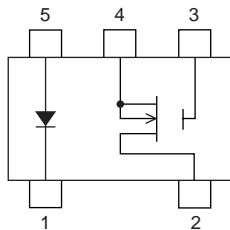
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

CPH5809

Electrical Characteristics at Ta=25°C

| Parameter | Symbol | Conditions | Ratings | | | Unit |
|--|---------------|--|---------|------|----------|---------------|
| | | | min | typ | max | |
| [MOSFET] | | | | | | |
| Drain-to-Source Breakdown Voltage | $V_{(BR)DSS}$ | $I_D=1mA, V_{GS}=0$ | 30 | | | V |
| Zero-Gate Voltage Drain Current | I_{DSS} | $V_{DS}=30V, V_{GS}=0$ | | | 1 | μA |
| Gate-to-Source Leakage Current | I_{GSS} | $V_{GS}=\pm 8V, V_{DS}=0$ | | | ± 10 | μA |
| Cutoff Voltage | $V_{GS(off)}$ | $V_{DS}=10V, I_D=1mA$ | 0.4 | | 1.3 | V |
| Forward Transfer Admittance | $ y_{fs} $ | $V_{DS}=10V, I_D=1.5A$ | 3.5 | 5.0 | | S |
| Static Drain-to-Source On-State Resistance | $R_{DS(on)1}$ | $I_D=1.5A, V_{GS}=4V$ | | 69 | 90 | $m\Omega$ |
| | $R_{DS(on)2}$ | $I_D=1A, V_{GS}=2.5V$ | | 84 | 118 | $m\Omega$ |
| Input Capacitance | C_{iss} | $V_{DS}=10V, f=1MHz$ | | 270 | | pF |
| Output Capacitance | C_{oss} | $V_{DS}=10V, f=1MHz$ | | 38 | | pF |
| Reverse Transfer Capacitance | C_{rss} | $V_{DS}=10V, f=1MHz$ | | 23 | | pF |
| Turn-ON Delay Time | $t_d(on)$ | See specified Test Circuit. | | 10 | | ns |
| Rise Time | t_r | See specified Test Circuit. | | 30 | | ns |
| Turn-OFF Delay Time | $t_d(off)$ | See specified Test Circuit. | | 42 | | ns |
| Fall Time | t_f | See specified Test Circuit. | | 52 | | ns |
| Total Gate Charge | Q_g | $V_{DS}=10V, V_{GS}=4V, I_D=3.0A$ | | 3.7 | | nC |
| Gate-to-Source Charge | Q_{gs} | $V_{DS}=10V, V_{GS}=4V, I_D=3.0A$ | | 0.7 | | nC |
| Gate-to-Drain "Miller" Charge | Q_{gd} | $V_{DS}=10V, V_{GS}=4V, I_D=3.0A$ | | 0.5 | | nC |
| Diode Forward Voltage | V_{SD} | $I_S=3.0A, V_{GS}=0$ | | 0.85 | 1.2 | V |
| [SBD] | | | | | | |
| Reverse Voltage | V_R | $I_R=1mA$ | 30 | | | V |
| Forward Voltage | V_{F1} | $I_F=0.5A$ | | 0.35 | 0.4 | V |
| | V_{F2} | $I_F=1A$ | | 0.42 | 0.47 | V |
| Reverse Current | I_R | $V_R=15V$ | | | 500 | μA |
| Interterminal Capacitance | C | $V_R=10V, f=1MHz$ cycle | | 35 | | pF |
| Reverse Recovery Time | t_{rr} | $I_F=I_R=100mA$, see specified Test Circuit. | | | 15 | ns |
| Thermal Resistance | Rthj-a | Mounted on a ceramic board (600mm ² X0.8mm) | | 110 | | $^{\circ}C/W$ |

Electrical Connection

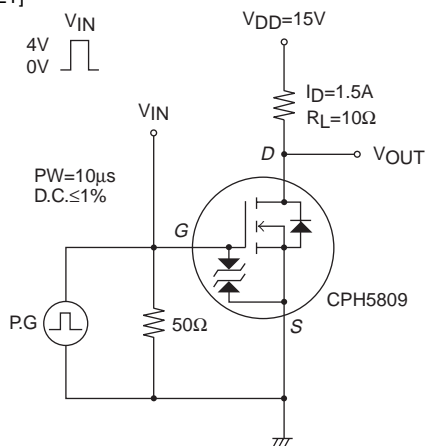


- 1 : Cathode
- 2 : Drain
- 3 : Gate
- 4 : Source
- 5 : Anode

(Top view)

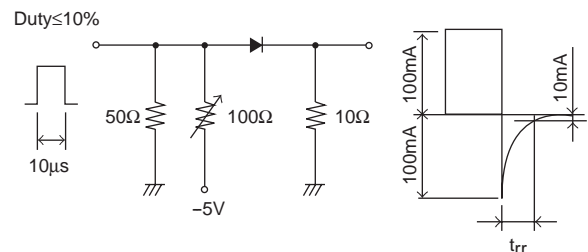
Switching Time Test Circuit

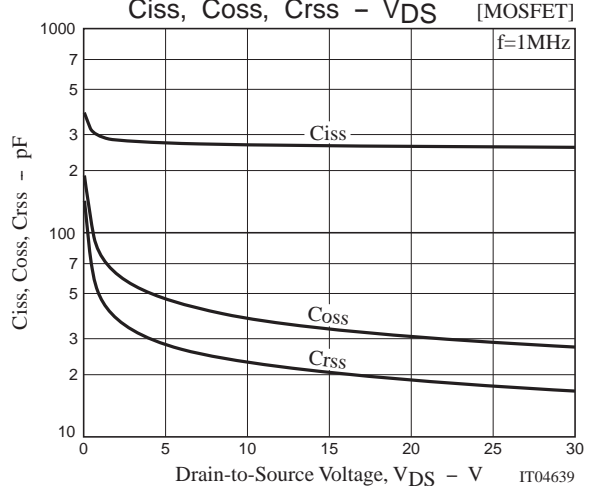
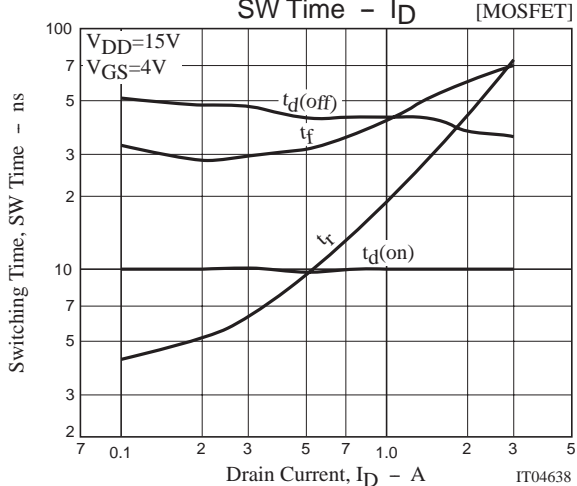
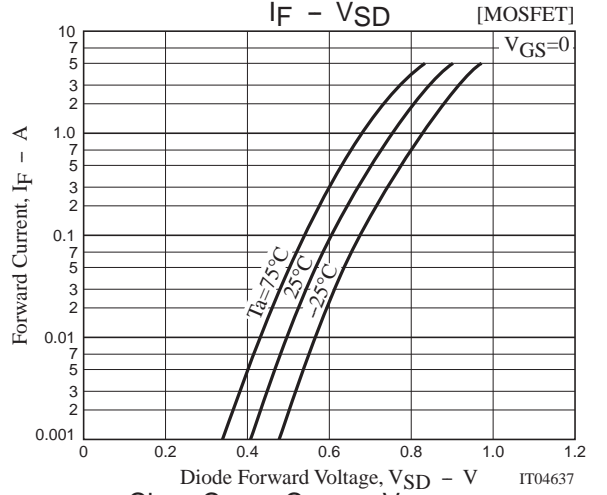
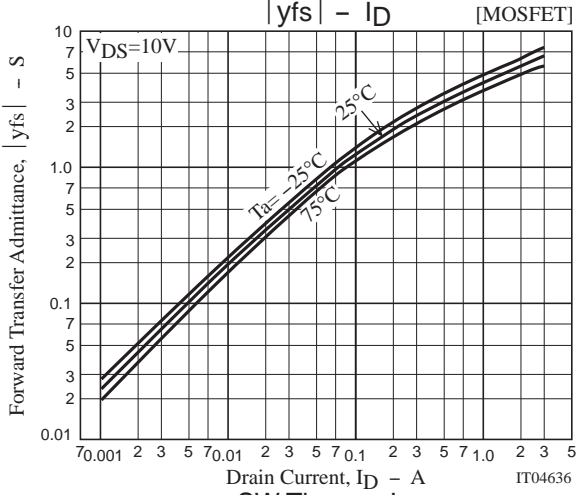
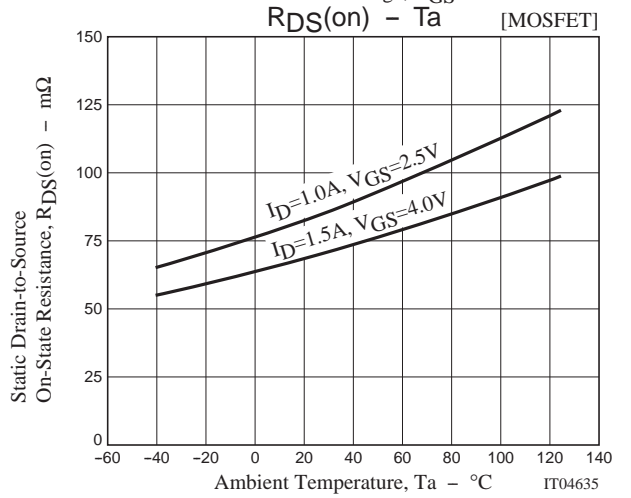
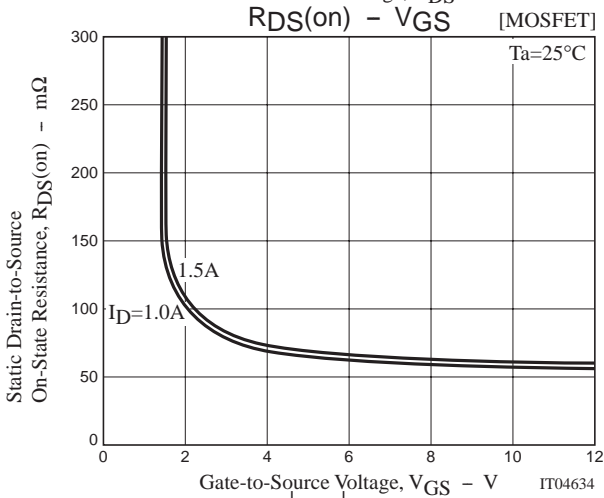
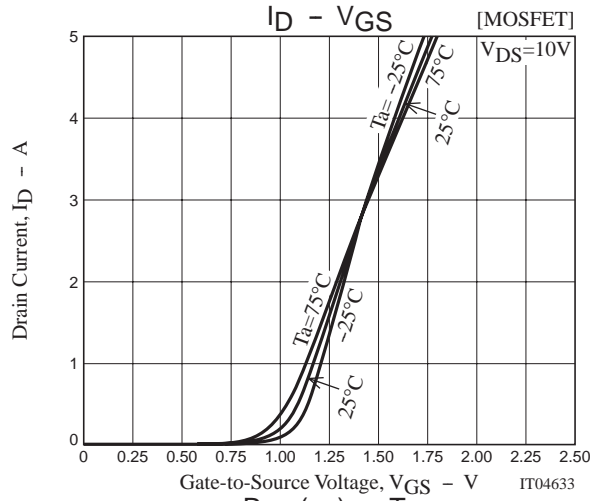
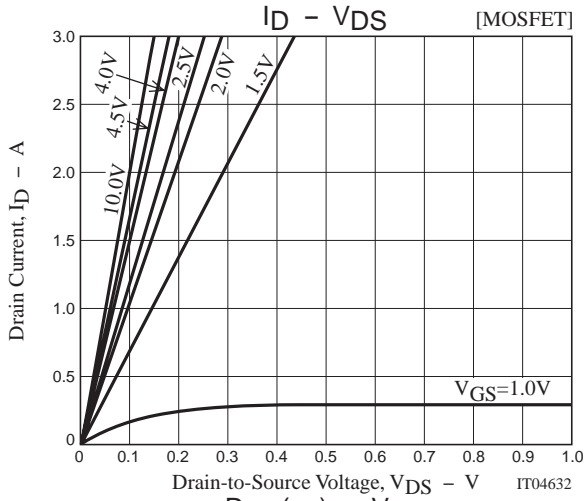
[MOSFET]

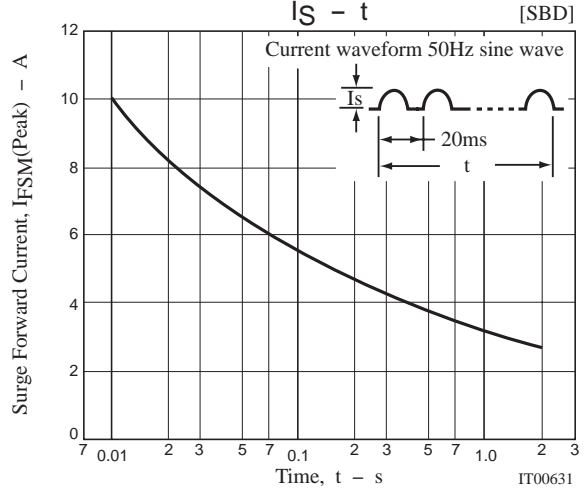
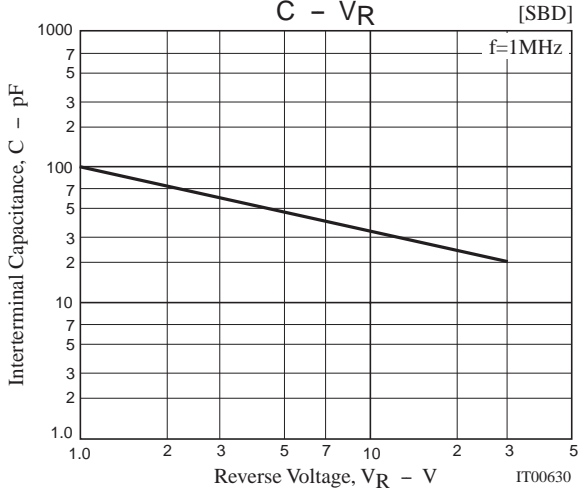
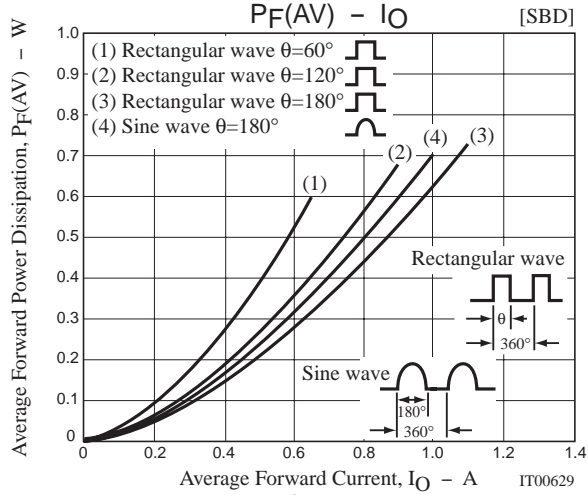
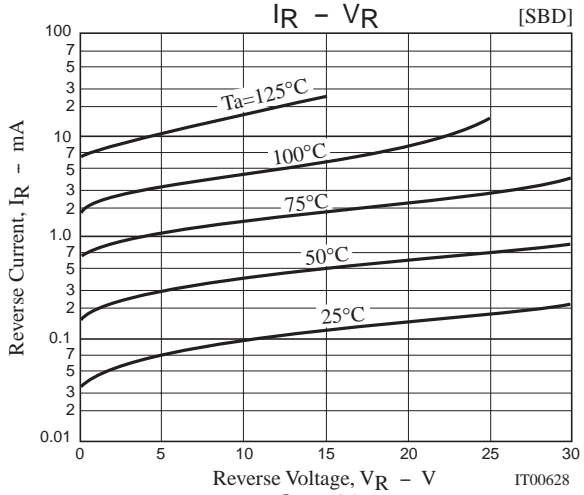
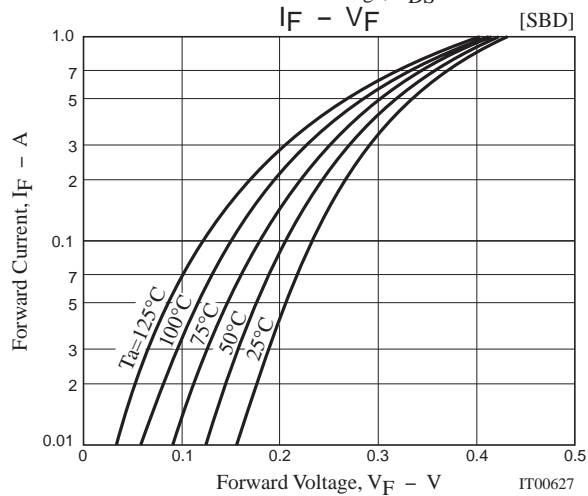
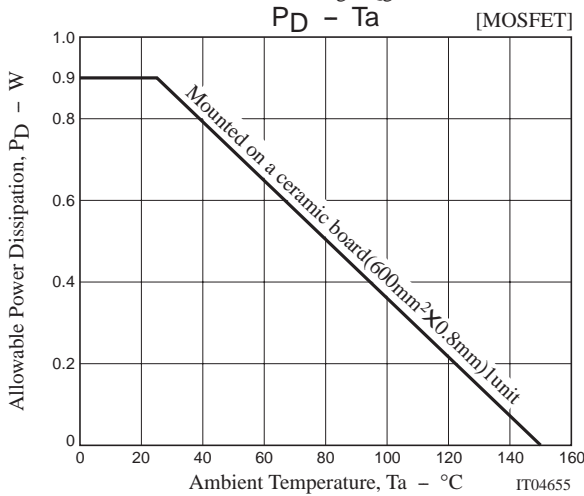
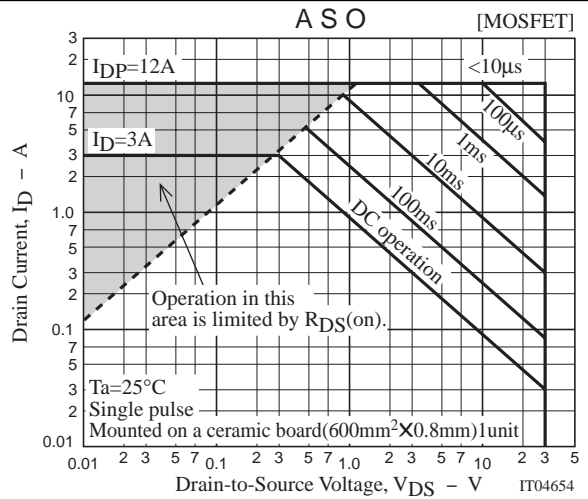
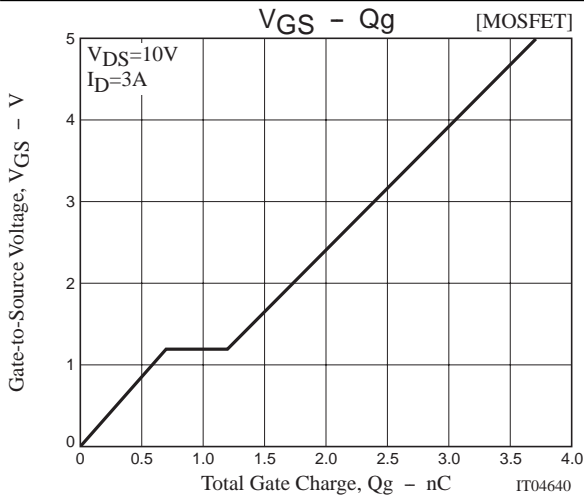


t_{rr} Test Circuit

[SBD]







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