



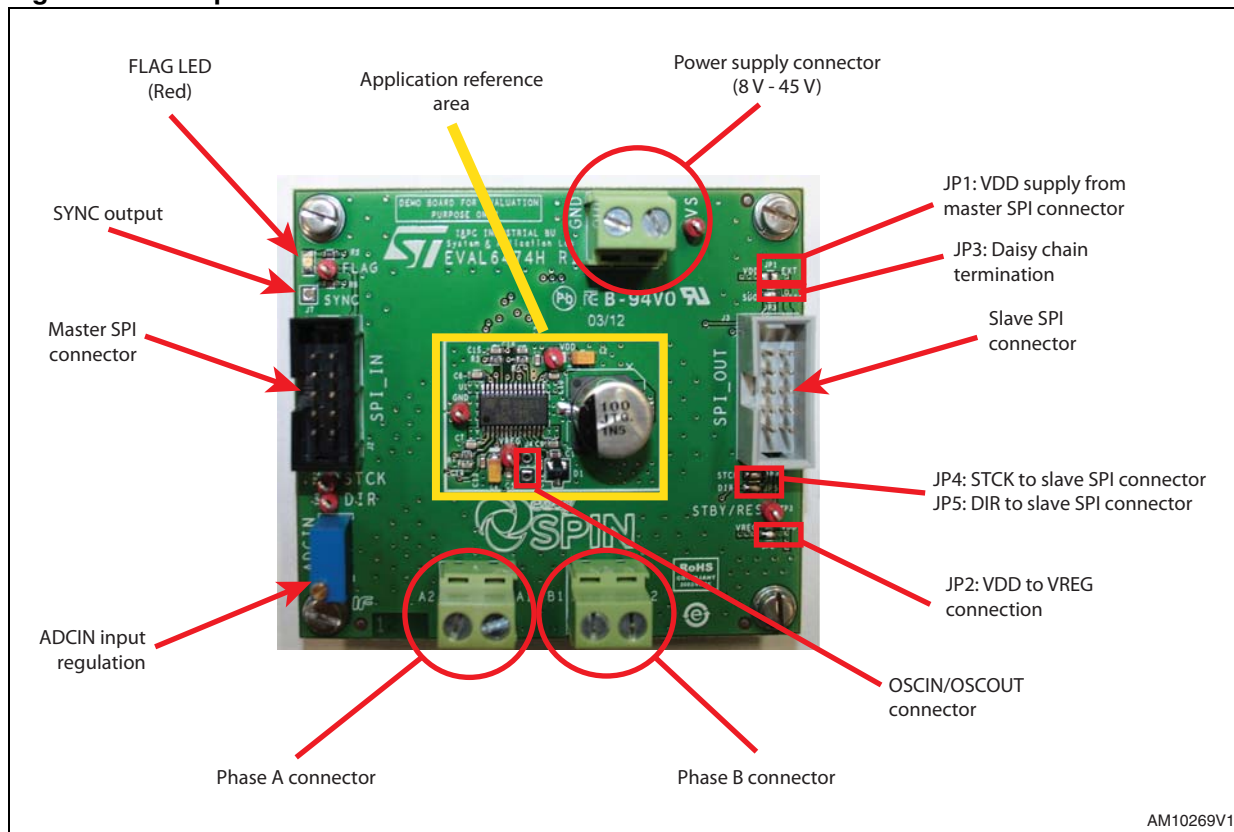
# 1 Board description

**Table 1. EVAL6474H specifications**

Parameter	Value
Supply voltage (VS)	8 to 45 V
Maximum output current (each phase)	3 A <sub>rms</sub>
Logic supply voltage (VREG)	Externally supplied: 3.3 V internally supplied: 3 V typical
Logic interface voltage (VDD)	Externally supplied: 3.3 V or 5 V internally supplied: VREG
Low level logic input voltage	0 V
High level logic input voltage	VDD <sup>(1)</sup>
Operating temperature	-25 to +125 °C
L6474H thermal resistance junction-to-ambient	21 °C/W typical

1. All logic inputs are 5 V tolerant.

**Figure 1. Jumper and connector location**



AM10269V1

**Table 2. Jumpers and connectors description**

Name	Type	Function
J1	Power supply	Motor supply voltage
J5	Power output	Bridge A outputs
J6	Power output	Bridge B outputs
J2	SPI connector	Master SPI
J3	SPI connector	Slave SPI
J4	NM connector	OSCIN and OSCOUT pins
J7	NM connector	SYNC output
TP1 (VS)	Test point	Motor supply voltage test point
TP4 (VDD)	Test point	Logic interface supply voltage test point
TP5 (VREG)	Test point	Logic supply voltage/L6474 internal regulator test point
TP6 (GND)	Test point	Ground test point
TP2 (STCK)	Test point	Step clock input test point
TP8 (DIR)	Test point	DIR output test point
TP3 (STBY/RES)	Test point	STBY/RES input test point
TP7 (FLAG)	Test point	FLAG output test point

**Table 3. Slave SPI connector pinout (J11)**

Pin number	Type	Description
1	Digital input	L6474 direction input
2	Open drain output	L6474 FLAG output
3	Ground	Ground
4	Supply	EXT_VDD (can be used as external logic power supply)
5	Digital output	SPI master IN slave OUT signal (connected to the L6474 SDO output through daisy chain termination jumper JP2)
6	Digital input	SPI serial clock signal (connected to L6474 CK input)
7	Digital input	SPI master OUT slave IN signal (connected to the L6474 SDI input)
8	Digital input	SPI slave select signal (connected to the L6474 CS input)
9	Digital input	L6474 step-clock input
10	Digital input	L6474 standby/reset input



Table 4. Bill of material

Item	Quantity	Reference	Value	Package
1	1	C1	220 nF/16 V	CAPC-0603
2	1	C2	47 $\mu$ F/6.3 V	CAPC-3216
3	1	C3	100 nF/6.3 V	CAPC-0603
4	1	C4	10 $\mu$ F/4 V	CAPC-3216
5	1	C5	100 nF/4 V	CAPC-0603
6	4	C6,C7,C8,C10	100 nF/50 V	CAPC-0603
7	1	C9A	100 $\mu$ F/63 V	CAPE-R8H12-P35
8	1	C9	100 $\mu$ F/63 V	CAPES-R10HXX
9	1	C11	10 nF/50 V	CAPC-0603
10	1	C13	3.3 nF/4 V	CAPC-0603
11	3	C14,C15,C16	1 nF/4 V	CAPC-0603
12	1	DL1	LED diode (red)	LEDC-0805
13	1	D1	BAV99	SOT-23
14	1	JP1	Jumper - open	JP2SO
15	4	JP2,JP3,JP4,JP5	Jumper - closed	JP2SO
16	3	J1,J5,J6	Screw connector 2 poles	MORSV-508-2P
17	2	J2, J3	Pol. IDC male header vertical 10 poles	CON-FLAT-5X2-180M
18	1	J4	N.M.	STRIP254P-M-2
19	1	J7	N.M.	TPTH-44SQ70
20	4	R1,R3,R4,R6	39 k $\Omega$	RESC-0603
21	1	R2	50 k $\Omega$	TRIMM-100X50X110-64W
22	1	R5	470 $\Omega$	RESC-0603
23	8	TP1,TP2,TP3,TP4,T P5,TP6,TP7,TP8	Test point	TH
24	1	U1	L6474H	HTSSOP28

Figure 3. EVAL6474H - layout (silk screen)

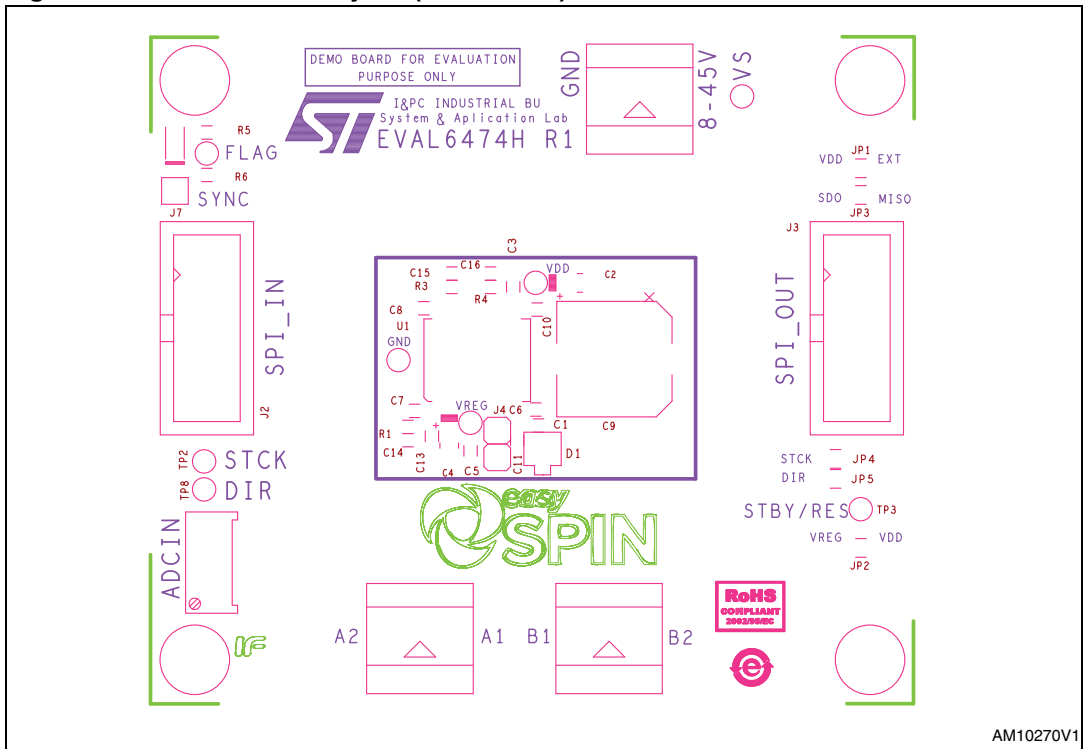


Figure 4. EVAL6474H - layout (top layer)

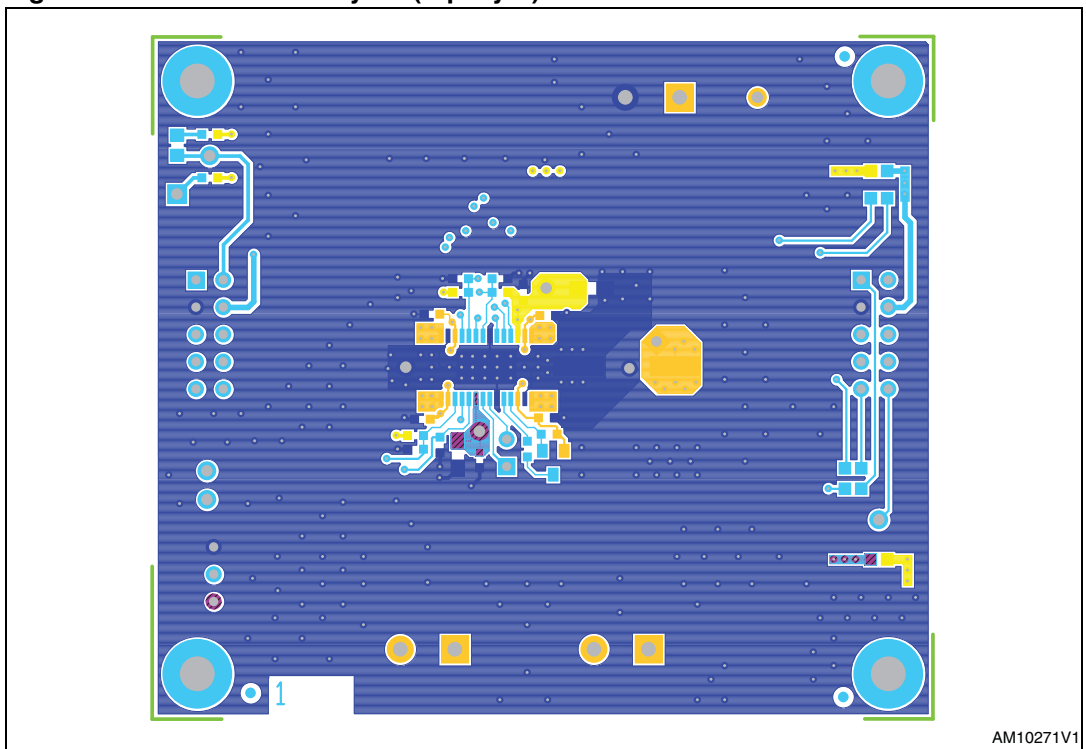


Figure 5. EVAL6474H - layout (inner layer 2)

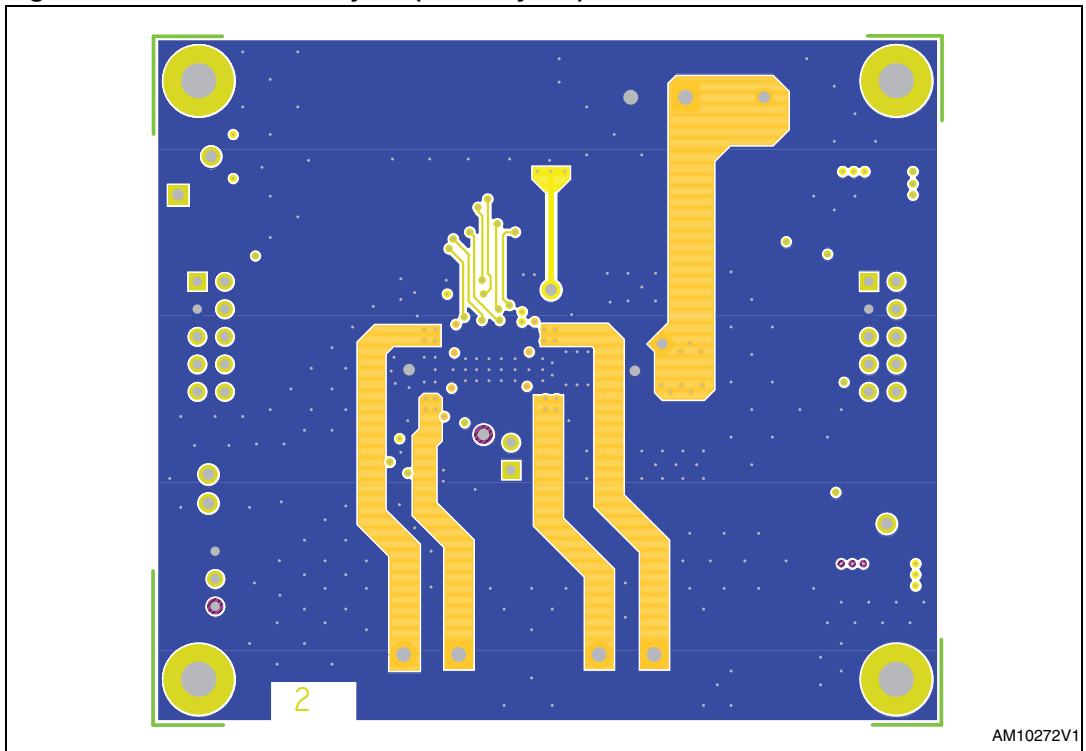


Figure 6. EVAL6474H - layout (inner layer 3)

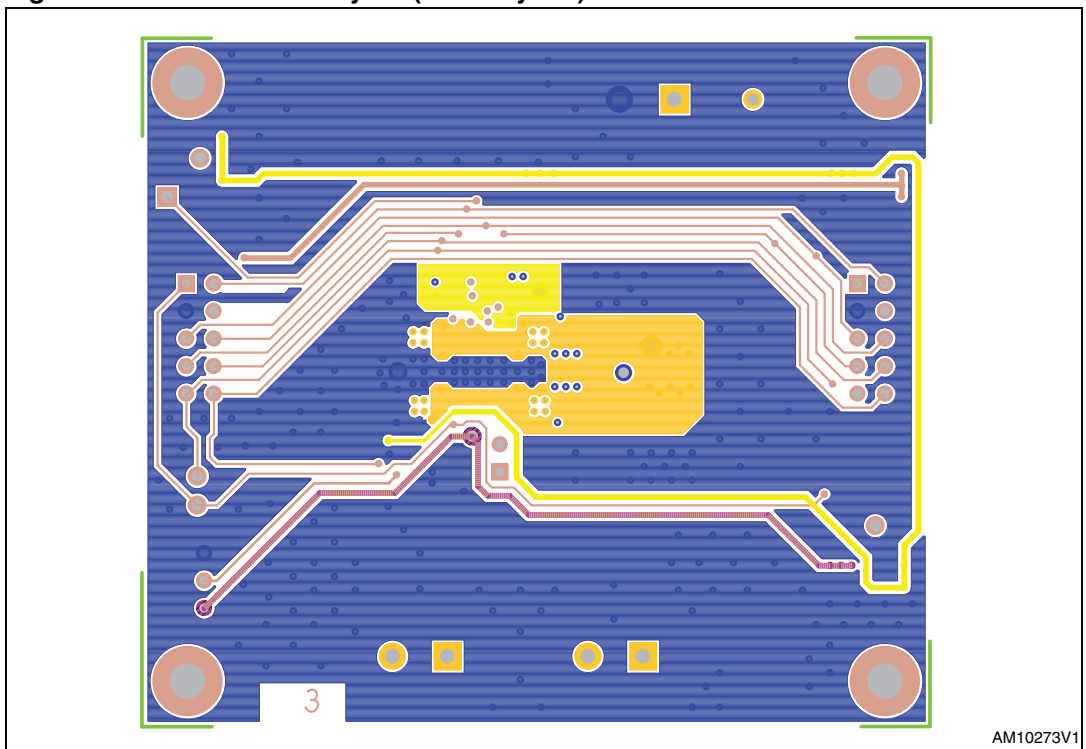
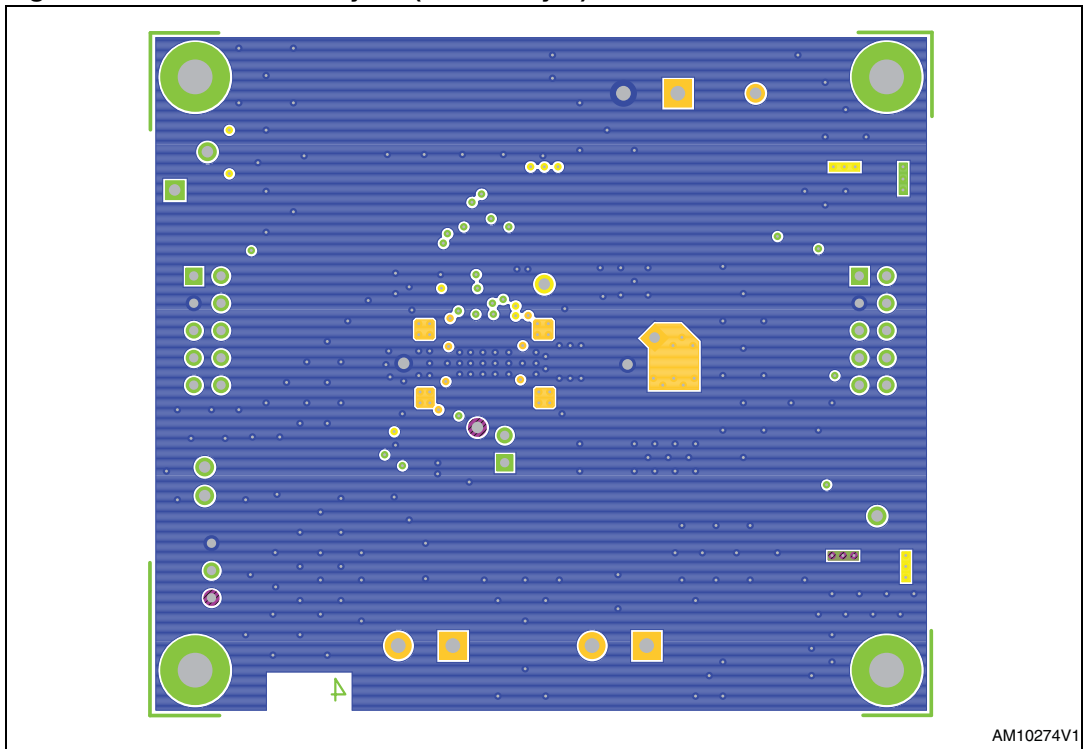
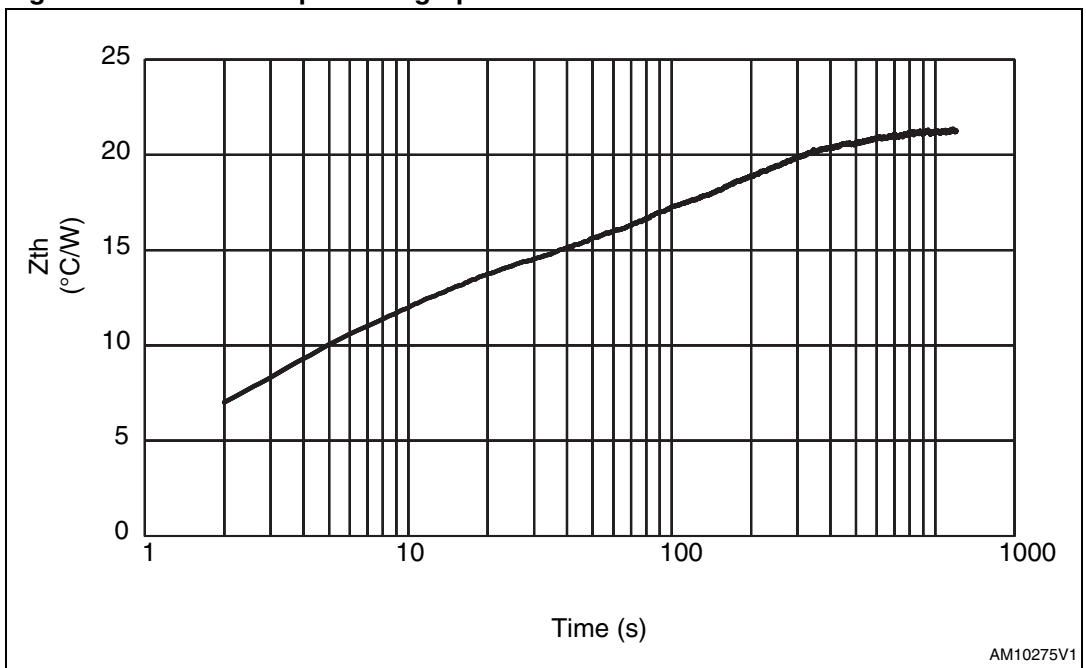


Figure 7. EVAL6474H - layout (bottom layer)



### 1.1 Thermal data

Figure 8. Thermal impedance graph





## 2 Revision history

**Table 5. Document revision history**

Date	Revision	Changes
02-Feb-2012	1	Initial release.

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