

FUJI Power Supply Control IC

DC/DC Power Supply control IC

FA7711V

Application Note

June-2010
Fuji Electric Systems Co.,Ltd.

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CONTENTS

1. Description	4
2. Features	4
3. Outline	4
4. Block diagram	5
5. Pin assignment	5
6. Ratings and characteristics	6
7. Characteristics curves	10
8. Description of each circuit	15
9. Design advice	18
10. Application circuit	25

Note

- Parts tolerance and characteristics are not defined in all application described in this Data book. When design an actual circuit for a product, you must determine parts tolerances and characteristics for safe and stable operation.

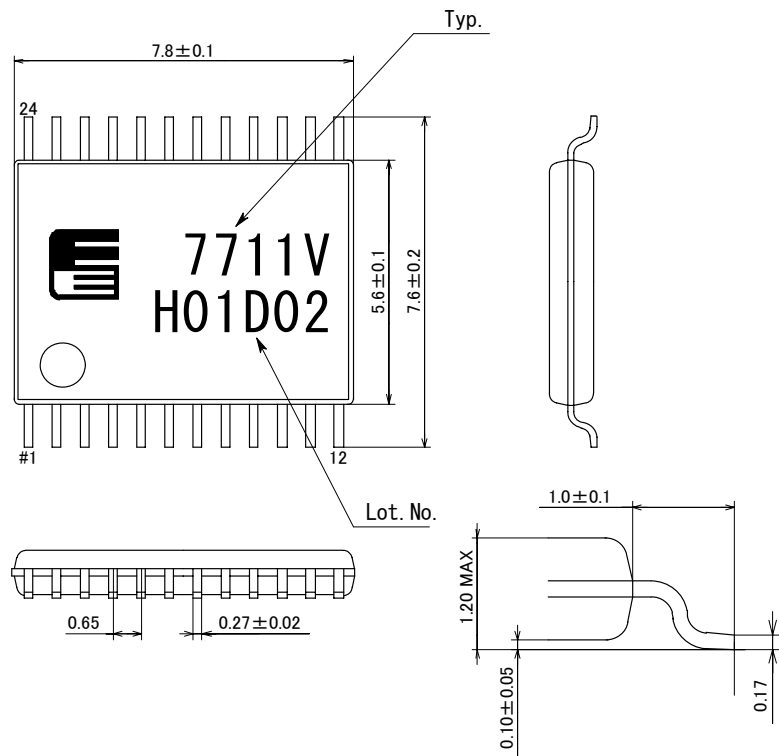
1. Description

FA7711V is a PWM type DC-to-DC converter control IC with 3ch outputs that can directly drive power MOSFETs. CMOS devices with high breakdown voltage are used in this IC and low power consumption is achieved. This IC is suitable for very small DC-to-DC converters because of their small and thin package (1.2mm max.), and high frequency operation (to 800kHz). You can select Pch or Nch of MOSFETs driven, and design any topology of DC-to-DC converter circuit like a buck, a boost, an inverting, a fly-back, or a forward.

2. Features

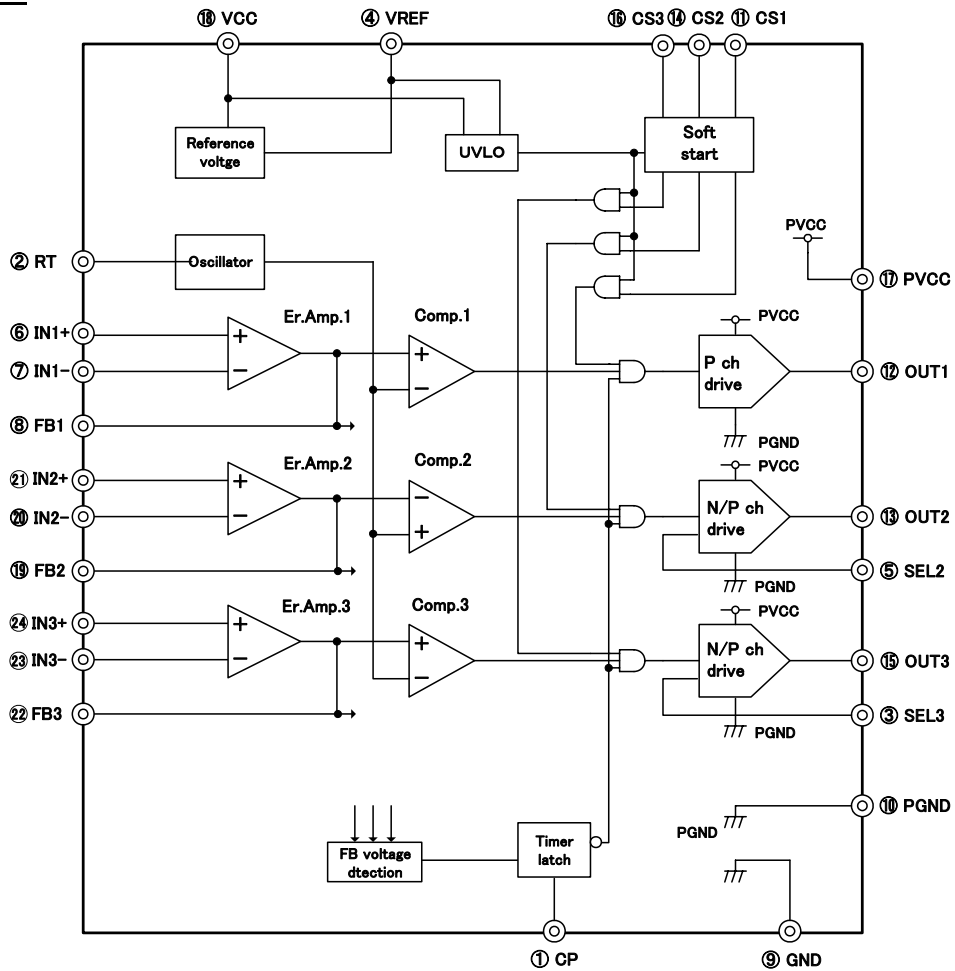
- MOSFET direct driving (Note : This function is available only for that Vcc is below 20V)
- Selectable output stage for Pch/Nch MOSFET on each channel
- Low operating current by CMOS process: 7mA (typ.)
- 3ch PWM control IC
- High frequency operation: 200kHz to 800kHz
- Simple setting of operation frequency by timing resistor
- Soft start function at each channel
- Adjustable maximum duty cycle at each channel
- Built-in under voltage lockout
- High accuracy reference voltage: VREF: 3.7V±1%
- Adjustable built-in timer latch for short-circuit protection
- Thin and small package: TSSOP-24

3. Outline



Unit : mm

4. Block diagram



5. Pin assignment

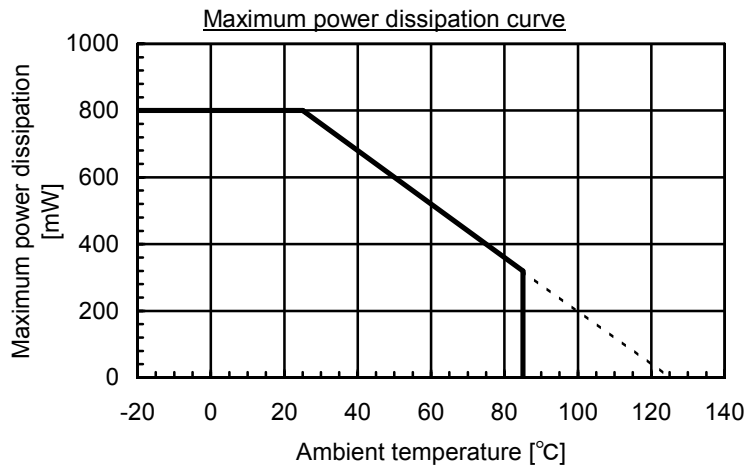
Pin No.	Pin symbol	Description
1	CP	Timer latched short circuit protection
2	RT	Oscillator timing resistor
3	SEL3	Selection of type of driven MOSFET(OUT3)
4	VREF	Reference voltage
5	SEL2	Selection of type of driven MOSFET(OUT2)
6	IN1+	Ch.1 non-inverting input to error amplifier
7	IN1-	Ch.1 inverting input to error amplifier
8	FB1	Ch.1 output of error amplifier
9	GND	Ground
10	PGND	Ground for driver
11	CS1	Soft start for Ch.1
12	OUT1	Ch.1 output
13	OUT2	Ch.2 output
14	CS2	Soft start for Ch.2
15	OUT3	Ch.3 output
16	CS3	Soft start for Ch.3
17	PVCC	Power supply for driver
18	VCC	Power supply
19	FB2	Ch.2 output of error amplifier
20	IN2-	Ch.2 inverting input to error amplifier
21	IN2+	Ch.2 non-inverting input to error amplifier
22	FB3	Ch.3 output of error amplifier
23	IN3-	Ch.3 inverting input to error amplifier
24	IN3+	Ch.3 non-inverting input to error amplifier

6. Ratings and characteristics

(1) Absolute maximum ratings

Item	Symbol	Conditions	Ratings	Units
Power supply voltage (VCC,PVCC pin)	V _{CC}		30	V
SEL2,SEL3 pin voltage	V _{SEL}		- 0.3 to 5.0	V
FB1,IN1-,IN1+,FB2,IN2-,IN2+,FB3,IN3-,IN3+ pin voltage	V _{EA_IN}		- 0.3 to 5.0	V
CS1,CS2,CS3,CP,RT,VREF pin voltage	V _{CTR_IN}		- 0.3 to 5.0	V
OUT1/2/3 pin source current	I _{OUT-}	Ta ≤ 25°C	- 800(peak)	mA
OUT1/2/3 pin sink current	I _{OUT+}		+800(peak)	mA
OUT1/2/3 pin source current	I _{OUT-}		- 50(continuous)	mA
OUT1/2/3 pin sink current	I _{OUT+}		+50(continuous)	mA
Power dissipation	P _d	Ta ≤ 25°C	800	mW
Operating junction temperature	T _j		+125	°C
Operating ambient temperature	T _{OPR}		- 20 to +85	°C
Storage temperature	T _{STG}		- 40 to +125	°C

*1: IC is soldered on glass-epoxy printed board (40mm × 80mm × 1.6mm).
Derating factor Ta ≥ 25°C : 8mW/°C



Thermal resistance: θ_{j-c} (Junction to Case)=70°C/W

IC is soldered on glass-epoxy printed board (40mm × 80mm × 1.6mm).

(2) Recommended operating conditions

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Power supply voltage (VCC)	V _{CC}		4.5	—	28	V
Power supply voltage (PVCC) *2	V _{PCC}		4.5	—	28	V
CS1,CS2,CS3,CP pin voltage	V _{CTR_IN}		0.0	—	4.1	V
SEL2,SEL3 pin voltage	V _{SEL_IN}		0.0	—	4.1	V
IN1-,IN1+,IN2-,IN2+,IN3-,IN3+ pin voltage	V _{EA_IN}		0.0	—	4.1	V
Oscillation frequency	f _{OSC}		200	—	800	kHz
VREF pin capacitance	C _{REF}		1.0	—	4.7	μF
VCC pin capacitance	C _{VCC}		1.0	—	—	μF
PVCC pin capacitance	C _{PVCC}		1.0	—	—	μF
CS1,CS3 pin capacitance	C _{CS1}	Between CS1/3 and GND	0.1	—	—	μF
CS2 pin capacitance	C _{CS2}	Between CS2 and VREF	0.1	—	—	μF
CP pin capacitance	C _{CP}	Between CP and GND	0.01	—	—	μF

*2: Apply the same voltage to Vcc, PVCC pins.

(3)Electrical chracteristics

- The characteristics is based on the condition of $V_{CC}=12V$, $C_{REF}=1.0\ \mu F$, $R_T=9.0k\ \Omega$, $T_a=+25^\circ C$, unless otherwise specified

(1)Reference voltage section (VREF pin)						
Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Reference voltage	V_{REF}		3.663	3.700	3.737	V
Line regulation	V_{REF_LINE}	$V_{CC}=4.5\text{ to }28V, I_{REF}=0mA$	—	± 8	± 25	mV
Load regulation	V_{REF_LOAD}	$I_{REF}=0\text{ to }7mA, V_{CC}=8V\text{ to }28V$	- 20	- 5		mV
		$I_{REF}=0\text{ to }1mA, V_{CC}=4.5V\text{ to }8V$		- 5		
Variation with temperature	V_{REF_TC1}	$T_a=-20\text{ to }+85^\circ C$		± 0.5		%

(2)Oscillator section (RT pin)						
Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Oscillation frequency	f_{OSC}	$R_T=9.0k\ \Omega$	500	560	620	kHz
Line regulation	f_{OSC_LINE}	$V_{CC}=4.5\text{ to }28V$	—	± 1	± 5	%
Variation with temperature	f_{OSC_TC1}	$T_a=-20\text{ to }+85^\circ C$		± 3		%

(3)Error Amplifier section (IN1+, IN1-, FB1, IN2+, IN2-, FB2, IN3+, IN3-, FB3 pin)						
Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input offset voltage	V_{OFFSET}	$V_{IN+}=1.8V, IN+ - IN-$	—	—	± 10	mV
Line regulation (Input offset)	V_{OFF_LINE}	$V_{CC}=4.5\text{ to }28V$		0		mV
Input current	I_{IN}	$V_{IN}=0.0\text{ to }5V$		0		μA
Common mode input voltage	V_{COM}		0.5		2.7	V
Open loop gain	A_{VO}			70		dB
Unity gain bandwidth	f_T			1.5		MHz
Output sink current	I_{SIFB}	$V_{FB}=0.5V, V_{IN-}=V_{REF}, V_{IN+}=1.8V$	1.9	2.7	3.5	mA
Output source current	I_{SOFB}	$V_{FB}=V_{REF}-0.5V, V_{IN-}=0V, V_{IN+}=1.8V$	- 280	- 185	- 90	μA

(4)Soft start section (CS1, CS2, CS3 pin)						
Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Threshold voltage (CS3) (Driving Nch-MOSFET)	$V_{CS3D20N}$	$D_{UTY3}=20\%, V_{FB3}=2.8V$	1.4	1.5	1.6	V
	$V_{CS3D80N}$	$D_{UTY3}=80\%, V_{FB3}=2.8V$	2.0	2.1	2.2	V
Threshold voltage (CS1/3) (Driving Pch-MOSFET)	$V_{CS1/3D0P}$	$D_{UTY1/3}=20\%, V_{FB1/3}=2.8V$	1.4	1.5	1.6	V
	$V_{CS1/3D20P}$	$D_{UTY1/3}=80\%, V_{FB1/3}=2.8V$	2.0	2.1	2.2	V
Threshold voltage (CS2) (Driving Nch-MOSFET)	$V_{CS2D20N}$	$D_{UTY2}=20\%, V_{FB2}=0.8V$	2.0	2.1	2.2	V
	$V_{CS2D80N}$	$D_{UTY2}=80\%, V_{FB2}=0.8V$	1.4	1.5	1.6	V
Threshold voltage (CS2) (Driving Pch-MOSFET)	$V_{CS2D20P}$	$D_{UTY2}=20\%, V_{FB2}=0.8V$	2.0	2.1	2.2	V
	$V_{CS2D80P}$	$D_{UTY2}=80\%, V_{FB2}=0.8V$	1.4	1.5	1.6	V

(5)Pulse width modulation section (FB1, FB2, FB3 pin)						
Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Threshold voltage (FB3) (Driving Nch-MOSFET)	V _{FB3D20N}	D _{UTY3} =20%, V _{CS3} =V _{REF}		1.5		V
	V _{FB3D80N}	D _{UTY3} =80%, V _{CS3} =V _{REF}		2.1		V
Threshold voltage (FB1/3) (Driving Pch-MOSFET)	V _{FB1/3D20P}	D _{UTY1/3} =20%, V _{CS1/3} =V _{REF}		1.5		V
	V _{FB1/3D80P}	D _{UTY1/3} =80%, V _{CS1/3} =V _{REF}		2.1		V
Threshold voltage (FB2) (Driving Nch-MOSFET)	V _{FB2D20N}	D _{UTY2} =20%, V _{CS2} =0V		2.1		V
	V _{FB2D80N}	D _{UTY2} =80%, V _{CS2} =0V		1.5		V
Threshold voltage (FB2) (Driving Pch-MOSFET)	V _{FB2D20P}	D _{UTY2} =20%, V _{CS2} =0V		2.1		V
	V _{FB2D80P}	D _{UTY2} =80%, V _{CS2} =0V		1.5		V

(6)Under voltage lockout section (VCC pin)						
Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
ON threshold voltage of VCC	V _{UVLOON}		2.6	3.3	4.0	V
Hysteresis voltage	V _{UVLOHYS}			0.1		V

(7)Timer latch protection section (CP pin)						
Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Threshold voltage of FB1	V _{THFB1ON}	*7-1	2.8	3.0	3.2	V
Threshold voltage of FB2	V _{THFB2ON}	*7-2	0.4	0.6	0.8	V
Threshold voltage of FB3	V _{THFB3ON}	*7-3	2.8	3.0	3.2	V
Charge current of CP	I _{CP}	V _{CP} =0.5V, V _{FB1} =V _{REF} - 0.5V	- 3.5	- 2.5	- 1.5	μA
Threshold voltage of CP	V _{THCPON}		2.8	3.0	3.2	V

*7-1:The current source of the CP pin operates when the voltage of FB1 exceeds the threshold voltage as shown in the table

*7-2:The current source of the CP pin operates when the voltage of FB2 fall below the threshold voltage as shown in the table

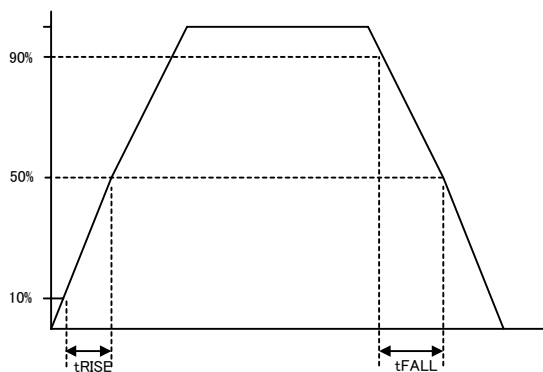
*7-3:The current source of the CP pin operates when the voltage of FB3 exceeds the threshold voltage as shown in the table

(8)Output section (OUT1, OUT2, OUT3, SEL2, SEL3 pin)						
Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
High side on resistance	R _{ONHI}	I _{OUT} =- 100mA		3	5	Ω
Low side on resistance	R _{ONLO}	I _{OUT} =+100mA		3	5	Ω
Rise time (Driving Pch-MOSFET)	t _{RISEP}	V _{CC} - OUT:7 Ω +2000pF *8-1		30		ns
Fall time (Driving Pch-MOSFET)	t _{FALLP}			30		
Rise time (Driving Nch-MOSFET)	t _{RISEN}	OUT- GND:7 Ω +2000pF *8-2		30		ns
Fall time (Driving Nch-MOSFET)	t _{FALLN}			30		
SEL2/3 pin voltage for driving Nch-MOSFET	V _{SELN}		0.0	—	0.35	V
SEL2/3 pin voltage for driving Pch-MOSFET	V _{SELP}		V _{REF} - 0.35	—	V _{REF}	V

(9)Overall section						
Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Operating mode supply current	I _{CCOP}	Operating mode		7	9	mA
		R _T =9.0k Ω				
	R _T =5.7k Ω		8	11		
	I _{CCD100}	latch mode		4		mA

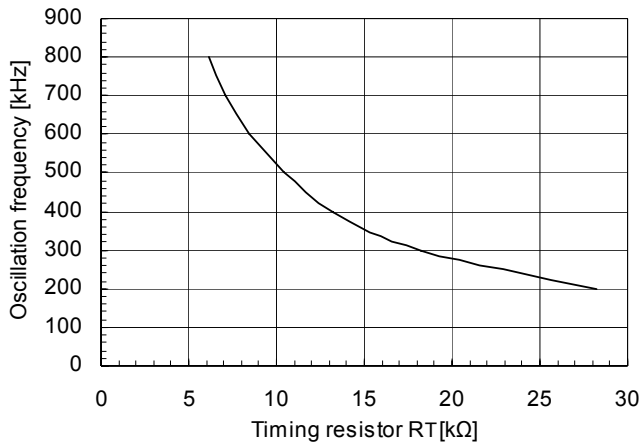
*8-1

*8-2

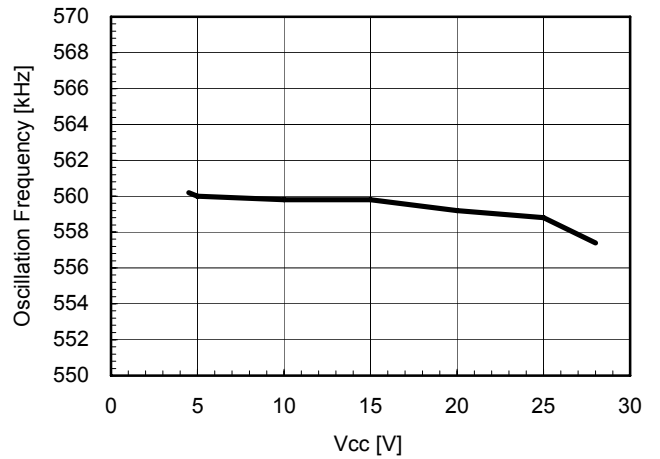


7. Characteristic curves

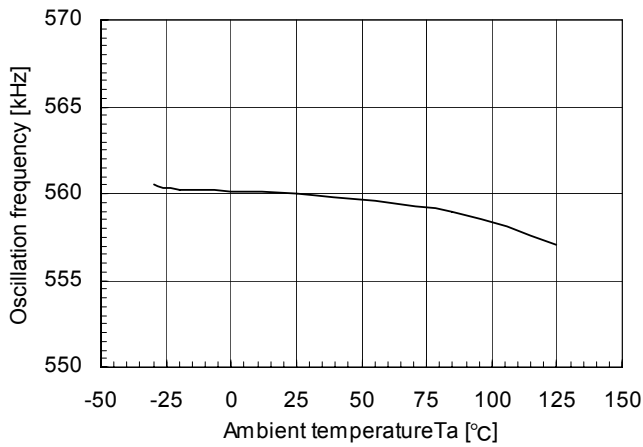
Timing resistor vs. Oscillation frequency



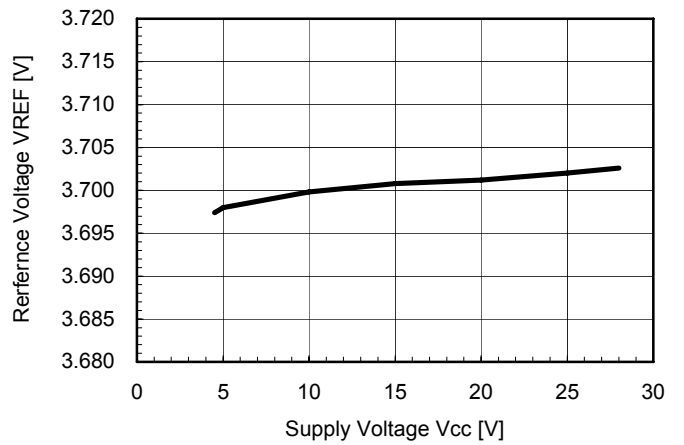
Oscillation Frequency vs. Supply Voltage



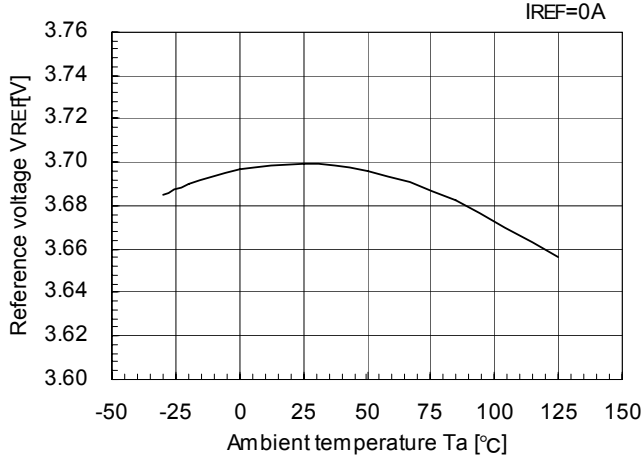
Oscillation frequency vs. Ambient temperature



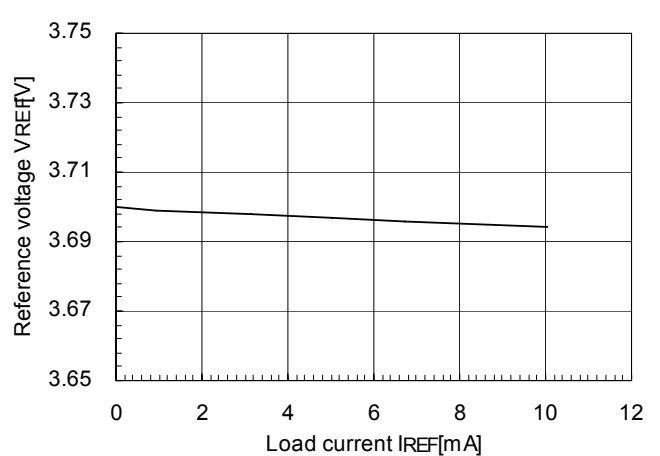
Reference Voltage vs. Supply Voltage IREF = 0mA

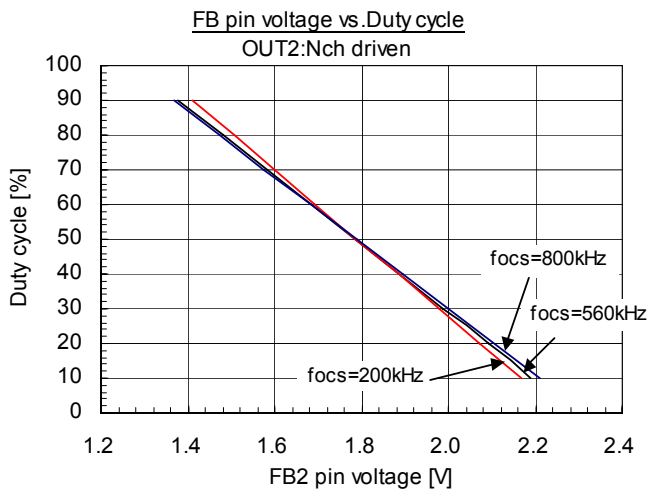
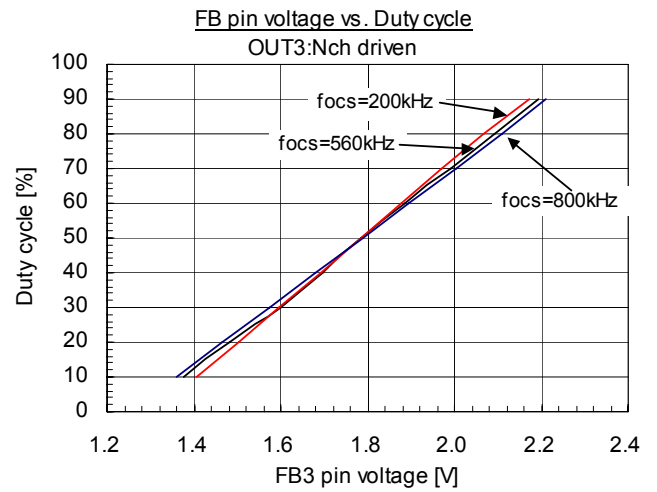
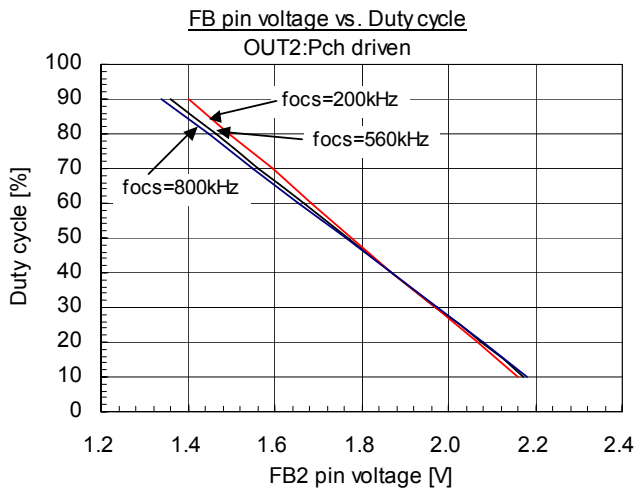
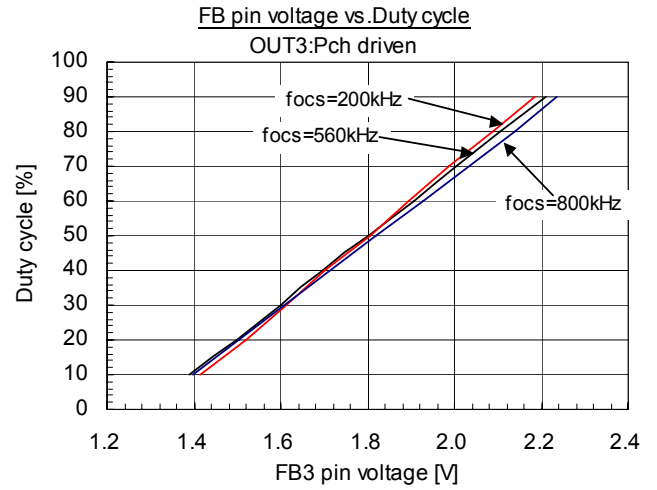
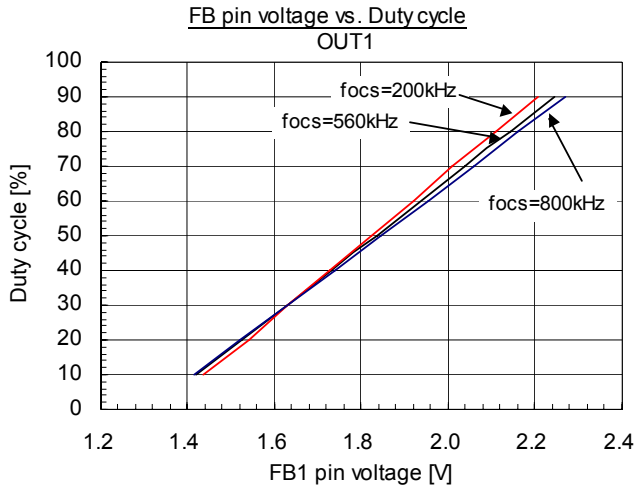


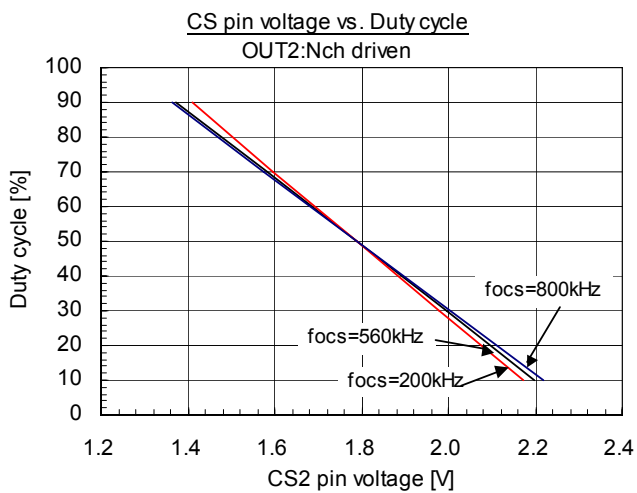
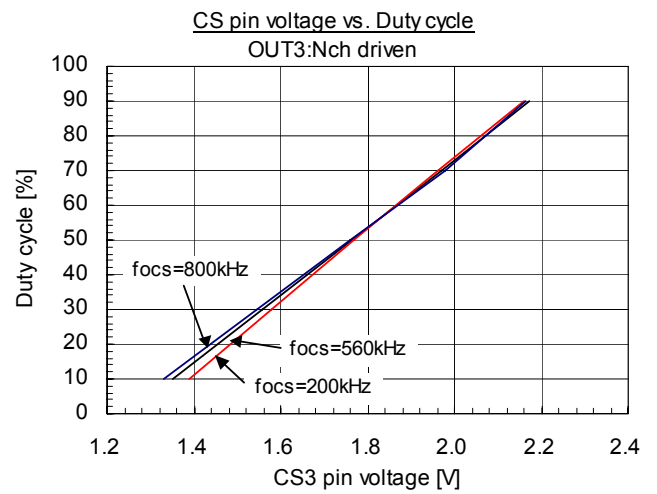
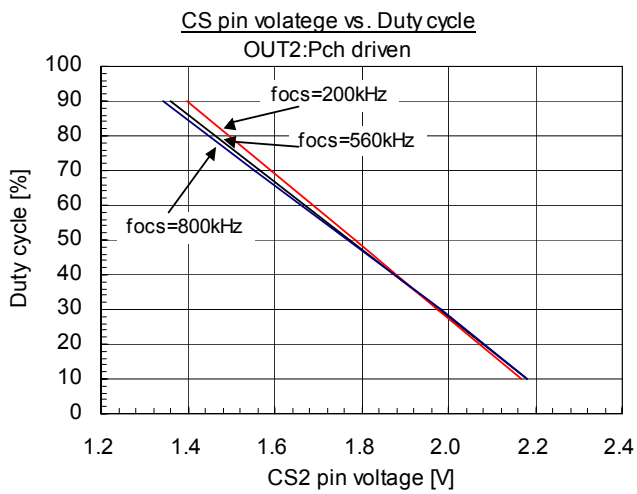
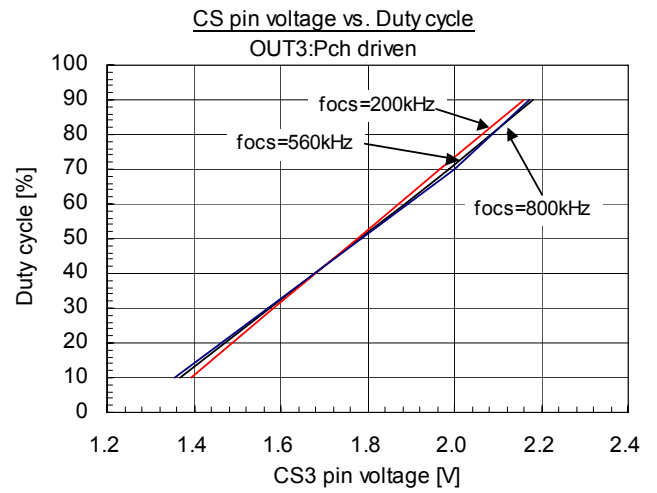
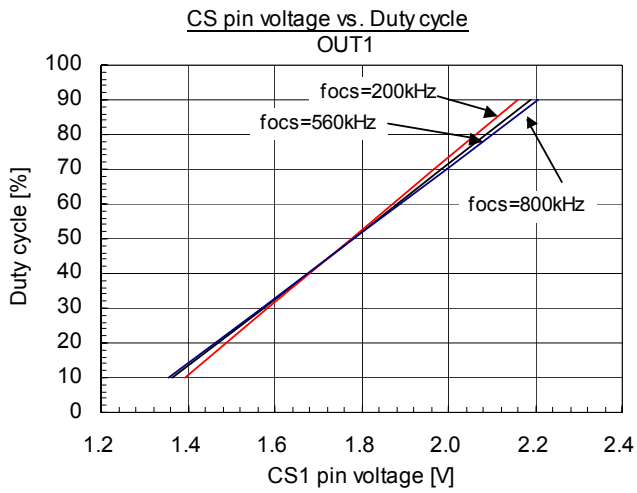
Reference voltage vs. Ambient temperature IREF=0A



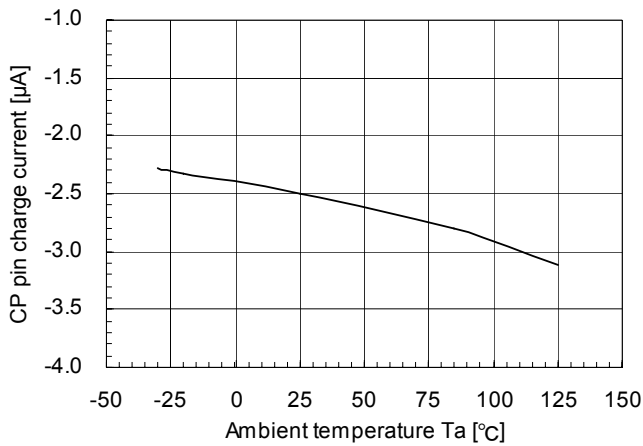
Reference voltage vs. Load current



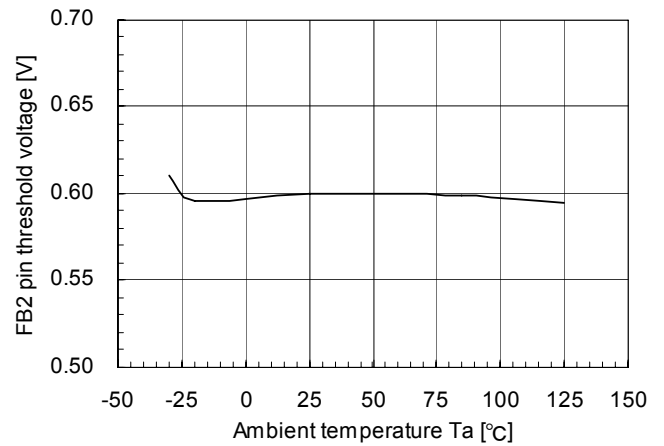




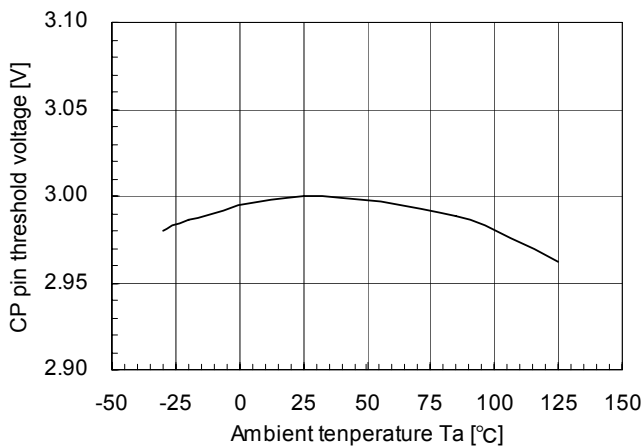
CP pin charge current vs. Ambient temperature



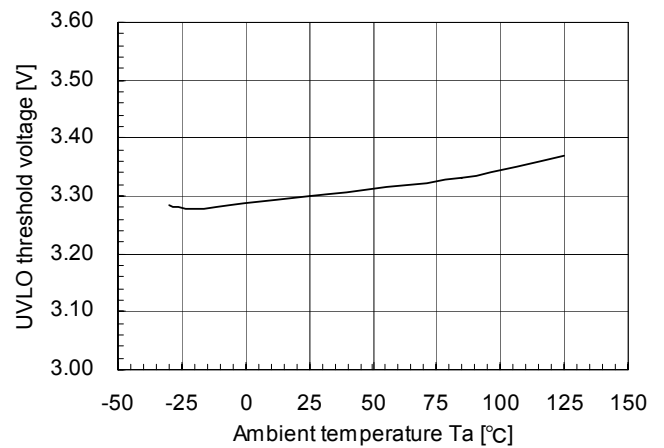
FB2 pin threshold voltage vs. Ambient temperature



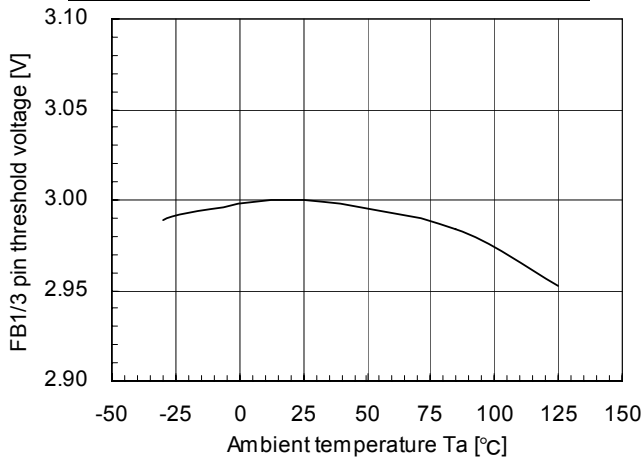
CP pin threshold voltage vs. Ambient temperature



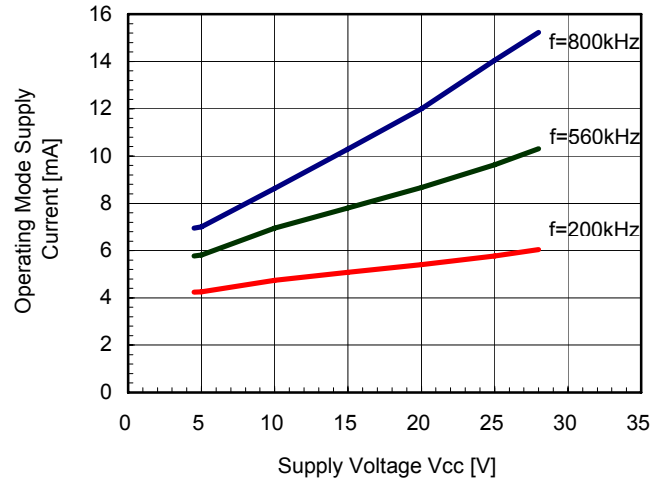
UVLO threshold voltage vs. Ambient temperature



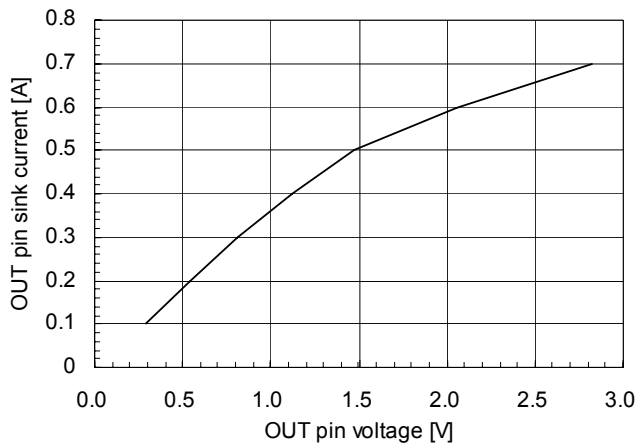
FB1/3 pin threshold voltage vs. Ambient temperature



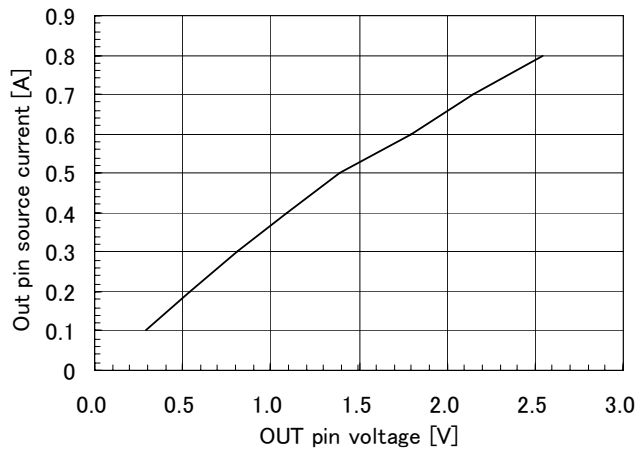
Operationg Mode Supply Current vs. Supply Voltage



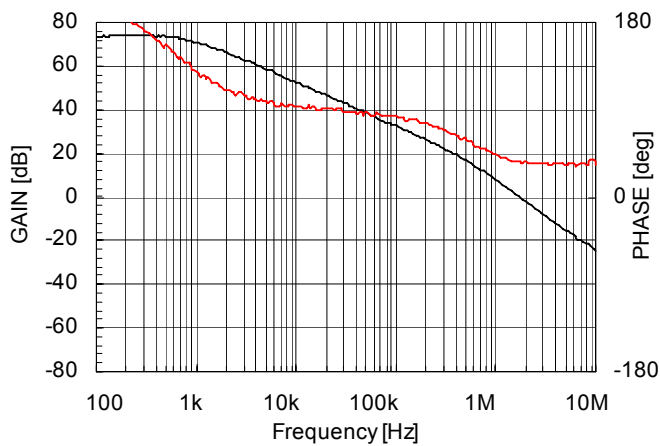
OUT pin Low side voltage vs. Sink current



OUT pin High side voltage vs. Source current



Error Amplifier gain and Phase vs. frequency



8. Description of each circuit

(1) Reference voltage circuit

The circuit generates the reference voltage (VREF) of $3.70V \pm 1\%$ compensated in temperature from VCC voltage. This voltages start to output when the undervoltage lockout protection (UVLO) is cancelled, and they stabilize after the supply voltage (VCC) reaches up to approx. 4.0V or higher.

The voltage (VREF) outputs externally from REF Pin, therefore, it can serve as a stabilized power source for reference voltage of Error Amplifier and maximum output duty setting or the like. The output current circuit should be within 1mA. (In case of $V_{CC}=8V$ to $28V$ should be within 7mA) The V_{REF} voltage also is used as a regulated power supply for IC's internal blocks.

VREF pin have to connect capacitors C_{REF} for in order to stabilize voltages (To determine capacitance, refer to recommended operating conditions).

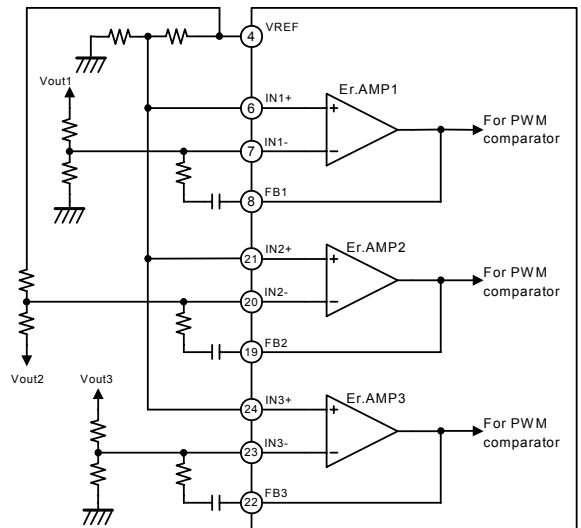


Fig.3

(2) Oscillator

The oscillator generates triangular waveforms by charging and discharging the built-in capacitor. Any desired oscillation frequency can be obtained by setting the value of the resistor connected to RT Pin (Fig. 1).

The voltage oscillates between approximately 1.3V and 2.3V in charging and discharging with almost the same gradients (Fig. 2). Your desired oscillation frequency can be determined by changing the gradient using the resistor (R_T) connected to RT Pin. (Large R_T : Low frequency, small R_T : High frequency) The waveforms of oscillator cannot be observed from the outside because a Pin for this purpose is not provided.

Approximately DC 1V is output to RT Pin.

The oscillator output is connected to PWM comparator.

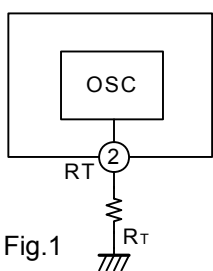


Fig.1

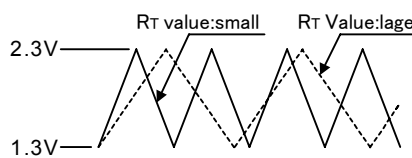


Fig.2

(4) PWM comparator

The PWM output generates from the oscillator output, the error amplifier output (FB1, FB2 and FB3) and CS voltage (CS1, CS2 and CS3) (Fig. 4). The oscillator output is compared with the preferred lower voltage between FB and CS for ch1 and ch3. While the preferred voltage is lower than oscillator output, the PWM output is low. While the preferred voltage is higher than oscillator output, the PWM output is high. Since the phase of Ch2 is the opposite phase of ch1 and ch3, higher voltage between FB2 and CS2 is preferred and while the preferred voltage is lower than the oscillator output, the PWM output 2 is high. (Cannot be observed externally)

The output duty changes sharply around the minimum and the maximum output duty. This phenomenon occurs more conspicuously when operating in a high frequency (i.e. when the pulse width is narrow). Cautious care must be taken when using high frequency.

The output polarity of OUT1, OUT2 changes according to the condition of SEL pin. (See Fig. 6)

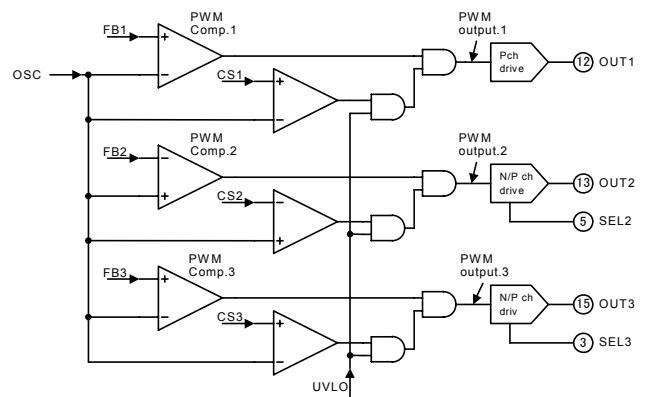


Fig.4

(3) Error amplifier

Error Amplifier has the inverting input $IN^*(-)$ Pin (Pin7, Pin20 and pin23) and non-inverted input $IN^*(+)$ Pin (Pin6, Pin21 and pin24) outputting externally, various circuit can be designed by kinds of external circuit structures. FB Pins (Pin, Pin19 and pin22) are the outputs of Error Amplifiers. Voltage Gain and phase compensation can be set by connecting a capacitor (C) and a resistor (R) between FB Pin and $IN^*(-)$ Pin.(Fig. 3) For more information about the connection for each output voltage of power supply, refer to Design Advice.

(5) Soft start circuit

This IC has a soft start function to protect DC-to-DC converter circuits from damage when starting operation. CS1 pin (Pin11), CS2 pin (pin14) and CS3 pin (Pin16) are used for soft start function of ch1, ch3 and ch2 respectively. (Fig. 5)

When the supply voltage is applied to the VCC pin and UVLO is cancelled, capacitor Ccs1, Ccs2 and Ccs3 is charged by VREF through the resistor Rcs1, Rcs2 or Rcs3. Therefore, CS1 and CS3 voltage gradually increases and CS2 voltage gradually decreases. Since CS1, CS2 and CS3 pin are connected to the PWM comparator internally, the pulses gradually widen and then the soft start function operates. (Fig. 6)

The maximum duty cycle can be set by using the CS pins. (See Design Advice about the detail)

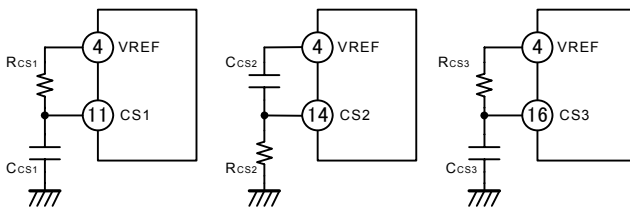


Fig.5

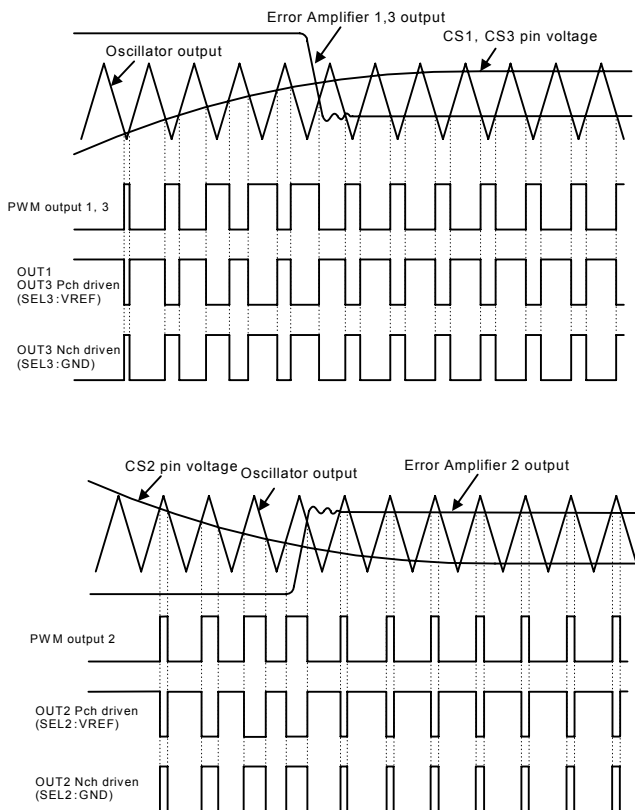


Fig.6

(6) Timer latched short-circuit protection

This IC has the timer latch short-circuit protection circuit. This circuit cuts off the output of all channels when the output voltage of DC-to-DC converter drops due to short circuit or overload. To set delay time for timer latch operation, a capacitor Ccp should be connected to the CP pin (Fig. 7).

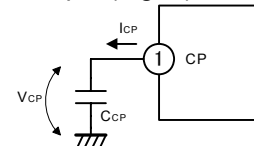


Fig.7

When one of the output voltage of the DC-to-DC converter drops due to short circuit or overload, the FB1 and FB3 pin voltage increases up to around the VREF voltage for ch1 and ch3, or the FB2 pin voltage drops down to around 0 V for ch2. When FB1 and FB3 pin voltage exceeds 3.2V(max.) or FB2 pin voltage falls below 0.4V(min.), constant-current source (2.5μA typ.) starts charging the capacitor Ccp connected to the CP pin. If the voltage of the CP pin exceeds 3.2 V (max.), the circuit regards the case as abnormal. Then the IC is set to off latch mode and the output of all channels is shut off, (Fig. 8) and the current consumption become 4mA(typ.) The period (tp) between the occurrence of short-circuit in the converter output and setting to off latch mode can be calculated by the following equation:

$$tp[s] = C_{CP} \times \frac{V_{THCPON}}{I_{CP}}$$

V_{THCPON}: CP pin latched mode threshold voltage [V]

I_{CP}: CP charge source current[μA]

C_{CP}: capacitance of CP pin capacitor[μF]

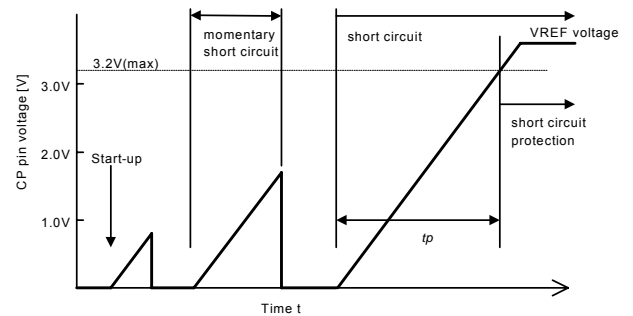


Fig.8

You can reset off latched mode of the short-circuit protection by either of the following ways about 1) CP pin, or 2) VCC pin:

- 1) CP voltage = 0V
- 2) VCC voltage UVLO voltage (3.3V, typ.) or below

If the timer-latched mode is not necessary, connect the CP pin to GND.

(7) Output circuit

The IC contains a push-pull output stage and can directly drive MOSFETs. The maximum peak current of the output stage is sink current of +800mA, and source current of - 800mA. The IC can also drive NPN and PNP transistors. The maximum current in such cases is ± 50 mA. You must design the output current considering the rating of power dissipation. (See Design Advice)

You can switch the types of external discrete MOSFETs by wiring of the SEL pins (Pin 3, Pin 5). For driving Nch MOS, connect the SEL pins to GND. For driving Pch MOS, connect the SEL pins to VREF. You can design buck converter or inverting converter by driving Pch MOS, and boost converter by driving Nch MOS.

Connect them either to GND or to VREF surely.

(8) Under voltage lockout circuit (UVLO)

The IC contains a under voltage lockout circuit to protect the circuit from the damage caused by malfunctions when the supply voltage drops. When the supply voltage rises from 0V, the IC starts to operate at Vcc of 3.3V(typ.) and outputs generate pulses. If a drop of the supply voltage occurs, it stops output at Vcc of 3.2V(typ.). When it occurs, the CS1 and CS3 pin are turned to low level and the CS2 pin to high level, and then these pins are reset.

9. Design Advice

(1) Setting the oscillation frequency

As described at Section 8-(2), "Description of Each Circuit," a desired oscillation frequency can be determined by the value of the resistor connected to the RT pin. When designing an oscillation frequency, you can set any frequency between 200kHz and 800kHz. You can obtain the oscillation frequency from the characteristic curve "Oscillation frequency (fosc) vs. timing resistor resistance (RT)" or the value can be approximately calculated by the following expression.

$$f_{osc} = 4.1 \times 10^3 \times R_T^{-0.905}$$

$$R_T = \left(\frac{4.1 \times 10^3}{f_{osc}} \right)^{1.105}$$

fosc: oscillation frequency [kHz]

RT : timing resistor [kΩ]

This expression, however, can be used for rough calculation, the obtained value is not guaranteed. The operation frequency varies due to the conditions such as tolerance of the characteristics of the ICs, influence of noises, or external discrete components. When determining the values, examine the effectiveness of the values in an actual circuit. The timing resistor RT should be wired to the GND pin as shortly as possible because the RT pin is a high impedance pin and is easy affected by noises.

(2) Determining soft start period

The period from the start of charging the capacitor CCS to widening n% of output duty cycle can be roughly calculated by the following expression: (see Fig. 5 for symbols)

For CS1:

$$ts1[ms] = R_{CS1} \cdot C_{CS1} \cdot \ln \left(\frac{V_{REF}}{V_{REF} - V_{CS1n}} \right)$$

For CS2

$$ts2[ms] = R_{CS2} \cdot C_{CS2} \cdot \ln \left(\frac{V_{REF}}{V_{CS2n}} \right)$$

For CS3

$$ts3[ms] = R_{CS3} \cdot C_{CS3} \cdot \ln \left(\frac{V_{REF}}{V_{REF} - V_{CS3n}} \right)$$

CCS1, CCS2, CCS3:

Capacitance connected to CS* pin [μF]

RCS1, RCS2, RCS3:

Resistance connected to CS* pin [kΩ]

VCS*n represents the voltage of CS Pin in the output duty of n%, and it changes according to the operation frequency. The value is obtained simply from the chart of "CS Pin voltage vs. output duty cycle" characteristic curves.

Charging of CS Pin begins after UVLO is cancelled. Note that the time from power-on of Power supply to start of charging Ccs* is t0, which is not zero as described in Fig. 8. Be careful.

To reset the soft start function, the voltage of CS pin is discharged with internal switch triggered by lowering the voltage of Power supply below the voltage of UVLO (3.3V, typ.). If Power supply restarts before the voltage is sufficiently discharged, the soft start function might not properly operate. Accordingly, cautious care must be taken about it.

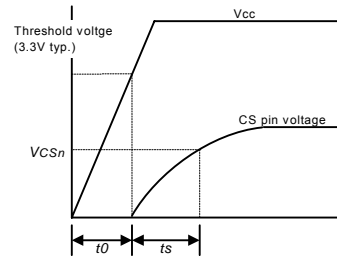


Fig.9

(3) Setting the maximum output duty

If you need to control the maximum output duty in the DC-DC converter circuit, you can control pulse width by connecting VREF pin to CS pin divided with resistors, as described in Fig. 10. The output duty of the voltage of CS pin in this case changes according to the operation frequency, as described in the chart of "CS pin voltage vs. Duty cycle" characteristic curves. Set the output duty accordingly based on your required operation frequency.

When the maximum duty cycle is limited, CS pin voltage at start-up is described in Fig. 11, and the approximate value of soft start period can be obtained by the following expressions:

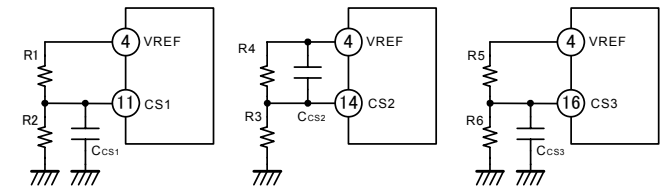


Fig.10

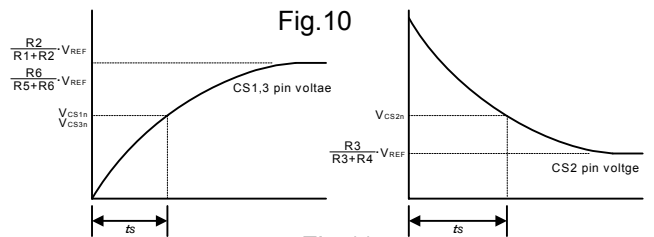


Fig.11

For CS1

$$ts1[ms] = R_0 \cdot C_{CS1} \cdot \ln \left(\frac{V_{CS1}}{V_{CS1} - V_{CS1n}} \right)$$

$$R_0 = \frac{R_1 \cdot R_2}{R_1 + R_2}$$

$$V_{CS1} = \frac{R_2}{R_1 + R_2} \cdot V_{REF}$$

For CS2

$$ts2[ms] = R_0 \cdot C_{CS2} \cdot \ln \left(\frac{V_{REF} - V_{CS2}}{V_{CS2n} - V_{CS2}} \right)$$

$$R_0 = \frac{R_3 \cdot R_4}{R_3 + R_4}$$

$$V_{CS2} = \frac{R_3}{R_3 + R_4} \cdot V_{REF}$$

For CS3

$$ts_3[ms] = R_0 \cdot C_{CS3} \cdot \ln\left(\frac{V_{CS3}}{V_{CS3} - V_{CS3n}}\right)$$

$$R_0 = \frac{R_5 \cdot R_6}{R_5 + R_6} \quad V_{CS3} = \frac{R_6}{R_5 + R_6} \cdot V_{REF}$$

$C_{CS1}, C_{CS2}, C_{CS3}$:

Capacitance connected to CS* pin [μ F]

R1 to R6 : Resistance connected to CS* pin [k Ω]

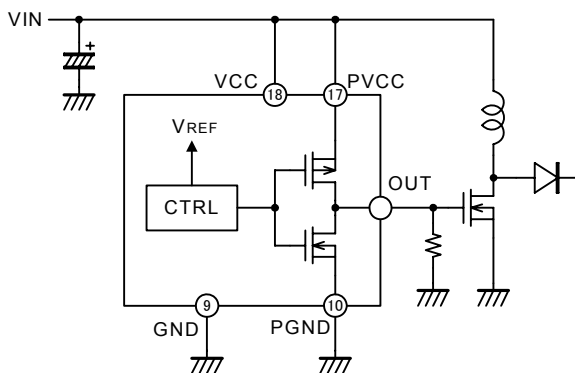
The output duty changes sharply around the minimum and the maximum output duty. This phenomenon occurs more conspicuously when operating in a high frequency (i.e. when the pulse width is narrow). Cautious care must be taken when using high frequency.

(4) Pull-up/Pull-down resistor at the output section

The power supply for control blocks of OUT pin drivers is the VREF. The VREF voltage is not operated at the condition of IC's power supply VCC below the UVLO voltage. Therefore, OUT* pins are unstable at VCC below the UVLO voltage.

If you have this condition of VCC and possibility of some trouble by unstable OUT* pins, connect pull up or pull down resistor to OUT* pins. (Fig.12)

For Nch driven



For Pch driven

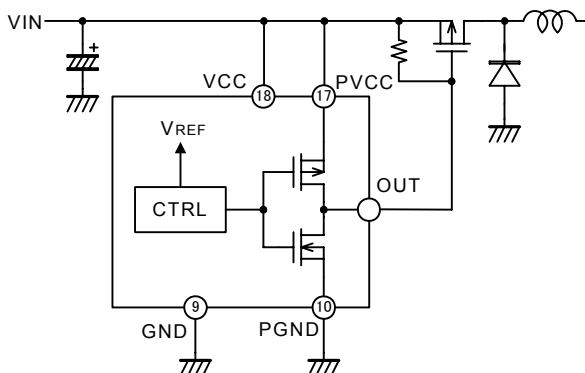


Fig.12

(5) Restriction and recommended operating conditions of external discrete component

To achieve a stable operation of the IC, the value of external discrete components connected to VCC, PVCC, VREF, CS, CP pins should be within the recommended operating conditions. And the voltage and the current applied to each pin should be also within the recommended operating conditions.

If the pin voltage of OUT1, OUT2, or VREG becomes higher than the VCC pin voltage, the current flows from the pins to the VCC pin because parasitic three diode exist between the VCC pin and these pins. Be careful not to allow this current to flow.

(6) Performance of output stage

The performance of output stages is the sink current (peak) of 800mA of and the source current (peak) of -800mA.

Switching speed is effected by external switching device, especially at high frequency, so examine the external switching device and frequency carefully.

If the performance of the ICs is not sufficient for your design, consider adding a buffer circuit to improve the performance.

(7) Loss Calculation

Since it is difficult to measure IC loss directly, the calculation to obtain the approximate loss of the IC connected directly to a MOSFET is described below.

When the supply voltage is VCC, the current consumption of the IC is ICCOP, the total input gate charge of the driven MOSFET is Qg and the switching frequency is fsw, the total loss Pd of the IC can be calculated by:

$$Pd \cong VCC \cdot (IC_{COP} + Qg \cdot fsw)$$

The value in this expression is influenced by the effects of the dependency of supply voltage, the characteristics of temperature, or the tolerance of parameter. Therefore, evaluate the appropriateness of IC loss sufficiently considering the range of values of above parameters under all conditions.

Example)

ICCOP=7mA for VCC=12V in the case of a typical IC from the characteristics curve. Qg=10nC, fsw=560kHz, the IC loss "Pd" is as follows.

$$Pd \cong 12 \cdot (7mA + 10nC \cdot 560kHz) \cong 151mW$$

if two MOSFETs are driven under the same condition for 3 channels, Pd is as follows:

$$Pd \cong 12 \cdot \{7mA + 3 \cdot (10nC \cdot 560kHz)\} = 286mW$$

(8) Attention for driving bipolar transistor

If you use bipolar transistor as a switching device, connect resistor R_B between Base of transistor and OUT* pin, else there is a possibility of destroy the IC by over current because OUT* pin driver does not contain a current limit resistor. (Fig.13) Output current of OUT* pins are below 40mA (continuous).

The connection of capacitor C_B is effective for speed up the switching.

(9) ON/OFF control

ON/OFF control using CS pin is not available when timer latch function is enable. In order to carry out ON/OFF control with CS pin, CP pin should be connected to GND so that timer latch function will be disable as shown in Fig.14.

For ch.1 and ch.3, output pulses are disabled by lowering CS pin voltage around zero. Ch.1 is controlled by CS1 pin and ch.3 is controlled by CS3. For ch.2, pulling up CS2 pin voltage to VREF voltage disables output pulses.

Each channel will re-start operation with soft-start function when CS pin is opened.

Fig.15 shows ON/OFF control method for Ch.1 and Ch.3 when timer latched short protection is used for all channels.

Please take care of that Ch.2 is not suitable for ON/OFF control, because the error amplifier of Ch.2 sinks large current (much larger than 2.7mA) for High Voltage of FB2 pin to stop switching of OUT2 pin.

The calculation example of ON/OFF circuit in Fig.15 is as follows.

VREF -> CS1 maximum current " I_{cs1max} "
 = V_{REF} / R_{18} (ex. $3.7V / 100k\ ohm = 37\mu A$)
 VREF -> CS3 maximum current " I_{cs3max} "
 = V_{REF} / R_{38} (ex. $3.7V / 100k\ ohm = 37\mu A$)
 Error Amp. Output Source Current " I_{SOFB} "
 = $185\mu A$ (typ.) for FB1 pin and FB3 pin

The base current ratio of Q_{FB}^* and Q_{CS}^* should be same as the collector current ratio for each channel.

(above case : collector current ratio = $185 / 37 = 5$)
 -> Base resistor ratio = $R_{56} / R_{55} = R_{53} / R_{52} = 5$)

Base resistor voltage drop should be larger than 300mV in order to obtain good sharing of base current for Q_{FB}^* and Q_{CS}^* .

Here, assuming h_{FE} less than 100 of Q^{**} , each base current are over $1.85\mu A$ and over $0.37\mu A$.

If R_{57} and R_{58} values to flow current over $(1.85\ \mu A + 0.37\ \mu A)$ are designed and

$R_{55} = R_{52} = 200k\ ohm$ and $R_{56} = R_{53} = 1M\ ohm$ are selected, base resistor voltage of R_{52} , R_{53} , R_{55} and R_{56} are over 370mV and these satisfy " 300mV condition ". Therefore, this condition achieves normal transistor operation.

Resistance of R_{57} and R_{58} should be smaller than 20% of above condition in order to obtain small h_{FE} of " 20 " which achieves low saturation voltage of Q^{**} .

In this case, if $V_{CC} = 17V$ (min.) and voltage drop of R_{57} and $R_{58} = V_{CC} - 2V$,

$$R_{57}\ or\ R_{58} < 20\% * (17V - 2V) / (1.85\ \mu A + 0.37\ \mu A) = 1.35\ M\ ohm$$

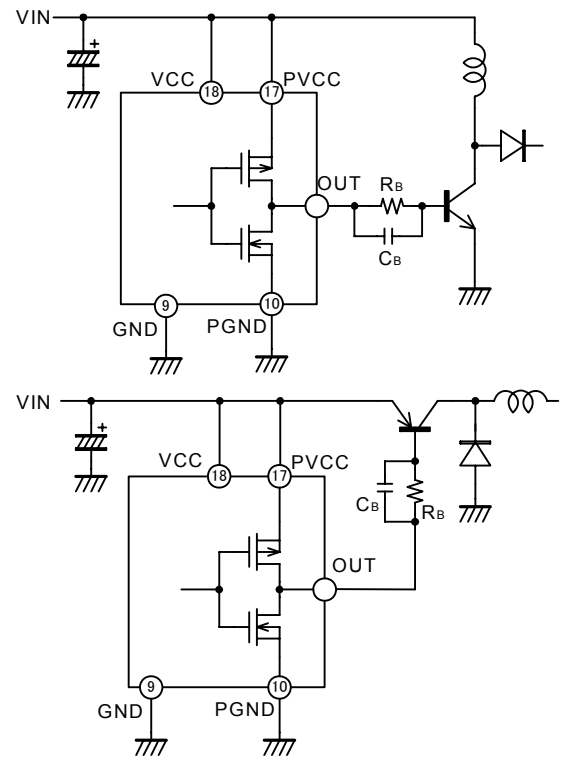


Fig.13

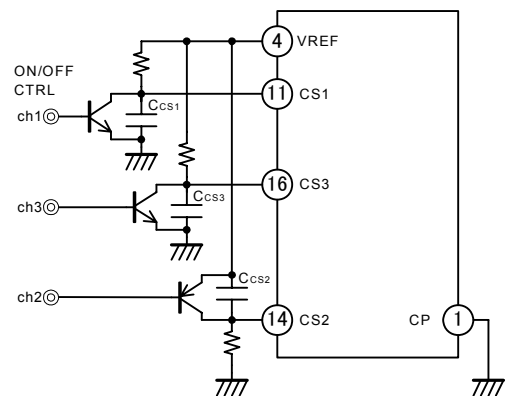


Fig.14

Timer latched Short Protection : not available

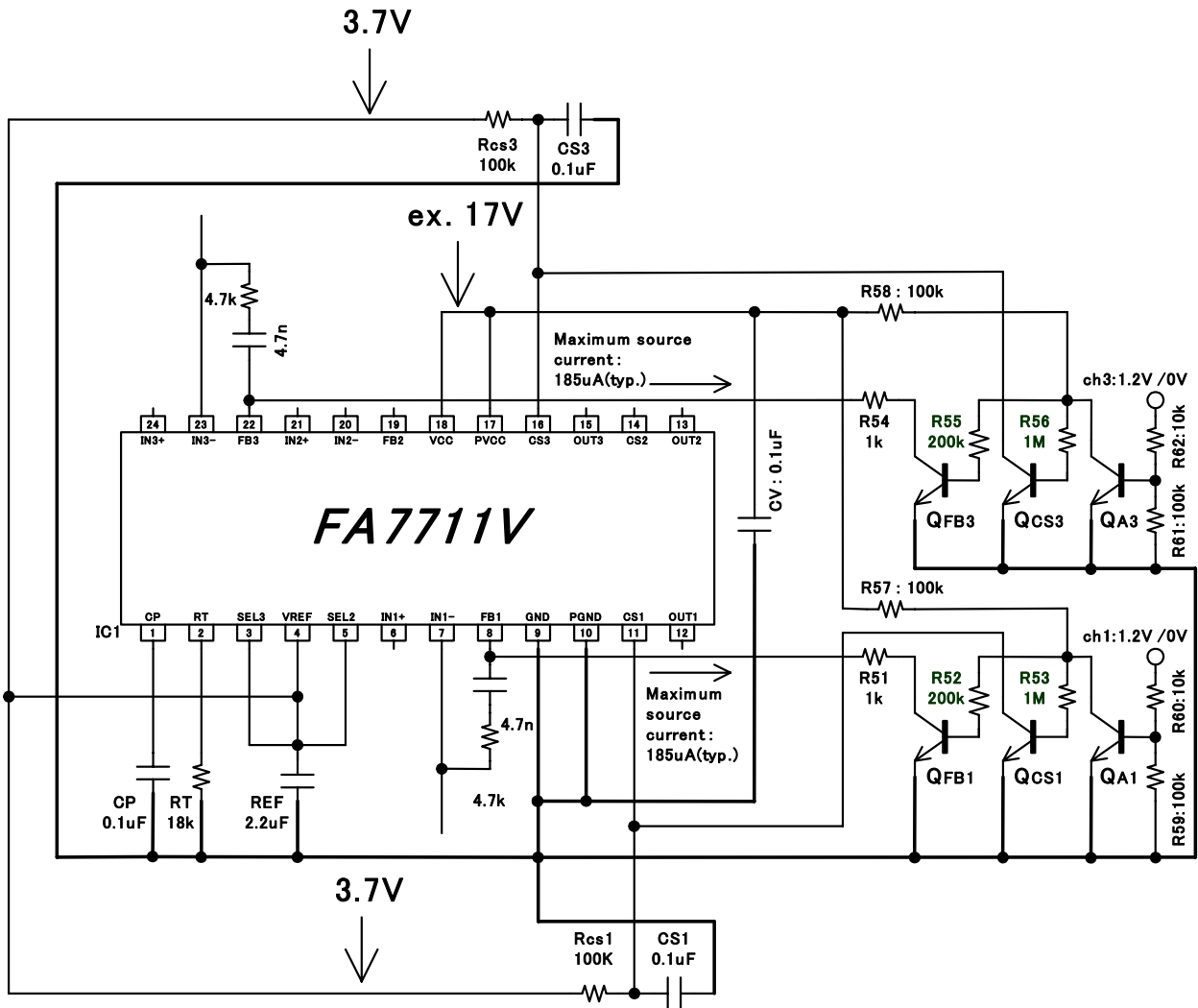


Fig.15 ON/OFF Circuit

Note : Channel 2 to control OUT2 pin is not suitable for ON/OFF control.

QA1, QA3:

Assuming base voltage as 0.9 V (max.),
 R59, R60, R61 and R62 should be designed so that the base current are larger than each collector current / 20.
 Here, 20 means fully small hFE in order to obtain low saturation voltage of QA*.

R51, R54 :

The voltage drop should be lower than 0.5 V at FB1 pin or FB3 pin to obtain 0% duty for ON mode of QFB*.
 ex. $R51 * I_{SOFB} = 1k \text{ ohm} * 185 \text{ uA}$
 $= 0.185 \text{ V}$
 $< 0.5 \text{ V}$

(10) Setting of the output voltage of DC-DC converter

Figure 16,17,18 shows the ways to set each channel of the output voltage of DC-DC converter.

• Applications for each channels

Ch1	Buck, Inverting
Ch2	Buck, Boost, Inverting, Fly-back
Ch3	Buck, Boost, Inverting, Fly-back

In the case of a boost, a buck, or a fly-back circuit, the output voltage can be calculated with:

For Ch1 (Fig.16, Fig.17)

$$V_{out1} = \frac{R10 + R11}{R11} \times V1$$

For Ch2 (Fig.17, Fig.18)

$$V_{out2} = \frac{R20 + R21}{R21} \times V2$$

For Ch3 (Fig.16, Fig.18)

$$V_{out3} = \frac{R30 + R31}{R31} \times V3$$

An inverting circuit, the output voltage can be calculated with:

For Ch1 (Fig.18)

$$V_{out1} = \frac{R10 + R11}{R10} \times V1 - \frac{R11}{R10} \times V_{REF}$$

For Ch2 (Fig.16)

$$V_{out2} = \frac{R20 + R21}{R20} \times V2 - \frac{R21}{R20} \times V_{REF}$$

For Ch3 (Fig.17)

$$V_{out3} = \frac{R30 + R31}{R30} \times V3 - \frac{R31}{R30} \times V_{REF}$$

The ratio of resistance can be calculated with:

$$\frac{R10}{R11} = \frac{V_{REF} - V1}{V_{out1} + V1}$$

(Use the absolute value of Vout voltage)

(The same Vout2 and Vout3 as Vout1)

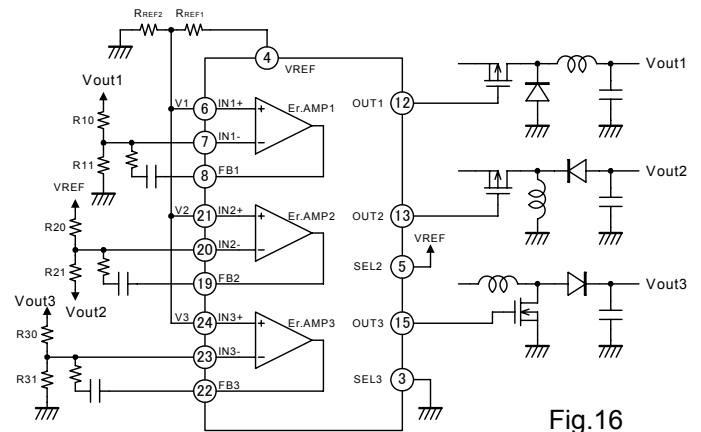


Fig.16

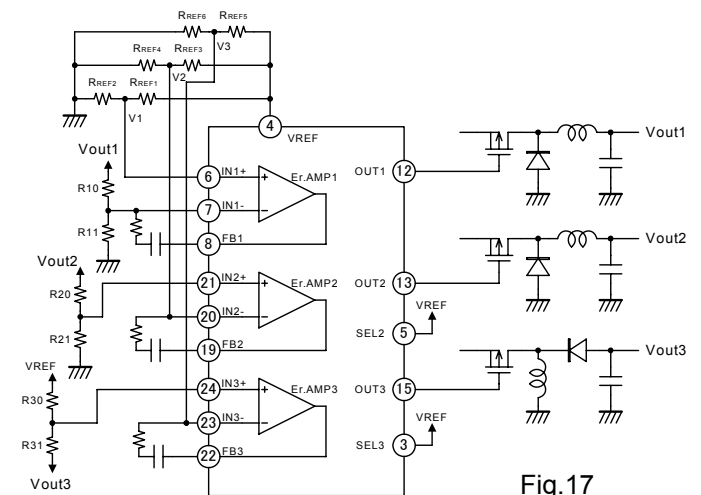


Fig.17

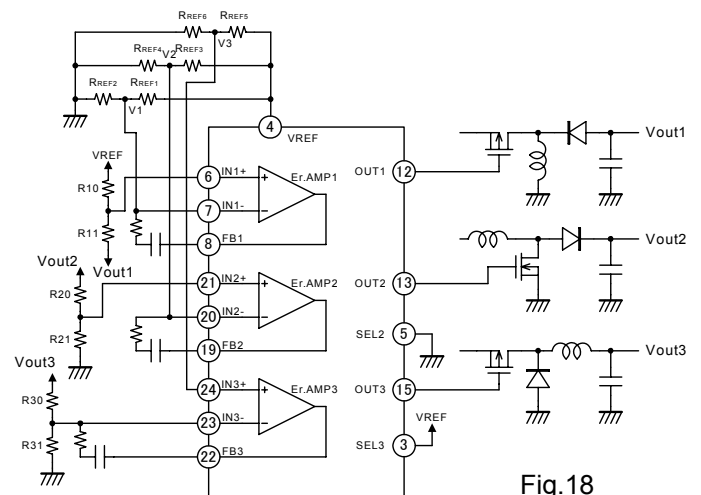


Fig.18

(11) Protection from negative voltage apply

If rather large negative voltage is applied to any pins of this IC, internal parasitic elements start operating, and they may cause malfunctions. Accordingly, the negative voltage, which is applied to each Pin of the ICs, must be kept above -0.3V.

In the case of the OUT* pin, in particular, the oscillation of voltage occurring after MOSFET's turning off can be applied to the OUT* pin through MOSFET's parasitic capacitance. As a result, there is a possibility that the negative voltage is applied to the OUT* pin. If this negative voltage reaches -0.3V or below, connect an Schottky barrier diode between OUT* pin and GND as shown in Fig. 21. The Schottky barrier diode's forward direction voltage clamps the voltage applied to the OUT* pin. In this case, use the Schottky barrier diode with low voltage drop in forward direction. Other pins should be kept above -0.3 V also based on the same reasons.

In the case of an inverting circuit, the negative voltage charged on the output capacitor will be applied to VREF pin just after turning off the input voltage.

If input voltage is turned on during applying a negative voltage to VREF pin, the negative voltage may lead malfunction.

This problem is likely to occur in the case of short interruption.

In such a case, re-start the converter after the output capacitor is discharged enough or connect a schottky barrier diode with low forward voltage between VREF pin and GND as shown in Fig.20.

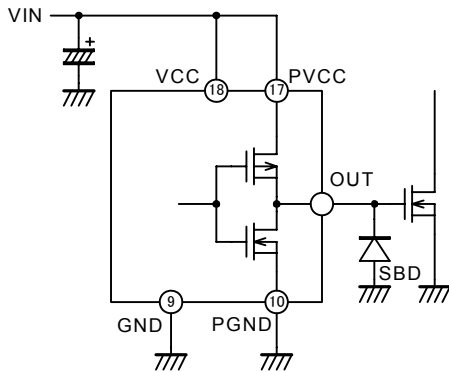


Fig.19

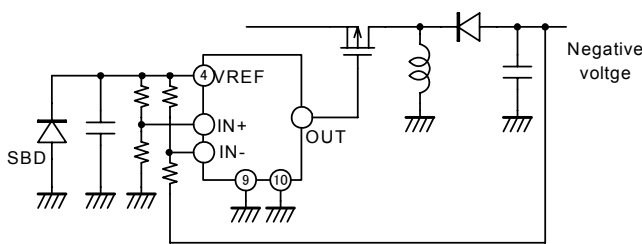


Fig.20

(12) An error pulse at start up

At start up, if rise time of VCC and PVCC pin is too short, an error pulse, which is several tens μ s width, may appear on the OUT pin.

The Internal circuit of IC is not stable before VREF pin voltage rises to about 1V. Therefore, It may cause an error pulses that a voltage is applied to PVCC pin before VREG pin voltage raises enough at start up.

The error pulse may appear when Vcc rise time from 0V to 12V is less than about a few hundred μ s.

In such a case, check the influence of the error pulse such as blowout of a fuse.

On the other hand, if rise time of Vcc is not so short, the error pulse will not appear.

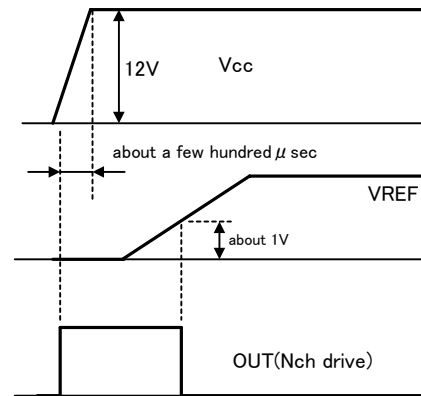


Fig.21

(13) Design of phase compensation

A switching power supply supervises output voltage with error amplifier, constitutes a closed loop, and is stabilizing voltage by negative feedback.

Phase delay with a smoothing filter and Gain with the main switching device, etc. is contained in the negative feedback circuit, and those sum totals become the phase and the gain in a closed loop.

The phase and the gain have the frequency characteristic. In a negative feedback circuit, if the gain remains 0dB or more at the frequency of 180 degrees delayed phase, a circuit will be oscillated.

In order to prevent oscillation, it is necessary to adjust the phase and the gain of error amplifier. (Fig.22) Since especially the switching power supply has repeated ON and OFF at high speed, the minute high frequency element is contained in the output, and if you setup the frequency characteristic of the error amplifier beyond necessity, it has a possibility of unstable operate and oscillate.

The gain when the phase turns 180 degrees calls gain margin, the phase when the gain becomes 0dB calls phase margin. Above 10dB of gain margin and above 50 degrees of phase margin are desirable generally and set to this condition in phase compensation. (Fig.22)

However, gain margin and phase margin against transient response (sudden change of load, etc.) are participate as trade-off, therefore when gain margin and phase margin is larger, transient response becomes margin-less condition, furthermore over shoot and under shoot of converter voltage is larger.

To determine the value of circuit components, it cannot decide here since conditions change a lot with the value of an output filter or others, but generally adjust the value between $1k\ \Omega$ and $100k\ \Omega$ of resistor R_{FB} and the value between $1nF$ and $100nF$ of capacitor C_{FB} . However the operation of switching power supply changes by load condition, duty cycle, temperature, etc., so when determine the value of components, examine with the real load condition in actual circuit.

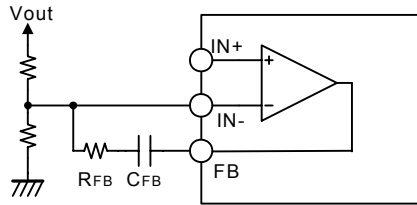


Fig.22

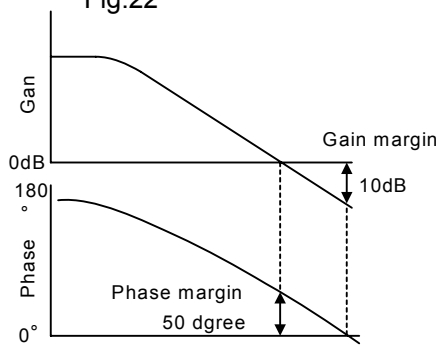
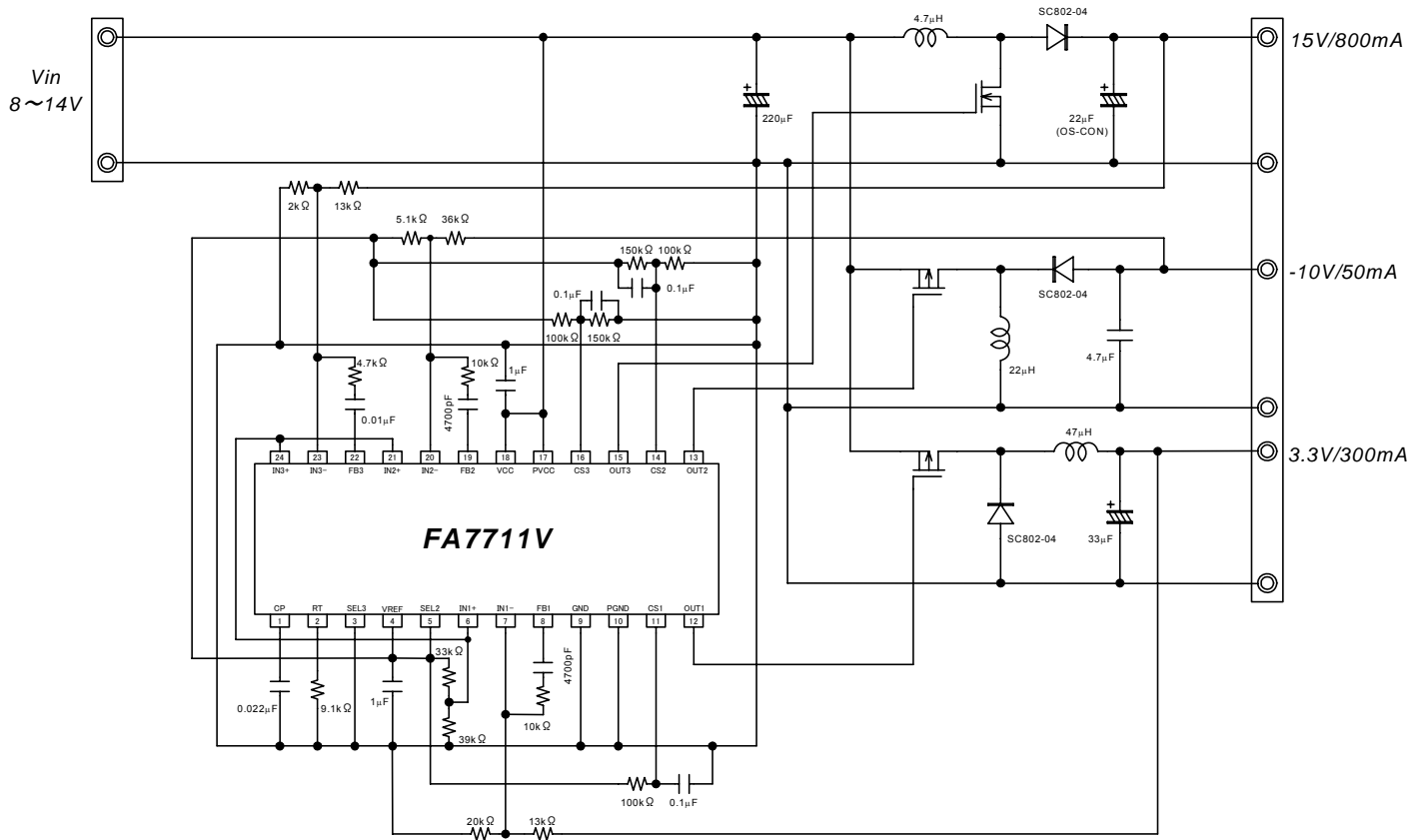


Fig.23

10. Application circuit



Obtained values are not guaranteed.
 When determining values and external discrete components, examine under the actual circuit condition.