HEWLETT PACKARD

IDC-51418
MagIC™ Silicon Bipolar MMIC
1.5 Gb/s Decision Circuit

Features

- **High Data Rates: 1.5 Gb/s NRZ**
- **Input Sensitivity < 20 mVpp Typical**
- **ECL Voltage Swing Compatible C-Input and Q-Outputs**
- **Single Ended or Differential C and D Inputs**
- **Single Power Supply: +5 V or -5.2 V**
- **Low Power: 450 mW Typical Dissipation**
- **Hermetic Glass-metal Surface Mount Package**

Description

The IDC-51418 is a high speed silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) decision circuit, housed in a miniature glass-metal hermetic, surface mount package. It is designed for data communications and LAN applications. Other uses include wide bandwidth communications and digital circuits, such as comparators and D type flip-flops. The IDC-51418 is a master-slave D type flip-flop with a high gain data preamplifier for increased sensitivity. Both the data and clock inputs can be driven differentially or single ended. The bias and input matching circuits are included on-chip.

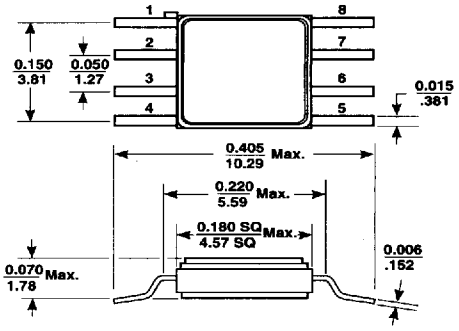
The IDC series of high speed decision circuits is fabricated using HP's 10 GHz, f_T, 25 GHz f_{MAX} ISOSAT™-1 silicon bipolar process that uses nitride self-alignment, submicrometer lithography, trench isolation, ion implantation, gold metallization, and polyimide inter-metal dielectric and scratch protection to achieve excellent performance uniformity, and reliability.

Truth Table

Input		Output	
Cn	Dn	Qn +1	$\overline{Qn+1}$
⌐	x	Qn	$\overline{Qn}$
⌐	0	0	1
⌐	1	1	0

Cn: Clock State at t = n
Dn: Data State at t = n
Qn: Output state at t = n
Qn +1: Output state at t = n +1

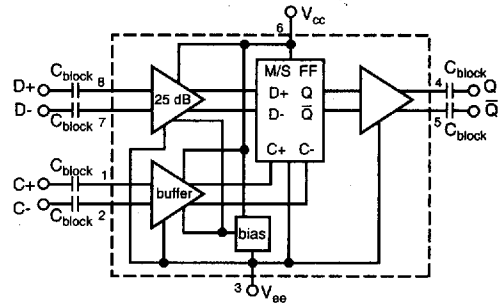
180 mil Package



PIN DESCRIPTION	
1 C+	8 D+
2 C-	7 D-
3 V_{ee}	6 V_{cc}
4 Q	5 $\overline{Q}$
Bottom of Package is V_{ee}	

Notes:
(unless otherwise specified)
1. Dimensions are in / mm
2. Tolerances in .xxx = ±.005 mm .xx = ±.13

Functional Block Diagram



Package bottom is also V_{ee}

Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions: V_{cc} = 5 V, V_{ee} = 0 V, R_L = 50 Ω		Units	Min.	Typ.	Max.
t_r	Q Output Rise Time, 10% to 90%	1.5 Gb/s	ps		200	
t_f	Q Output Fall Time, 90% to 10%	1.5 Gb/s	ps		190	
V_{in} (D+,D-)	Minimum Data Input Amplitude (single ended), BER = 10^{-9}	1.5 Gb/s	mVpp		20	40
CPM	Clock Phase Margin	1.5 Gb/s	deg		335	
F_b max	Maximum Data Rate (NRZ Operation)	V_{in} = 40 mV_{pp}	Gb/s	1.2	1.5	
V_{ck}(C+,C-)	Clock Input Amplitude (single ended)		mVpp		600	
V_o(Q, $\overline{Q}$)	Output Voltage		mVpp	650	800	
t_{pd}	Propagation Delay Time, Falling Clock Edge to Q Output		ps		500	
t_{setup}	Setup Time (see Timing Diagram)		ps		-25	
t_{hold}	Hold Time (see Timing Diagram)		ps		60	
VSWR	Clock and Data Input VSWR	f = .01-1.5 GHz			1.3:1	
VSWR	Q, $\overline{Q}$ Output VSWR	f = .01-1.5 GHz			2.0:1	
I_d	Quiescent Device Current		mA	75	95	115

The recommended Power Supply Voltage range ($V_{cc} - V_{ee}$) for this device is 4.5 to 5.5 V.

Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Voltage	8 V
Power Dissipation[2, 3]	800 mW
C or D Input	2 Vpp
Junction Temperature	200°C
Storage Temperature	-65 to 200°C

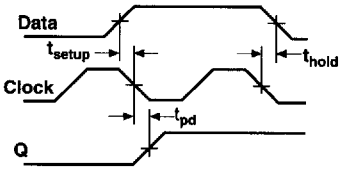
Thermal Resistance[2]: θ_{jc} = 55°C/W

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. Derate at 18 mW/°C for T_{case} > 156°C

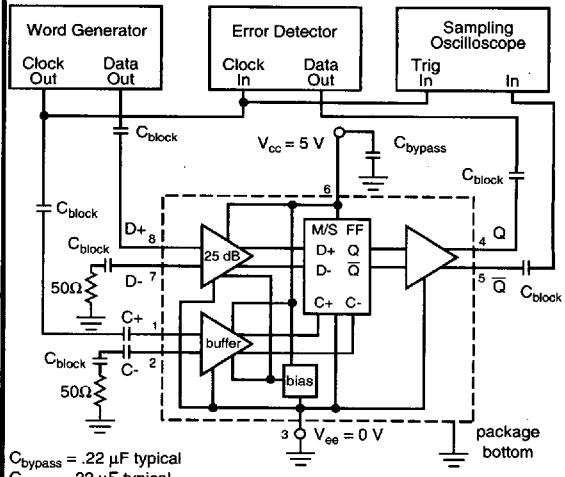
Typical Performance, T_A = 25°C, V_{cc} = 5 V, V_{ee} = 0 V, R_L = 50 Ω

(unless otherwise noted)

Timing Diagram



Test Configuration
Single Ended Input/Single Ended Output

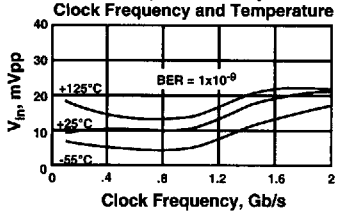


Notes: For transparent (non-latched comparator) operation, AC couple pins 1, 2 (C+, C-) to ground.

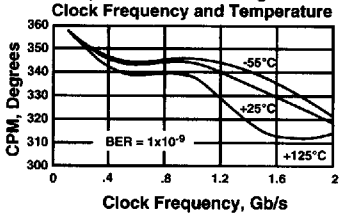
Good RF ground of Pin 3 and package bottom is critical for proper operation and good VSWR performance of this part.

FIBER OPTICS

Data Input Sensitivity vs. Clock Frequency and Temperature



Input Clock Phase Margin vs. Clock Frequency and Temperature



Quiescent Input/Output Voltages
(Inputs terminated, offset voltages = 0 V)

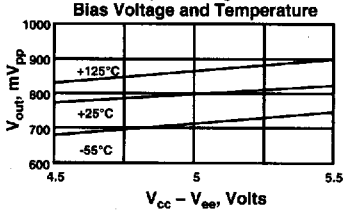
$V_{cc} - V_{ee}$	D	C	Q
5.0 V	5.0 V	3.8 V	3.4 V
-5.2 V	0.0 V	-1.2 V	-1.6 V

Note: Small offset voltages between D+ and D- will cause Q (Q) to go to a high (Vcc -.2 V) or low (Vcc -1.2 V) state.

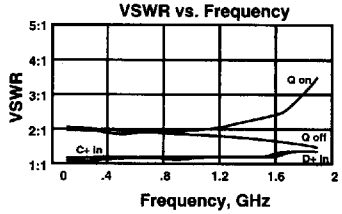
Output Voltages in the Latched (on/off) State

$V_{cc} - V_{ee}$	Q (V_{OH})	$\overline{Q}$ (V_{OL})
5.0 V	4.8 V	3.8 V
-5.2 V	-.2 V	-1.2 V

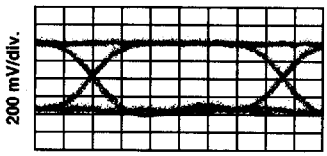
Output Voltage vs. Bias Voltage and Temperature



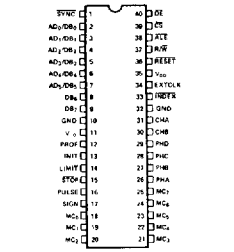
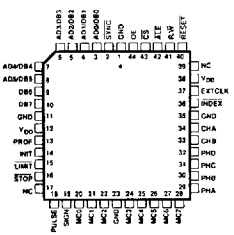
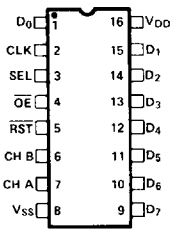
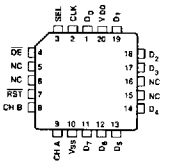
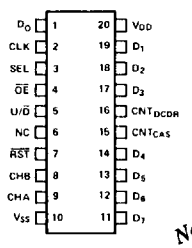
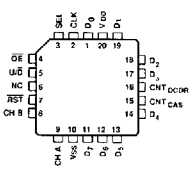
VSWR vs. Frequency



Output Eye Diagram at 1.5 Gb/s (Pseudorandom pattern = 2^{23} -1)



Motion Control ICS – HCTL-XXXX Series

Package Outline Drawing	Part No.	Package	Description	Page No.
	HCTL-1100	PDIP	CMOS General Purpose Motion Control IC	1-104
	HCTL-1100 OPT PLC	PLCC	CMOS General Purpose Motion Control IC	
	HCTL-2000	PDIP	CMOS Quadrature Decoder/Counter IC, 12-bit Counter	1-86
	HCTL-2016	PDIP	CMOS Quadrature Decoder/Counter IC, 16-bit Counter	
	*New* HCTL-2016 OPT PLC	PLCC	CMOS Quadrature Decoder/Counter IC, 16-bit Counter	1-102
	HCTL-2020	PDIP	CMOS Quadrature Decoder/Counter IC, 16-bit Counter, Quadrature Decoder Output Signals, Cascade Output Signals	1-86
	*New* HCTL-2020 OPT PLC	PLCC	CMOS Quadrature Decoder/Counter IC, 16-bit Counter, Quadrature Decoder Output Signals, Cascade Output Signals	1-102

Accessories for Encoders and Encoder Modules

Package Outline Drawing	Part No.	Description	Page No.
	HEDS-8902	4-wire connector with 15.5 cm (6.1 in.) flying leads. Locks into HEDS-5500 and HEDS-5600 2 channel encoders. Also fits HEDS-9000, HEDS-9100, and HEDS-9200 2 channel encoder modules.	1-61 1-22 1-28
	HEDS-8903	5-wire connector with 15.5 cm (6.1 in.) flying leads. Locks into HEDS-5540 and HEDS-5640 three channel encoders. Also fits HEDS-9040 and HEDS-9140 three channel encoder modules.	1-61 1-32
	HEDS-8905	Alignment Tool for HEDS-9140	1-32
	HEDS-8906	Alignment Tool for HEDS-9040	1-32
	HEDS-8901	Gap Setting shown for film codewheels	1-51
	HEDS-8932	Gap Setting shown for glass codewheels	1-51
	HEDS-8910 OPT 0 □□	Alignment Tool for HEDS-5540/5545 and HEDS-5640/5645. Order in appropriate shaft size.	1-61