DATA SHEET

TDA9803
Multistandard VIF-PLL demodulator

Preliminary specification
File under Integrated Circuits, IC02

November 1992

Philips Semiconductors

PHILIPS

Multistandard VIF-PLL demodulator TDA9803

FEATURES

- Suitable for negative and positive vision modulation
- Gain controlled 3-stage IF amplifier; suitable for VIF frequencies up to 60 MHz
- True synchronous demodulation with active carrier regeneration (ultra-linear demodulation, good intermodulation figures reduced harmonics and excellent pulse response)
- Peak sync AGC for negative modulation, e.g. B/G standard
- Peak white AGC for positive modulation, e.g. L standard
- Video amplifier to match sound trap and sound filter
- AGC output voltage for tuner; adjustable take-over point (TOP)
- AFC detector without extra reference circuit
- Stabilizer circuit for ripple rejection and to achieve constant output signals
- 5 to 8 V positive supply voltage range, low power consumption (230 mW at +5 V supply)

GENERAL DESCRIPTION

The TDA9803 is a monolithic integrated circuit for vision IF signal processing in multistandard TV and VTR sets.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage (pin 20)	4.5	5	8.8	V
I_P	supply current	39	46	53	mA
$V_{i\ IF}$	vision IF input signal sensitivity (RMS value, pins 1 and 2)	–	50	90	μV
	maximum vision IF input signal (RMS value, pins 1 and 2)	70	150	–	mV
G_v	IF gain control range	64	70	73	dB
$V_{o\ CVBS}$	CVBS output signal on pin 7 (peak-to-peak value)	1.7	2.0	2.3	V
B	–3 dB video bandwidth on pin 7	6	8	–	MHz
S/N (W)	signal-to-noise ratio weighted; for video	56	59	–	dB
$\alpha_{1.1}$	intermodulation attenuation	56	62	–	dB
$\alpha_{3.3}$		56	62	–	dB
α_H	suppression of harmonics in video signal	35	40	–	dB
T_{amb}	operating ambient temperature range	0	–	+70	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA9803	20	DIL	plastic	SOT146(1)
TDA9803T	20	mini-pack	plastic	SOT163A(2)

Note

1. SOT146-1; 1996 December 9.
2. SOT163-1; 1996 December 9.

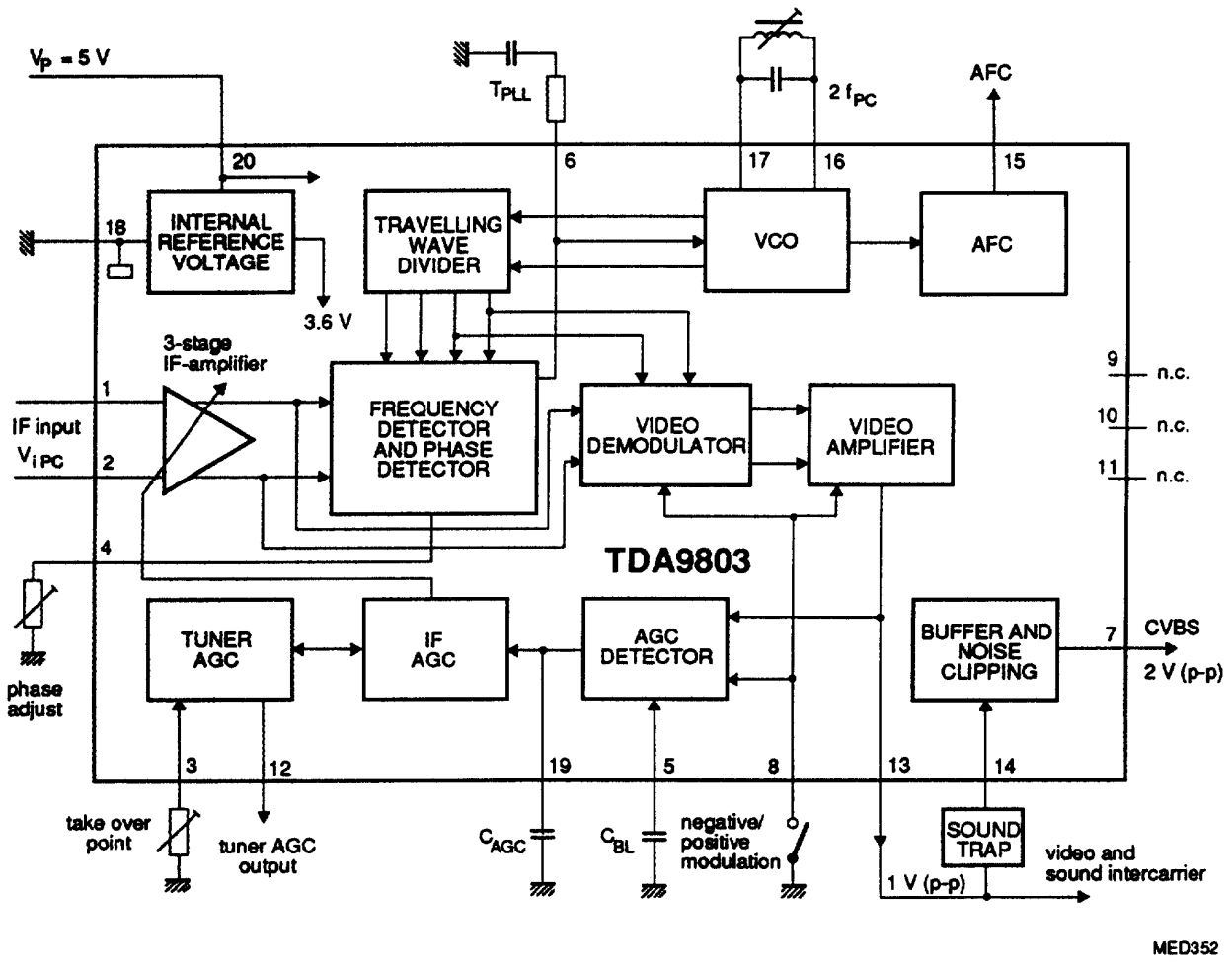


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
$V_{i\ IF}$	1	vision IF differential input signal
	2	
TADJ	3	tuner AGC take-over adjust (TOP)
ΦADJ	4	phase detector adjust
C_{BL}	5	black level capacitor, mute switch input
T_{PLL}	6	PLL time constant of phase detector
$V_{o\ CVBS}$	7	CVBS (positive) output signal
STD	8	standard switch (negative = HIGH, positive = LOW)
n.c.	9	not connected
	10	
	11	
TAGC	12	tuner AGC output
$V_{o\ VID}$	13	video and sound intercarrier output signal
$V_{i\ VID}$	14	video input signal to buffer amplifier
AFC	15	automatic frequency control output
VCO1	16	VCO reference circuit for 2 f_{PC}
VCO2	17	
GND	18	ground (0 V)
C_{AGC}	19	AGC capacitor
V_P	20	positive supply voltage

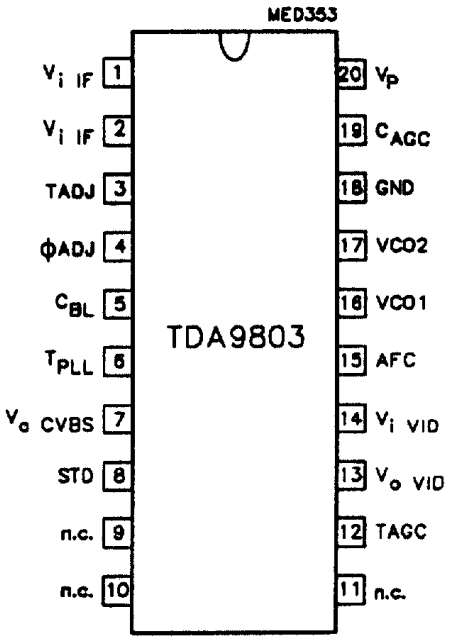


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Vision IF input

The vision IF amplifier consists of three AC-coupled differential amplifier stages; each stage comprises a controlled feedback network by means of emitter degeneration.

IF and tuner AGC

The automatic control voltage to maintain the video output signal at a constant level is generated according to the transmission standard. For negative modulation the peak-sync level is detected, for positive modulation the peak white level is detected. The AGC detector charges and discharges the capacitor on pin 19 to set the IF gain and the tuner gain. The standard is switched by the voltage on pin 8. To reduce the response time for positive modulation (which needs a very long time constant) a black level detector (C_{BL}) increases the AGC capacitor discharge current for low-level video signals.
The AGC capacitor voltage is transferred to an internal IF control signal, and is fed to the tuner AGC to generate the tuner AGC output current on pin 12 (open-collector output). The tuner AGC voltage take over point is adjusted on pin 3. This allows the tuner and the IF SAW filter to be matched to achieve the optimum IF input level.

Frequency detector, phase detector and video demodulator

The IF amplifier output signal is fed to a frequency detector and to a phase detector. The frequency detector is operational before lock-in. A DC current is generated which is proportional to the frequency difference between the input frequency and the VCO frequency. After lock-in, the frequency detector and the phase detector generate a DC current proportional to the phase difference between VCO and input signals. The control signal for the VCO is provided by the phase detector. The video demodulator is a linear multiplier, designed for low distortion and wide bandwidth. The vision IF input signal is multiplied by the in-phase component of the VCO output. The demodulated output signal is fed via an integrated low-pass filter (f_g = 12 MHz) to the video amplifier for suppression of the carrier harmonics. The polarity of the video signal is switched in the demodulator stage according to the TV standard.

VCO and travelling wave divider

The VCO operates with a symmetrically-connected reference LC-circuit, operating at double vision carrier frequency. Frequency control is performed by an internal varicap diode. The voltage to set the VCO frequency to the actual frequency of double vision carrier frequency, is also amplified and converted for the AFC output current.
The VCO signal is divided-by-two in a travelling wave divider, which generates two differential output signals with 90 degree phase difference independent of frequency.

Video amplifier, buffer and noise clipping

The video amplifier is a wide bandwidth operational amplifier with internal feedback. Dependent on transmission standard, a level shifter provides the same sync level for positive as for negative modulation. A nominal positive modulated video signal of 1 V (p-p) is present on the composite video output (pin 13).

The input impedance of the 7 dB wideband buffer amplifier (with internal feedback) is suitable for ceramic sound trap filters.
The CVBS output (pin 7) provides a positive video signal of 2 V (p-p). Noise clipping is provided internally.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 20) for a maximum chip temperature (note 1)			
	SOT146 at +120 °C	0	8.8	V
	SOT163A at +100 °C	0	5.5	V
V_I	voltage on pins 1, 2, 7, 8, 13, 14, 15 and 19	0	V_P	V
$t_{s\ max}$	short–circuit time	–	10	s
V_{12}	tuner AGC output voltage	–	13.2	V
T_{stg}	storage temperature range	–25	+150	°C
V_{ESD}	electrostatic handling for all pins (note 2)	–	±300	V

Notes

1. Supply current I_P = 53 mA at T_{amb} = +70 °C.
2. Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor (negative and positive voltage).

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	
	SOT146	73 K/W
	SOT163A	85 K/W

CHARACTERISTICS

V_P = 5 V; T_{amb} = +25 °C; f_{PC} = 38.9 MHz; f_{SC} = 33.4 MHz with V_{PC}/V_{SC} = 13 dB (B/G); V_{iIF} = 10 mV RMS value (sync level at B/G; peak-white level at L); video modulation DSB; residual carrier: B/G = 10%, L = 3%; video signal in accordance with CCIR line 17; measurements taken in Fig.3 unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 20)	see note 1	4.5	5	8.8	V
I_P	supply current		39	46	53	mA
Standard switch (pin 8)						
V_{IH}	input voltage for negative modulation	see note 2	1.5	–	V_P	V
V_{IL}	input voltage for positive modulation		0	–	0.8	V
I_{IL}	LOW level input current	V_8 = 0 V	–	–300	–360	μA
Vision IF input (pins 1 and 2)		B/G standard				
V_i	input signal sensitivity (RMS value)	–1 dB video at output	–	50	90	μV
	maximum input signal (RMS value)	+1 dB video at output	70	150	–	mV
ΔV_i	IF amplitude difference between picture and sound carrier	within AGC range	–	0.7	1	dB
G_{IF}	IF gain control range	see Fig.4	64	70	73	dB
B	–3 dB IF bandwidth	upper cut-off frequency	70	100	–	MHz
R_i	input resistance		1.7	2.2	2.7	kΩ
C_i	input capacitance		1.2	1.7	2.5	pF
$V_{1, 2}$	DC input voltage		3.0	3.4	3.8	V
True synchronous video demodulator		see note 3				
f_{VCO}	maximum oscillator frequency for carrier regeneration	$f = 2f_{PC}$	125	130	–	MHz
Δf_{VCO}	oscillator drift (free running) as a function of temperature	see note 4; ΔT = 0 to +70 °C	–	–	±1300	10^{-6}
$V_{o\ ref}$	oscillator swing at pins 16 and 17 (RMS value)		tbn	120	tbn	mV
Δf_{PC}	vision carrier capture range (negative)		1.5	2	–	MHz
	vision carrier capture range (positive)		1.5	2	–	MHz
t_{acqu}	acquisition time	see note 5; BL = 60 kHz	–	–	30	ms
$V_{i\ IF}$	IF input signal sensitivity (RMS value, pins 1 and 2)					
	for PLL still locked	see note 6; maximum IF gain	–	70	100	μV
	for C/N = 10 dB	see note 7	–	100	140	μV
I_{loop}	FPLL loop offset current at pin 6	see note 8	–	–	±4.5	μA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Composite video amplifier (pin 13)		sound carrier off				
$V_{0\ vid}$	output signal (peak-to-peak value)	see Fig.7	0.9	1.0	1.1	V
V_{13}	sync level	B/G and L	1.4	1.5	1.6	V
	zero carrier level	B/G	2.5	2.6	2.7	V
		L	1.37	1.47	1.57	V
	upper video clipping level		$V_P - 1.1$	$V_P - 1.0$	–	V
	lower video clipping level		–	0.3	0.4	V
$V_{0\ FM}$	IF intercarrier level (RMS value)	sound carrier on; see note 9	tbn	140	tbn	mV
R_{13}	output resistance		–	–	10	Ω
I_{int13}	internal bias current for emitter follower	DC	1.8	2.5	–	mA
I_{13}	maximum output sink current	DC and AC	1.4	tbn	–	mA
	maximum output source current		2.0	tbn	–	mA
B	–3 dB video bandwidth	$C_{13} < 50$ pF; $R_L > 1$ kΩ	7	10	–	MHz
α_H	suppression of video signal harmonics	see note 10; $C_{13} < 50$ pF; $R_L > 1$ kΩ	35	40	–	dB
RR	ripple rejection on pin 13	see Fig.9	32	35	–	dB
CVBS buffer amplifier and noise clipper (pins 7 and 14)						
R_{14}	input resistance		2.6	3.3	4.0	kΩ
C_{14}	input capacitance		1.4	2	3.0	pF
V_{14}	DC voltage at input		1.5	1.8	2.1	V
G_v	voltage gain	see note 11	6	7	7.5	dB
$V_{o\ CVBS}$	CVBS output signal on pin 7 (peak-to-peak value)	sound carrier off; see Fig.3	1.7	2.0	2.3	V
	CVBS output level	upper video clipping	tbn	4.0	–	V
		lower video clipping	–	1.0	tbn	V
		sync level	1.25	1.35	1.45	V
R_7	output resistance		–	–	10	Ω
I_{int7}	internal bias current for emitter follower	DC	1.8	2.5	–	mA
I_7	maximum output sink current	DC and AC	1.4	tbn	–	mA
	maximum output source current		2.4	tbn	–	mA
B	–3 dB video bandwidth	$C_7 < 20$ pF; $R_L > 1$ kΩ	8	11	–	MHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Measurements from IF input to CVBS output (pin 7) 330 Ω between pins 13 and 14, sound carrier off						
$V_{o\ CVBS}$	CVBS output signal on pin 7 (peak–to–peak value)		1.7	2.0	2.3	V
ΔV_o	deviation of CVBS output signal at B/G	50 dB gain control	–	–	0.5	dB
		30 dB gain control	–	–	0.1	dB
	black level tilt	B/G standard; see note 12	–	–	1	%
	vertical tilt for worst case in L standard	vision carrier modulated by test line (VITS) only; see note 12	–	–	1.5	%
ΔG	differential gain		–	2	5	%
$\Delta\varphi$	differential phase		–	1	3	deg
B	–3 dB video bandwidth	C_L < 20 pF; R_L > 1 kΩ	6	8	–	MHz
S/N(W)	signal-to-noise ratio; weighted	see Fig.5 and note 13	56	59	–	dB
$\alpha_{1.1}$	intermodulation at 'blue'	see Fig.6 and note 14; f = 1.1 MHz	56	62	–	dB
	intermodulation at 'yellow'		58	64	–	dB
$\alpha_{3.3}$	intermodulation at 'blue'	f = 3.3 MHz	56	62	–	dB
	intermodulation at 'yellow'		57	63	–	dB
α_C	residual vision carrier (RMS value)	fundamental wave	–	1	10	mV
		harmonics	–	1	10	mV
α_H	suppression of video signal harmonics	see note 10	35	40	–	dB
RR	ripple rejection on pin 7	see Fig.9	25	28	–	dB
AGC detector (pin 19)						
t_{resp}	response to an increasing amplitude step of 50 dB in input signal	B/G and L	–	1	10	ms
	response to a decreasing amplitude step of 50 dB in input signal	B/G	–	50	100	ms
		L	–	100	150	ms
I_{19}	charging current	B/G and L; see note 12	0.85	1.1	1.35	mA
	additional charging current	L in case of missing VITS pulses and no white video content	2.2	2.7	3.2	μA
	discharging current	B/G	17	22	27	μA
		normal mode L	0.24	0.33	0.42	μA
		fast mode L	31	44	57	μA
V_{19}	AGC voltage	see Fig.4				
		maximum gain	0	tbn	–	V
		minimum gain	–	tbn	V_P – 0.7	V
V_{13}	threshold voltage level	see Fig.7				
	for additional charging current	L	1.9	1.95	2.0	V
	for fast L mode	L	1.6	1.65	1.7	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Tuner AGC (pin 12)						
V_i	IF input signal for minimum starting point of tuner take over (RMS value)	input at pins 1 and 2; R_{TOP} = 22 kΩ	–	–	5	mV
	IF input signal for maximum starting point of tuner take over (RMS value)	input at pins 1 and 2; R_{TOP} = 0 Ω	50	–	–	mV
V_{12}	allowable voltage	from external source	–	–	13.2	V
	saturation voltage	I_{12} = 1.7 mA	–	–	0.2	V
ΔV_{12}	variation of take over point by temperature	ΔT = 0 to +50 °C	–	1	3	dB
I_{12}	sink current	see Fig.4				
		no tuner gain reduction	–	0.1	0.3	μA
		maximum tuner gain reduction	1.7	2.0	2.6	mA
ΔG_{IF}	IF slip by automatic gain control	tuner gain current from 20 to 80%	–	6	8	dB
AFC circuit (pin 15)		see Fig.8 and note 15				
S	control steepness $\Delta I_{15}/\Delta f$	see note 16	0.6	0.72	0.84	μA/kHz
Δf_{IF}	frequency variation by temperature	ΔT = 0 to +70 °C; see note 4	–	–	±1300	10^{-6}
V_{15}	output voltage upper limit	see Fig.8	V_P – 0.5	V_P – 0.3	–	V
	output voltage lower limit		–	0.3	0.5	V
I_{15}	output current source		160	200	240	μA
	output current sink		160	200	240	μA
ΔI_{15}	residual video modulation current (peak–to–peak value)	B/G and L	–	20	30	μA

Notes

1. Typical values of video and sound parameters are decreased at V_P = 4.5 V.
2. The input voltage for negative modulation has to be $V_8 > 1.5$ V, or pin 8 open-circuit.
3. Loop bandwidth BL = 60 kHz (natural frequency f_n = 15 kHz; damping factor d = 2 calculated with grey level and FPLL input signal level).
   Resonance circuit of VCO: $Q_o > 50$; C_{ext} = 8.2 pF; $C_{int} \approx 8.5$ pF (loop voltage about 2.7 V).
4. The oscillator drift is related to the picture carrier frequency (at external temperature-compensated LC-circuit).
5. $V_{i\,IF}$ = 10 mV (RMS value); Δf = 1 MHz (VCO frequency offset related to picture carrier frequency); white picture video modulation.
6. $V_{i\,IF}$ for 0.9 V CVBS (peak–to–peak value) at composite video output pin 13; PLL is still locked.
7. Transformer at IF input (Fig.3). The C/N ratio at IF input for ‘lock–in’ is defined as the vision IF input signal (sync level, RMS value) in relation to a superimposed, 5 MHz band–limited white noise signal (RMS value); video modulation: white picture.
8. Offset current measured between pin 6 and half of supply voltage (V = 2.5 V) under the following conditions: no input signal at IF input (pins 1 and 2) and IF–amplifier gain at minimum ($V_{19} = V_P$), pin 4 (phase adjust) open–circuit.

9. The intercarrier output signal is superimposed to the video signal at pin 13 and can be calculated by the following formula: $20 \log\left(\frac{V_{13\ interc.(p\text{-}p)}}{1\ V\ (p\text{-}p)}\right) = \frac{V_{iSC}}{V_{iPC}} + 6.9\ dB \pm 2\ dB$

   with: $\frac{V_{iSC}}{V_{iPC}}$ dB = sound to picture carrier ratio at IF input (pins 1 and 2) in dB

   and
   ±2 dB = tolerance of intercarrier output amplitude $V_{o\ FM}$.
10. Measurements taken with SAW filter G1956; modulation: VSB, $f_{video} > 0.5$ MHz, loop bandwidth BL = 60 kHz.
11. The 7 dB buffer gain accounts for 1 dB loss in the sound trap. Buffer output signal is typical 2 V (p-p). If no sound trap is applied a 330 Ω resistor must be connected from output to input (from pin 13 to pin 14).
12. The leakage current of the AGC capacitor has to be < 1 μA in B/G mode (< 30 nA in L mode) to avoid larger tilt.
13. S/N is the ratio of black-to-white amplitude to the black level noise voltage (RMS value, pin 7). B = 5 MHz weighted in accordance with CCIR-567 at a source impedance of 50 Ω.
14. $\alpha_{1.1}$ = 20 log (V_o at 4.4 MHz / V_o at 1.1 MHz) + 3.6 dB; $\alpha_{1.1}$ value at 1.1 MHz related to black/white signal
    $\alpha_{3.3}$ = 20 log (V_o at 4.4 MHz / V_o at 3.3 MHz); $\alpha_{3.3}$ value at 3.3 MHz related to colour carrier.
15. To match the AFC output signal to different tuning systems a current source output is provided (Fig.8).
16. Depending on the ratio $\Delta C/C_o$ of the LC resonance circuit of VCO
    ($Q_o > 50$; $C_o = C_{int} + C_{ext}$; C_{ext} = 8.2 pF; $C_{int} \approx 8.5$ pF).

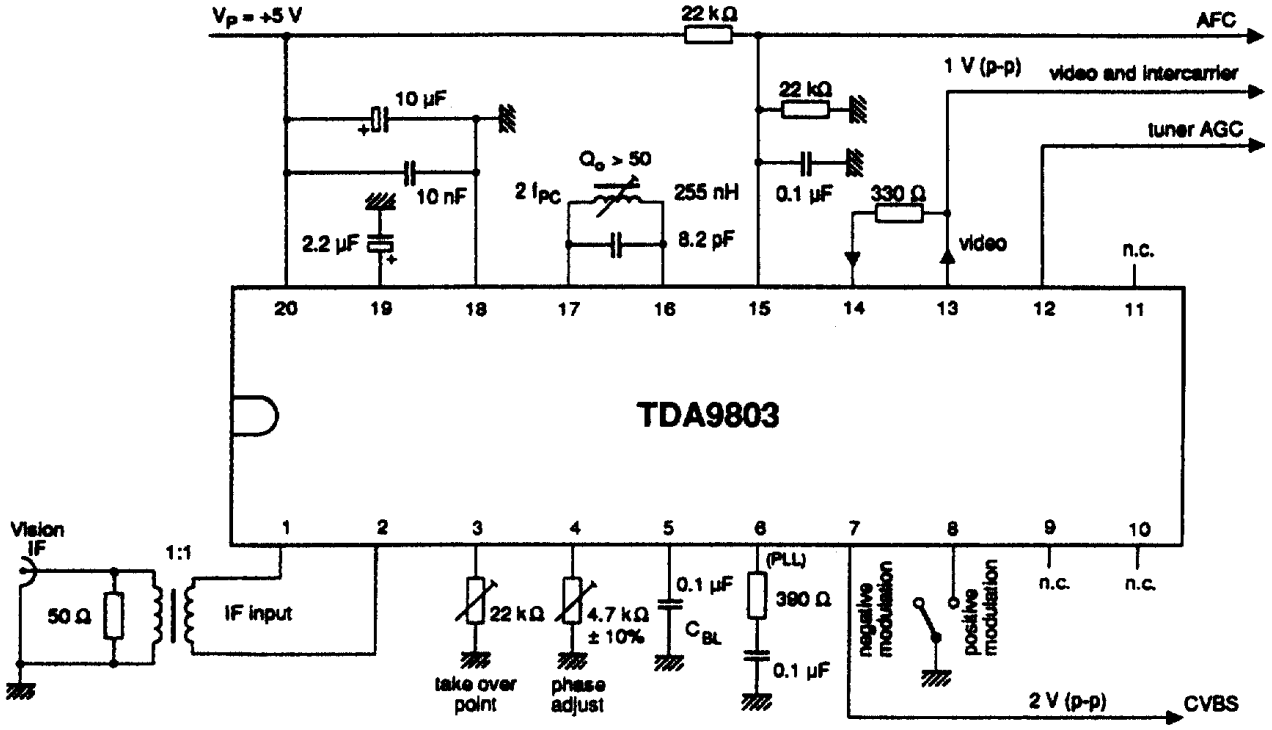


Fig.3 Test circuit.

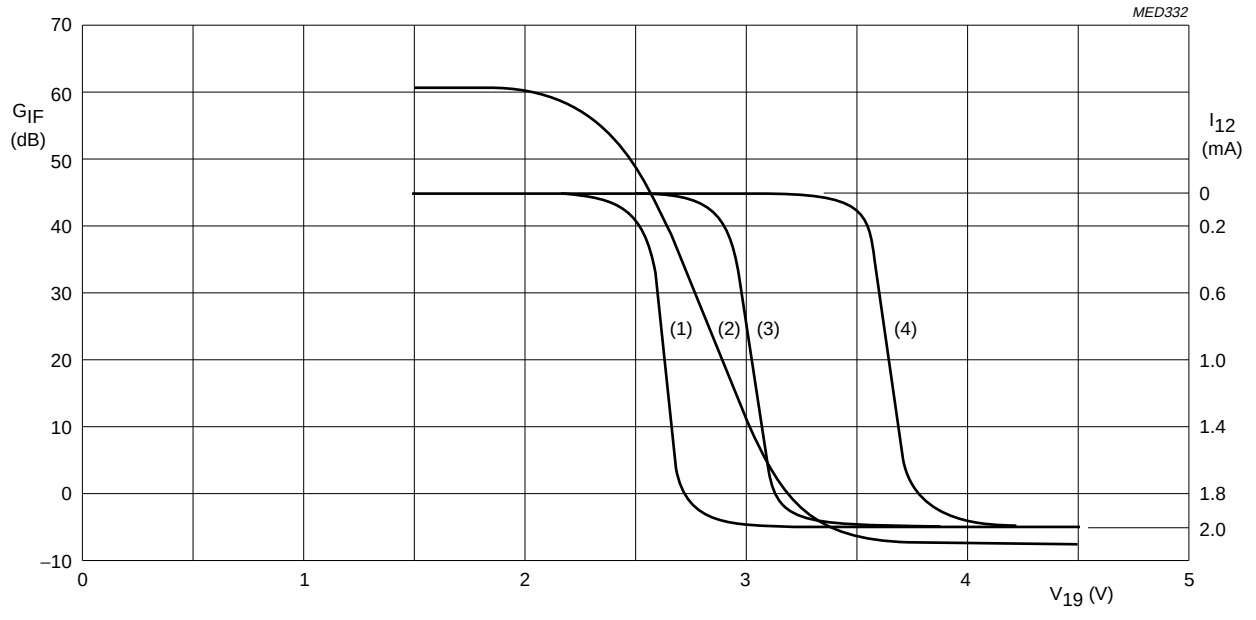


Fig.4 IF AGC (dashed) and tuner AGC as a function of take over point adjustment.

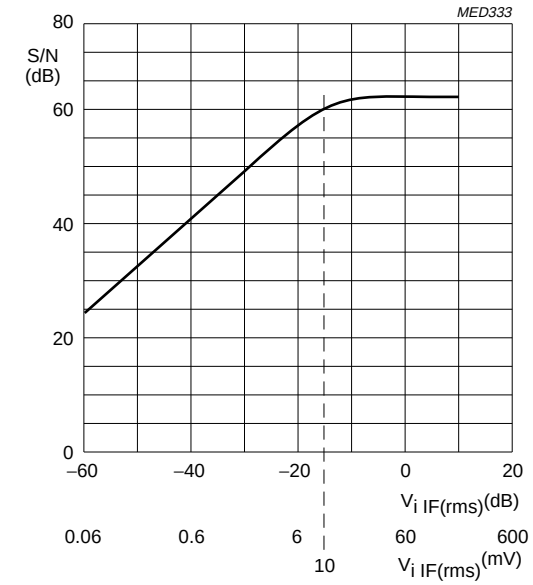
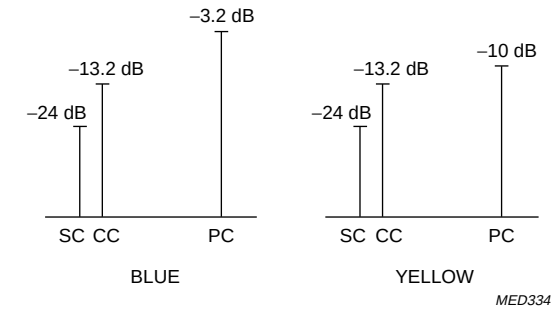


Fig.5 Typical signal-to-noise ratio as a function of the IF input signal.



SC = sound carrier level ; with respect to TOP sync level.
CC = chrominance carrier level ; with respect to TOP sync level.
PC = picture carrier level ; with respect to TOP sync level.

Sound shelf attenuation: 17 dB.

Fig.6 Input conditions for intermodulation measurements.

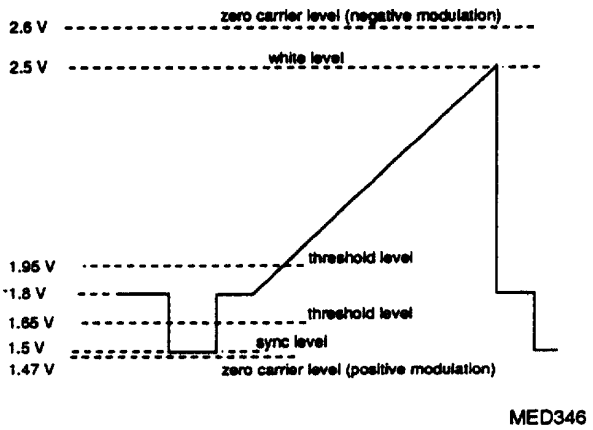


Fig.7 Video signal levels on output pin 13.

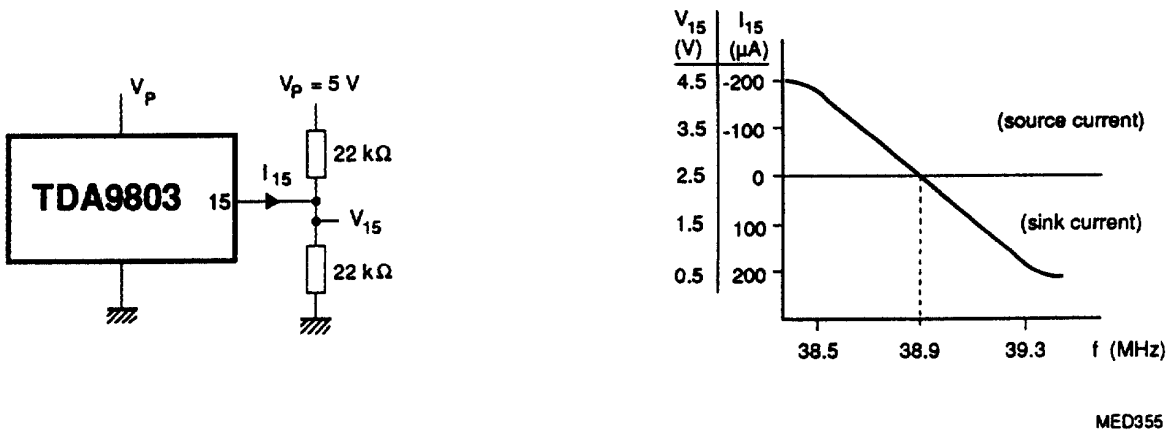


Fig.8 Measurement conditions and typical AFC characteristic.

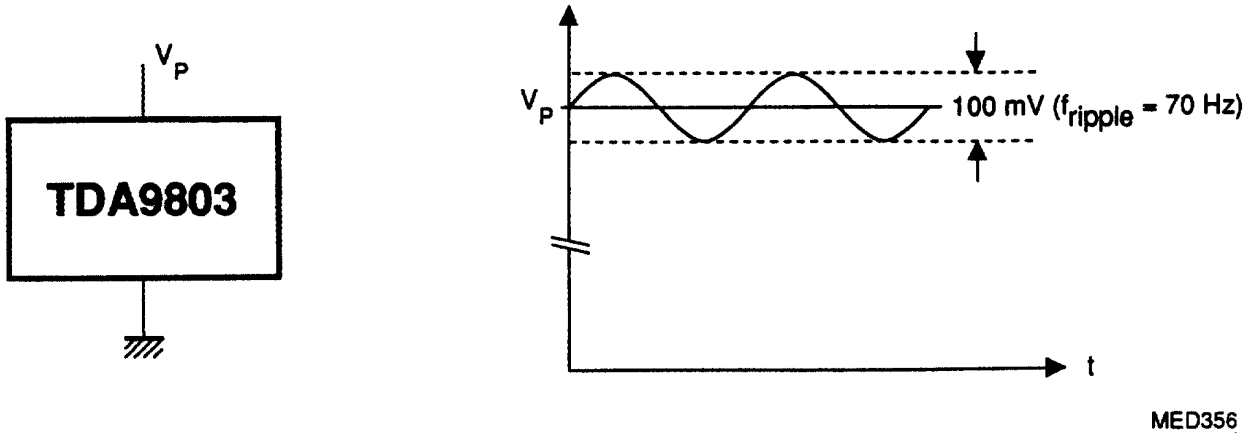


Fig.9 Ripple rejection condition.

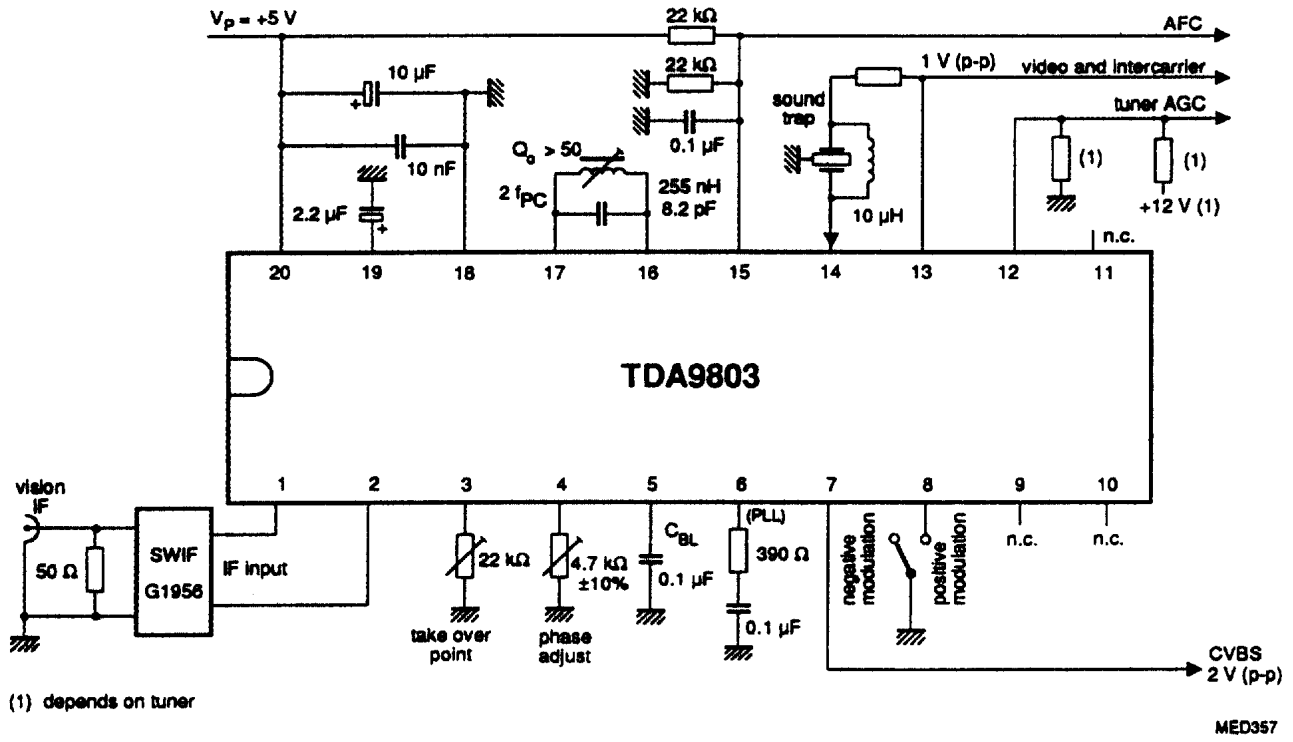


Fig.10 Application circuit.

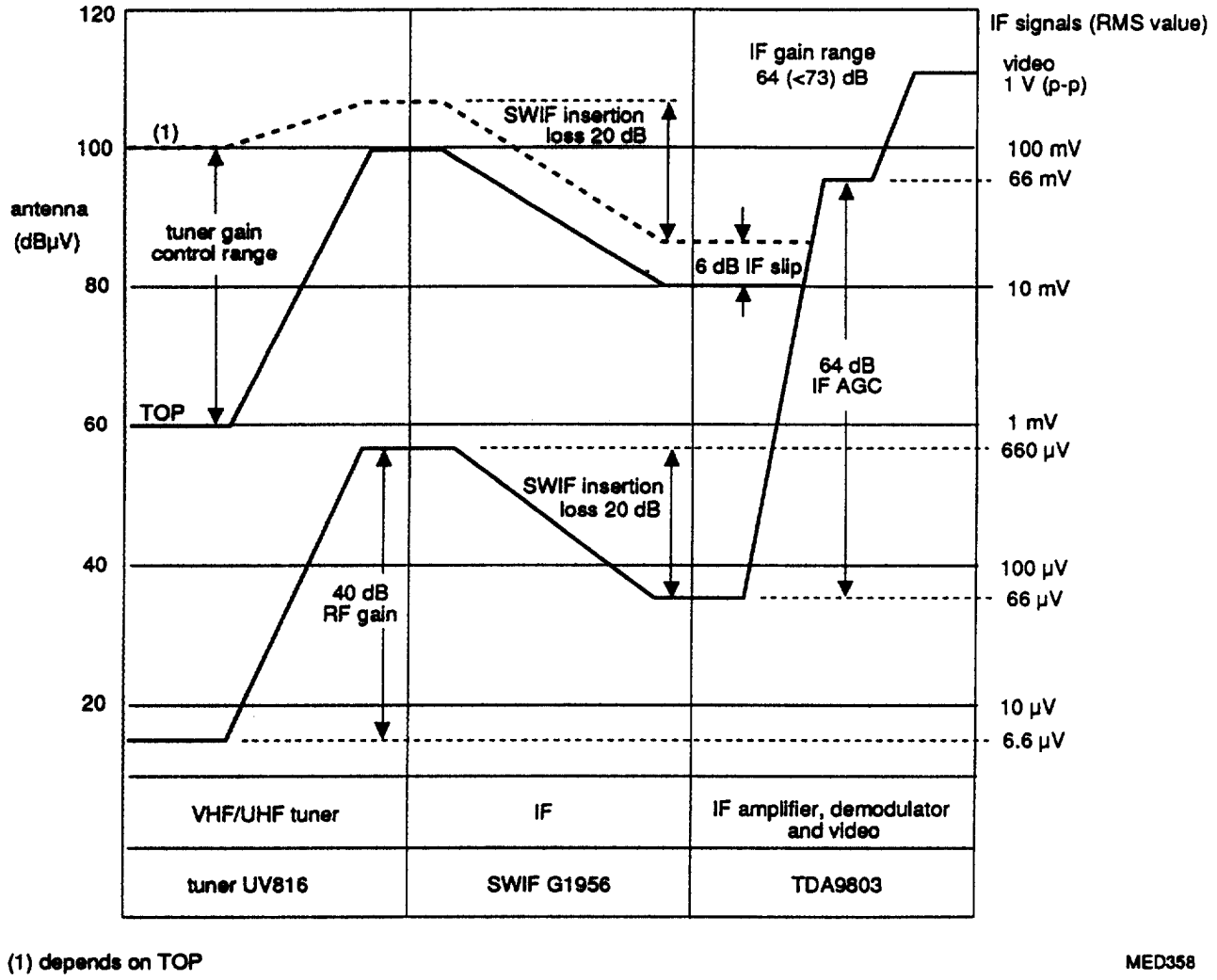


Fig.11 Front end level diagram.

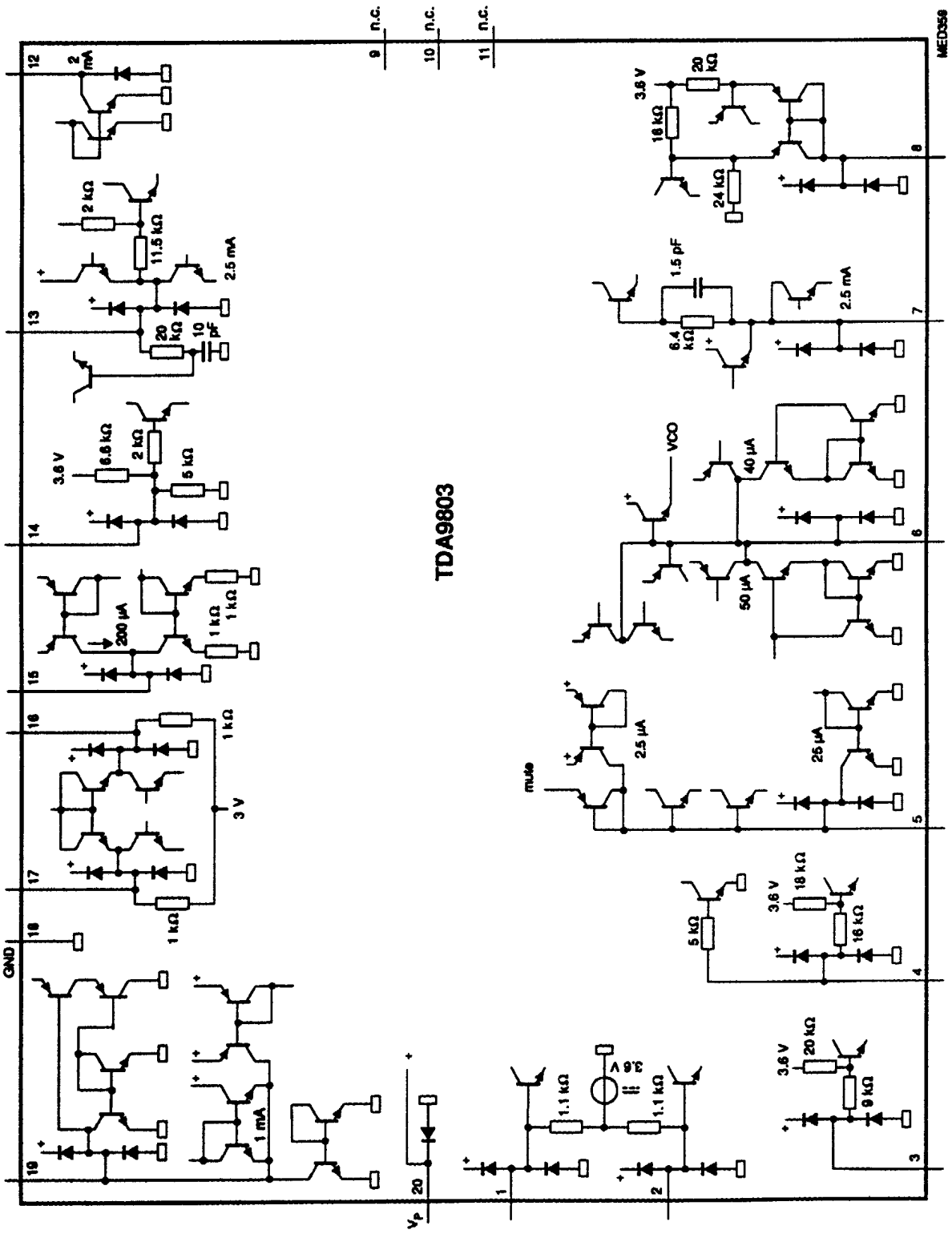
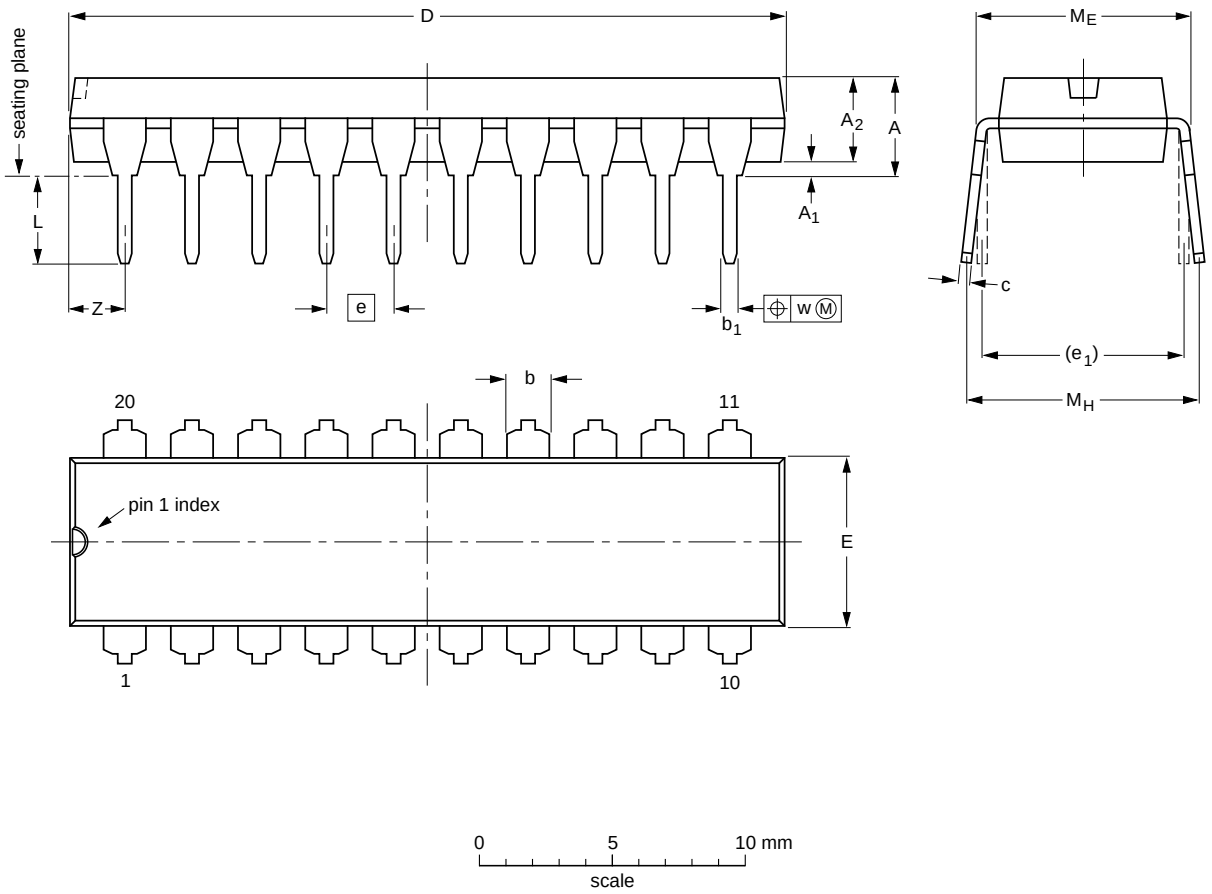


Fig.12 Internal circuits.

PACKAGE OUTLINE

DIP20: plastic dual in-line package; 20 leads (300 mil) **SOT146-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

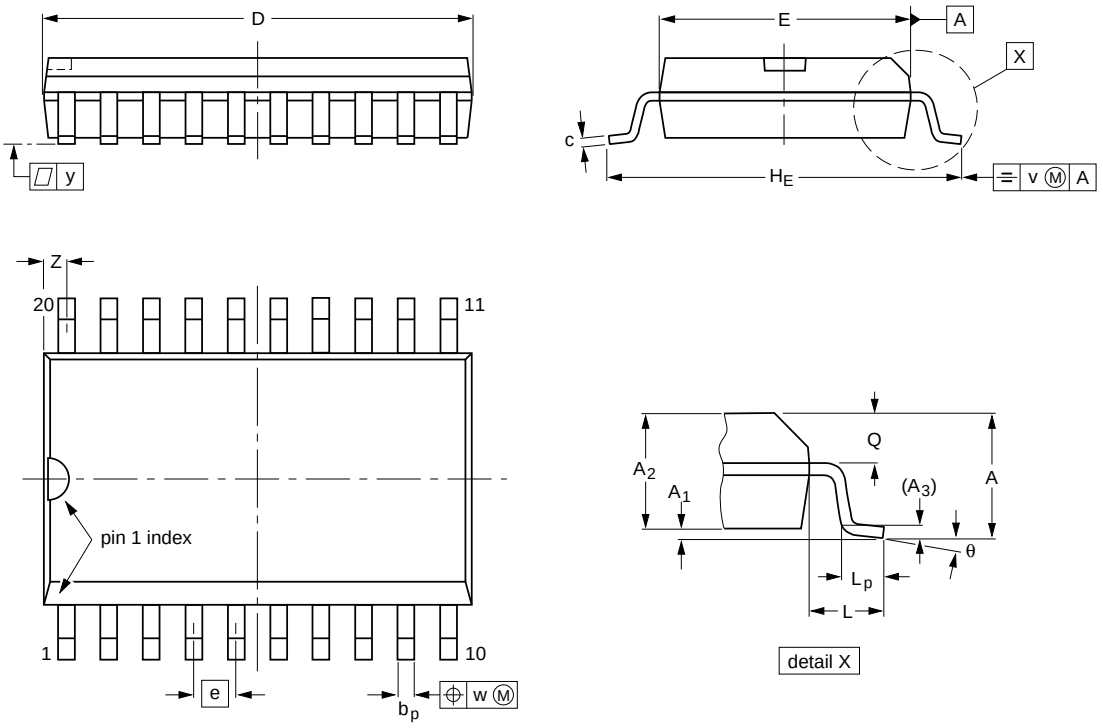
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.0
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT146-1			SC603			~~92-11-17~~ 95-05-24

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013AC				~~92-11-17~~ 95-01-24

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

DIP

Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

SO

Reflow soldering

Reflow soldering techniques are suitable for all SO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

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