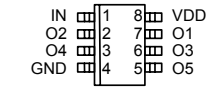
MONOLITHIC 5-TAP FIXED DELAY LINE (SERIES 3D7225)

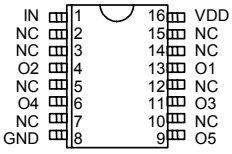
FEATURES

- All-silicon, low-power CMOS technology
- TTL/CMOS compatible inputs and outputs
- Vapor phase, IR and wave solderable
- Auto-insertable (DIP pkg.)
- Low ground bounce noise
- Leading- and trailing-edge accuracy
- **Delay range:** 0.75ns through 3500ns
- **Delay tolerance:** 2% or 0.5ns
- **Temperature stability:** ±2% typical (-40C to 85C)
- **Vdd stability:** ±1% typical (4.75V-5.25V)
- **Minimum input pulse width:** 30% of total delay
- 8-pin Gull-Wing available as drop-in replacement for hybrid delay lines

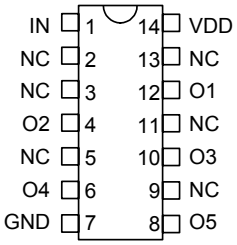
PACKAGES



3D7225Z-xx SOIC-8
3D7225M-xx DIP-8
3D7225H-xx Gull-Wing



3D7225S-xx SOL-16



3D7225-xx DIP-14
3D7225G-xx Gull-Wing
3D7225K-xx Unused pins removed

For mechanical dimensions, click here.
For package marking details, click here.

FUNCTIONAL DESCRIPTION

The 3D7225 5-Tap Delay Line product family consists of fixed-delay CMOS integrated circuits. Each package contains a single delay line, tapped and buffered at 5 points spaced uniformly in time. Tap-to-tap (incremental) delay values can range from 0.75ns through 700ns. The input is reproduced at the outputs without inversion, shifted in time as per the user-specified dash number. The 3D7225 is TTL- and CMOS-compatible, capable of driving ten 74LS-type loads, and features both rising- and falling-edge accuracy.

PIN DESCRIPTIONS

IN	Delay Line Input
O1	Tap 1 Output (20%)
O2	Tap 2 Output (40%)
O3	Tap 3 Output (60%)
O4	Tap 4 Output (80%)
O5	Tap 5 Output (100%)
VDD	+5 Volts
GND	Ground

The all-CMOS 3D7225 integrated circuit has been designed as a reliable, economic alternative to hybrid TTL fixed delay lines. It is offered in a standard 8-pin auto-insertable DIP and space saving surface mount 8-pin SOIC and 16-pin SOL packages.

TABLE 1: PART NUMBER SPECIFICATIONS

DASH NUMBER	TOLERANCES		INPUT RESTRICTIONS			
	TOTAL DELAY (ns)	TAP-TAP DELAY (ns)	Rec'd Max Frequency	Absolute Max Frequency	Rec'd Min Pulse Width	Absolute Min Pulse Width
-.75	3.0 ± 0.5*	0.75 ± 0.4	41.7 MHz	166.7 MHz	12.0 ns	3.00 ns
-1	4.0 ± 0.5*	1.0 ± 0.5	37.0 MHz	166.7 MHz	13.5 ns	3.00 ns
-1.5	6.0 ± 0.5*	1.5 ± 0.7	31.2 MHz	166.7 MHz	16.0 ns	3.00 ns
-2	8.0 ± 0.5*	2.0 ± 0.8	25.0 MHz	166.7 MHz	20.0 ns	3.00 ns
-2.5	10.0 ± 0.5*	2.5 ± 1.0	22.2 MHz	125.0 MHz	22.5 ns	4.00 ns
-4	16.0 ± 0.7*	4.0 ± 1.3	8.33 MHz	133.3 MHz	30.0 ns	6.00 ns
-5	25.0 ± 1.0	5.0 ± 1.5	13.3 MHz	66.7 MHz	37.5 ns	7.50 ns
-10	50.0 ± 1.0	10.0 ± 2.0	6.67 MHz	33.3 MHz	75.0 ns	15.0 ns
-20	100.0 ± 2.0	20.0 ± 4.0	3.33 MHz	16.7 MHz	150 ns	30.0 ns
-50	250.0 ± 5.0	50.0 ± 10	1.33 MHz	6.67 MHz	375 ns	75.0 ns
-100	500.0 ± 10	100 ± 20	0.67 MHz	3.33 MHz	750 ns	150 ns
-200	1000 ± 20	200 ± 40	0.33 MHz	1.67 MHz	1500 ns	300 ns
-700	3500 ± 70	700 ± 140	0.10 MHz	0.48 MHz	5250 ns	1050 ns

*** Total delay referenced to Tap1 output; Input-to-Tap1 = 5.0ns ± 1.0ns**
NOTE: Any dash number between .75 and 700 not shown is also available as standard.

APPLICATION NOTES

OPERATIONAL DESCRIPTION

The 3D7225 five-tap delay line architecture is shown in Figure 1. The delay line is composed of a number of delay cells connected in series. Each delay cell produces at its output a replica of the signal present at its input, shifted in time. The delay cells are matched and share the same compensation signals, which minimizes tap-to-tap delay deviations over temperature and supply voltage variations.

INPUT SIGNAL CHARACTERISTICS

The Frequency and/or Pulse Width (high or low) of operation may adversely impact the specified delay accuracy of the particular device. The reasons for the dependency of the output delay accuracy on the input signal characteristics are varied and complex. Therefore a Maximum and an Absolute Maximum operating input frequency and a Minimum and an Absolute Minimum operating pulse width have been specified.

OPERATING FREQUENCY

The Absolute Maximum Operating Frequency specification, tabulated in Table 1, determines the highest frequency of the delay line input signal that can be reproduced, shifted in time at the device output, with acceptable duty cycle distortion.

The Maximum Operating Frequency specification determines the highest frequency of the delay line input signal for which the output delay accuracy is guaranteed.

To guarantee the Table 1 delay accuracy for input frequencies higher than the Maximum Operating Frequency, the 3D7225 must be tested at the user operating frequency. Therefore, to facilitate production and device identification, the part number will include a custom reference designator identifying the intended frequency of operation. The programmed delay accuracy of the device is guaranteed, therefore, only at the user specified input frequency. Small input frequency variation about the selected frequency will only marginally impact the programmed delay accuracy, if at all. Nevertheless, it is strongly recommended that the engineering staff at DATA DELAY DEVICES be consulted.

OPERATING PULSE WIDTH

The Absolute Minimum Operating Pulse Width (high or low) specification, tabulated in Table 1, determines the smallest Pulse Width of the delay line input signal that can be reproduced, shifted in time at the device output, with acceptable pulse width distortion.

The Minimum Operating Pulse Width (high or low) specification determines the smallest Pulse Width of the delay line input signal for which the output delay accuracy tabulated in Table 1 is guaranteed.

To guarantee the Table 1 delay accuracy for input pulse width smaller than the Minimum Operating Pulse Width, the 3D7225 must be tested at the user operating pulse width. Therefore, to facilitate production and device identification, the part number will include a

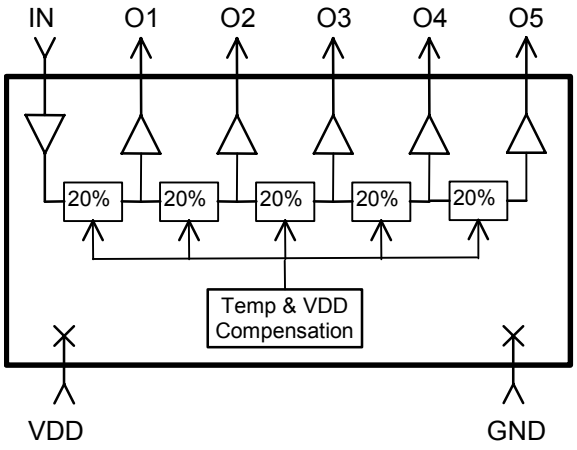


Figure 1: 3D7225 Functional Diagram

APPLICATION NOTES (CONT'D)

custom reference designator identifying the intended frequency and duty cycle of operation. The programmed delay accuracy of the device is guaranteed, therefore, only for the user specified input characteristics. Small input pulse width variation about the selected pulse width will only marginally impact the programmed delay accuracy, if at all. Nevertheless, it is strongly recommended that the engineering staff at DATA DELAY DEVICES be consulted.

POWER SUPPLY AND TEMPERATURE CONSIDERATIONS

The delay of CMOS integrated circuits is strongly dependent on power supply and temperature. The monolithic 3D7225 programmable delay line utilizes novel and innovative compensation circuitry to minimize the delay variations induced by fluctuations in power supply and/or temperature.

The thermal coefficient is reduced to 250 PPM/C, which is equivalent to a variation, over the -40C to 85C operating range, of ±2% from the room-temperature delay settings and/or 1.0ns, whichever is greater. The power supply coefficient is reduced, over the 4.75V-5.25V operating range, to ±1% of the delay settings at the nominal 5.0VDC power supply and/or 1.0ns, whichever is greater. **It is essential that the power supply pin be adequately bypassed and filtered. In addition, the power bus should be of as low an impedance construction as possible. Power planes are preferred.**

DEVICE SPECIFICATIONS

TABLE 2: ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
DC Supply Voltage	V_{DD}	-0.3	7.0	V	
Input Pin Voltage	V_{IN}	-0.3	V_{DD}+0.3	V	
Input Pin Current	I_{IN}	-1.0	1.0	mA	25C
Storage Temperature	T_{STRG}	-55	150	C	
Lead Temperature	T_{LEAD}		300	C	10 sec

TABLE 3: DC ELECTRICAL CHARACTERISTICS

(-40C to 85C, 4.75V to 5.25V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Static Supply Current*	I_{DD}		3.5	5.5	mA	
High Level Input Voltage	V_{IH}	2.0			V	
Low Level Input Voltage	V_{IL}			0.8	V	
High Level Input Current	I_{IH}			1.0	µA	$V_{IH} = V_{DD}$
Low Level Input Current	I_{IL}			1.0	µA	V_{IL} = 0V
High Level Output Current	I_{OH}		-35.0	-4.0	mA	V_{DD} = 4.75V V_{OH} = 2.4V
Low Level Output Current	I_{OL}	4.0	15.0		mA	V_{DD} = 4.75V V_{OL} = 0.4V
Output Rise & Fall Time	T_R & T_F		2.0	2.5	ns	C_{LD} = 5 pf

*I_{DD}(Dynamic) = 5 * C_{LD} * V_{DD} * F
where: C_{LD} = Average capacitance load/tap (pf)
F = Input frequency (GHz)

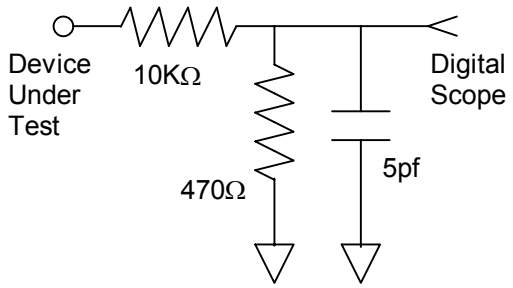
Input Capacitance = 10 pf typical
Output Load Capacitance (C_{LD}) = 25 pf max

SILICON DELAY LINE AUTOMATED TESTING

TEST CONDITIONS

INPUT:
Ambient Temperature: 25°C ± 3°C
Supply Voltage (Vcc): 5.0V ± 0.1V
Input Pulse: High = 3.0V ± 0.1V
Low = 0.0V ± 0.1V
Source Impedance: 50Ω Max.
Rise/Fall Time: 3.0 ns Max. (measured between 0.6V and 2.4V)
Pulse Width: PW_{IN} = 1.25 x Total Delay
Period: PER_{IN} = 2.5 x Total Delay

OUTPUT:
R_{load}: 10KΩ ± 10%
C_{load}: 5pf ± 10%
Threshold: 1.5V (Rising & Falling)



NOTE: The above conditions are for test only and do not in any way restrict the operation of the device.

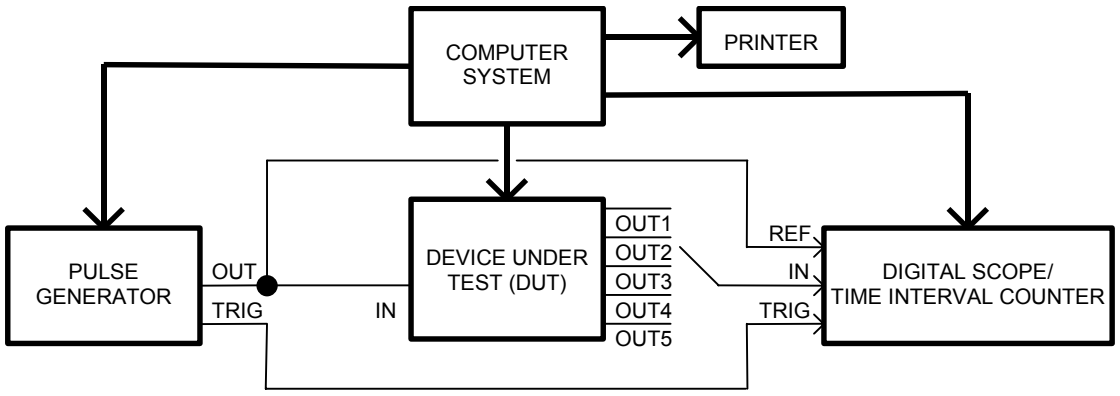


Figure 2: Test Setup

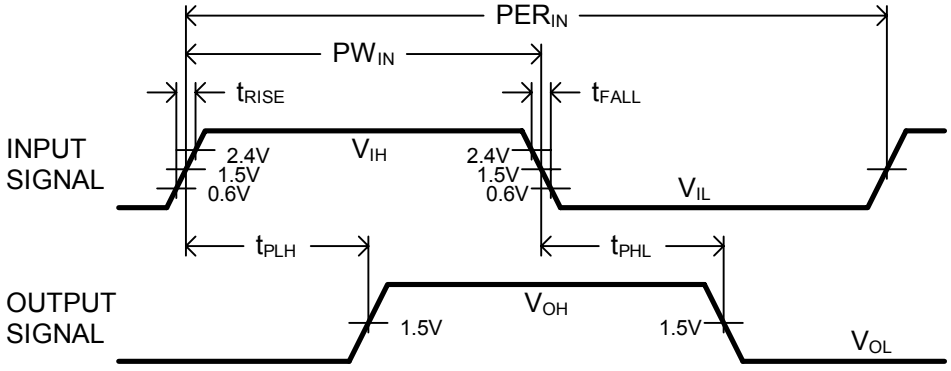


Figure 3: Timing Diagram