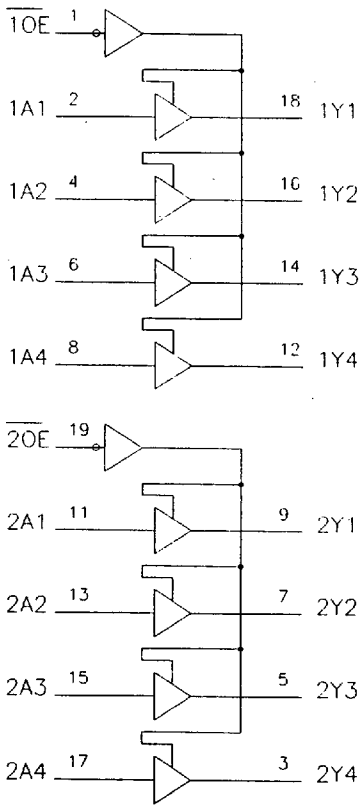
Preliminary

Radiation Hardened 54LVT244RP

3.3V ABT Octal Buffers/ Drivers

For Space Applications



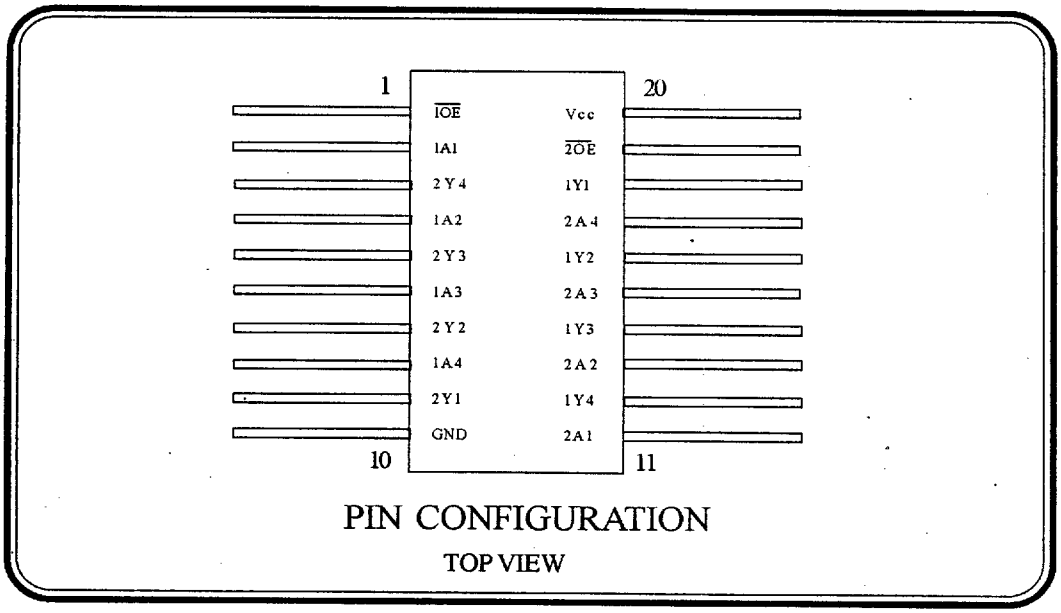
54LVT244RP Logic Diagram (Positive Logic)

SEI's 54LVT244RP (RP for RAD-PAK®) octal buffers/drivers microcircuit features a minimum 100 kilorad (Si) total dose tolerance. Using SEI's radiation hardened RAD-PAK® packaging technology, the 54LVT244RP is fully equivalent to the commercial 54LVT244 from Industry Standard. The 54LVT244RP is designed specifically for low voltage (3.3V) V_{CC} operation, but with the capability to provide a TTL interface to a 5V system environment. The 54LVT244RP is organized as two 4-bit drivers with separate output-enable ($\overline{OE}$) inputs. When $\overline{OE}$ is low, the device passes data from the A inputs to the Y outputs. When $\overline{OE}$ is high, the outputs are in the high-impedance state. Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level. The 54LVT245RP has a total dose survivability of 100 krad (Si) and is available in Class S packaging and screening.

SPACE ELECTRONICS INCORPORATED

Tel: (619) 452-4167 Fax: (619) 452-5499
INTERNET: 102005.1635@COMPUSERVE.COM

Radiation Hardened
54LVT244RP 3.3V Advanced BiCMOS Technology Octal Buffers/Drivers



PIN CONFIGURATION

TOP VIEW

Features:

- 3.3V ABT Octal Buffers/Drivers with 3-State Outputs
- Pin Compatible with Industry Standard 54LVT244
- RAD-PAK® Radiation Hardened Against Natural Space Radiation
- Total Dose Hardness >100 krad (Si)
- Single Event Effect
  - No Latchup, >119MeV/mg/cm²
- Package:
  - 20 Pin RAD-PAK® flat pack
  - 20 Pin RAD-PAK® DIP

  Package dimensions to be determined
- Operating Temperature Range: -55 °C to 125°C
- JEDEC Approved Byte Wide Pinout
- Supports Mixed-Mode Signal Operation
  - 5V Input and Output Voltages with 3.3V Vcc
- Supports Unregulated Battery Operation Down to 2.7V.
- Typical V_{OLP} (Output Ground Bounce) < 0.8V at V_{CC}=3.3V, T_A=25°C
- Latch-Up Performance Exceeds 500mA Per JEDEC Standard JESD-17
- Supports Live Insertion
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors

TQM
Total Quality Management

Aug 1996

For Further Information Contact:
Space Electronics Inc.
4031 Sorrento Valley Blvd., San Diego, CA 92121
(619) 452-4167 Fax (619) 452-5499
INTERNET: 102006.1635@COMPUSERVE.COM

54LVT244RP ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN	MAX	UNITS
Supply Voltage Range	V_{CC}	-0.5	4.6	V
Input Voltage Range	V_I	-0.5	7	V
Voltage Range Applied to any Output in the High State or Power-Off State	V_O 1/	-0.5	7	V
Current Into Any Output in the Low State	I_O		96	mA
Current Into Any Output in the High State	I_O 2/		48	mA
Input Clamp Current	I_{IK} ($V_I < 0$)		-50	mA
Output Clamp Current	I_{OK} ($V_O < 0$)		-50	mA
Total Power Dissipation @ T_A = +55°C 3/			1.6	W

54LVT244RP RECOMMENDED OPERATING CONDITIONS 4/

PARAMETER	SYMBOL	MIN	MAX	UNITS
Supply Voltage	V_{CC}	2.7	3.6	V
High-Level Input Voltage	V_{IH}	2		V
Low-Level Input Voltage	V_{IL}		0.8	V
Input Voltage	V_I		5.5	V
High-Level Output Current	I_{OH}		-24	mA
Low-Level Output Current	I_{OL}		48	mA
Input Transition Rise or Fall Rate	$\Delta t/\Delta v$		10	ns/V
Operating Free-Air Temperature	T_A	-55	125	°C

Note:

1/ The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2/ This current flows only when the output is in the high state and $V_O > V_{CC}$.

3/ The maximum package poewr dissipation is calculated using a junction temperature of 150°C and a board trace lenght of 750 mils.

4/ Unused control inputs must be held high or low to prevent them from floating.

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SAN DIEGO, CA 92121
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54LVT244RP DC ELECTRICAL CHARACTERISTICS

(T_A = -55°C to 125°C, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP 5/	MAX	UNIT
Input Clamp Voltage	V_{IK}	V_{CC} = 2.7V,	I_I = -18mA			1.2	V
High-Level Output Voltage	V_{OH}	V_{CC} = Min to Max 6/,	I_{OH} = -100µA	V_{CC} - 0.2			V
		V_{CC} = 2.7V,	I_{OH} = -8mA	2.4			V
		V_{CC} = 3V,	I_{OH} = -24mA	2			
Low-Level Output Voltage	V_{OL}	V_{CC} = 2.7V	I_{OL} = 100µA			0.2	
			I_{OL} = 24mA			0.5	
		V_{CC} = 3V	I_{OL} = 16mA			0.4	
			I_{OL} = 32mA			0.5	
			I_{OL} = 48mA			0.55	
Input Current	I_I	V_{CC} = 0 or Max 6/,	V_I = 5.5V			50	µA
		V_{CC} = 3.6V	V_I = V_{CC} or GND (Control Inputs)	-1		1	
			V_I = V_{CC} (Data Inputs)			1	
			V_I = 0 (Data Inputs)			-5	
Input Hold Current	$I_{I(hold)}$	V_{CC} = 3V	V_I = 0.8V (A Inputs)	75			µA
			V_I = 2V (A Inputs)	-75			
Off-State High-Level Output Current	I_{OZH}	V_{CC} = 3.6V,	V_O = 3V			5	µA
Off-State Low-Level Output Current	I_{OZL}	V_{CC} = 3.6V,	V_O = 0.5V			-5	µA
Supply Current	I_{CC}	V_{CC} = 3.6V, I_O = 0, V_I = V_{CC} or GND	Outputs High		0.12	0.39	mA
			Outputs Low		8.6	14	
			Outputs Disabled		0.12	0.39	

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54LVT244RP DC ELECTRICAL CHARACTERISTICS (continued)

(T_A = -55°C to 125°C, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP 5/	MAX	UNIT
Supply Current Change 7/	ΔI_{CC}	V_{CC} = 3V to 3.6V, One Input at V_{CC} - 0.6V, Other Inputs at V_{CC} or GND			0.3	mA
Input Capacitance	C_i	V_I = 3V or 0		4		pF
Output Capacitance	C_o	V_O = 3V or 0		8		pF

Note:

5/ All typical values are at Vcc = 3.3V, TA = 25oC.

6/ For conditions shown as Min or Max, use appropriate value specified under recommended operating conditions.

7/ This is the increase in supply current for each input that is at the speicifed TTL voltage level rather than Vcc or GND.

54LVT244RP SWITCHING CHARACTERISTICS

(T_A = -55°C to 125°C, C_L = 50pF, unless otherwise noted)

PARAMETER	SYMBOL	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	MAX	UNIT
Propagation Delay Time, Low-to-High Level Output	t_{PLH}	A	Y	V_{CC} = 3.3 ± 0.3V	0.5	4.7	ns
				V_{CC} = 2.7V		5.2	
Propagation Delay Time, High-to-Low Level Output	t_{PHL}			V_{CC} = 3.3 ± 0.3V	0.5	4.4	ns
				V_{CC} = 2.7V		5.4	
Enable Time to High-Level	t_{PZH}	OE	Y	V_{CC} = 3.3 ± 0.3V	0.8	5.4	
				V_{CC} = 2.7V		6.5	
Enable Time to Low-Level	t_{PZL}			V_{CC} = 3.3 ± 0.3V	0.8	5.4	
				V_{CC} = 2.7V		7.6	
Disable Time from High-Level	t_{PHZ}	OE	Y	V_{CC} = 3.3 ± 0.3V	1.5	6.2	
				V_{CC} = 2.7V		6.9	
Disable Time from Low-Level	t_{PLZ}			V_{CC} = 3.3 ± 0.3V	1.2	5.5	
				V_{CC} = 2.7V		6	

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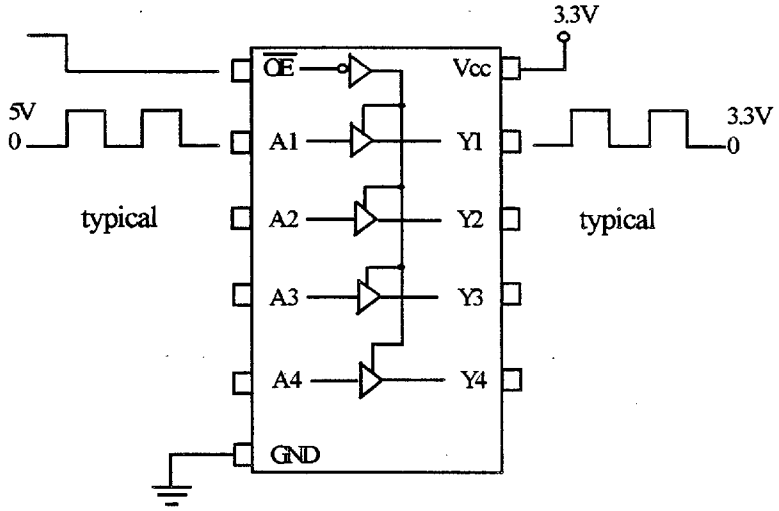

Figure 1. Application Circuit - TTL to 3.3V Logic Conversion

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

Figure 2. Functional Table

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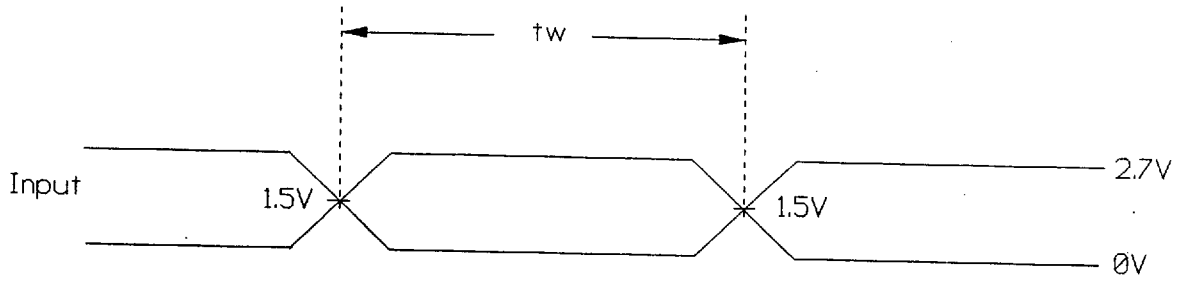
Voltage Waveforms
Pulse Duration



Voltage Waveforms
Setup and Hold Times

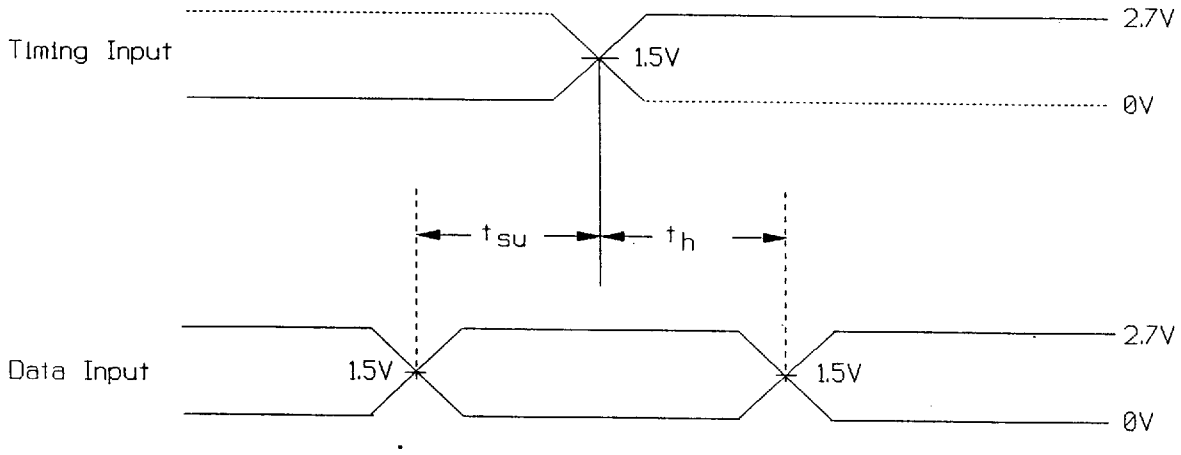


Figure 3. Voltage Waveforms

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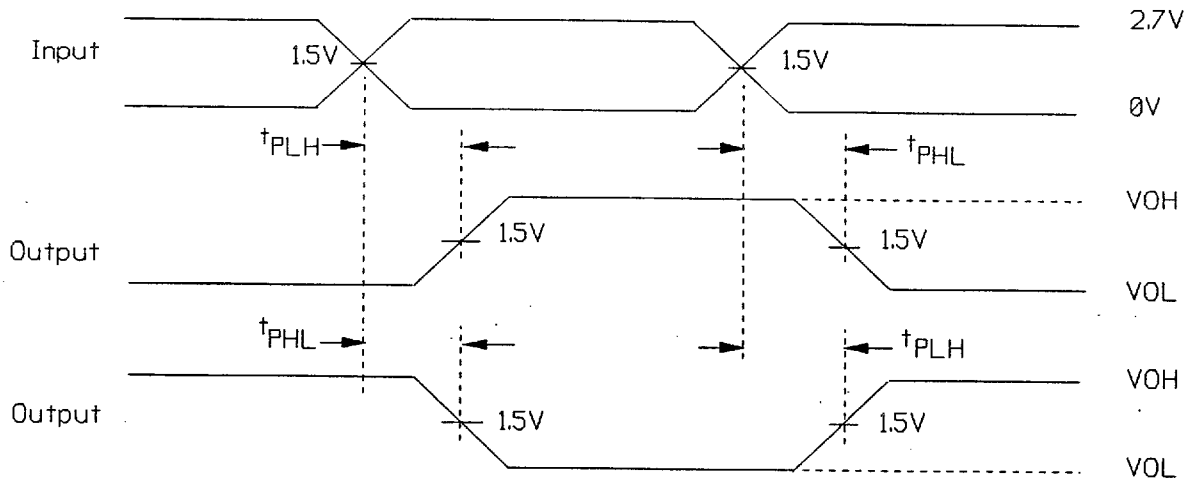
Voltage Waveforms
Propagation Delay Times
Inverting and Noninverting Outputs



Voltage Waveforms
Enable and Disable Times
Low-and High-Level Enabling

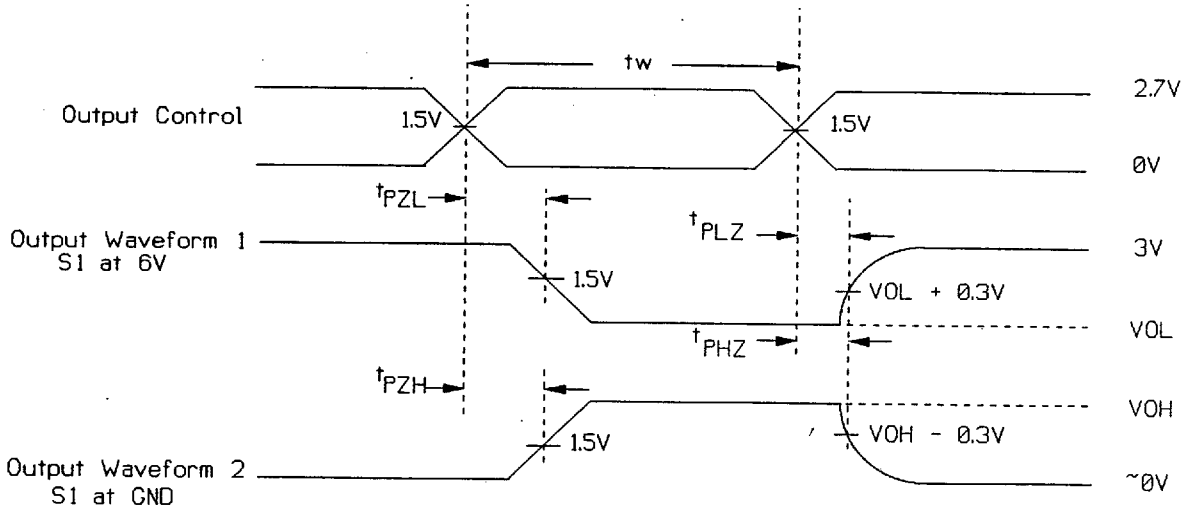


Figure 3. Voltage Waveforms (continue)

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