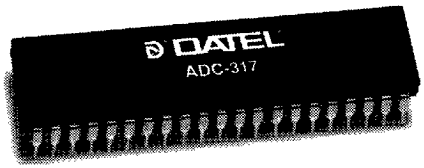
ADC-317
8-Bit, 125MHz, Low-Power Flash A/D Converter

FEATURES

- **8-Bit resolution**
- **±1/2LSB integral and differential nonlinearity**
- **125MHz minimum conversion rate**
- **Low power consumption (870mW)**
- **Wide input bandwidth (200MHz)**
- **Low input capacitance (18pF)**
- **Single –5.2V supply**



GENERAL DESCRIPTION

DATEL's ADC-317 is an 8-bit, high-speed flash A/D converter capable of digitizing analog signals at a guaranteed rate of 125MHz. The ADC-317 is virtually free of sparkle code errors up to Nyquist conditions and has a built-in integral nonlinearity (INL) compensation circuit that keeps the INL at typically ±0.5LSB. The ADC-317 is available in a 42-pin, plastic, dual-in-line package and operates over the extended commercial temperature range of –20 to +75°C. The digital I/O levels of this A/D converter are compatible with ECL 100K/10KH/10K families.

Compared with earlier devices, the ADC-317's performance is superior due to the incorporation of advanced processing, new circuit design, and carefully considered layout.

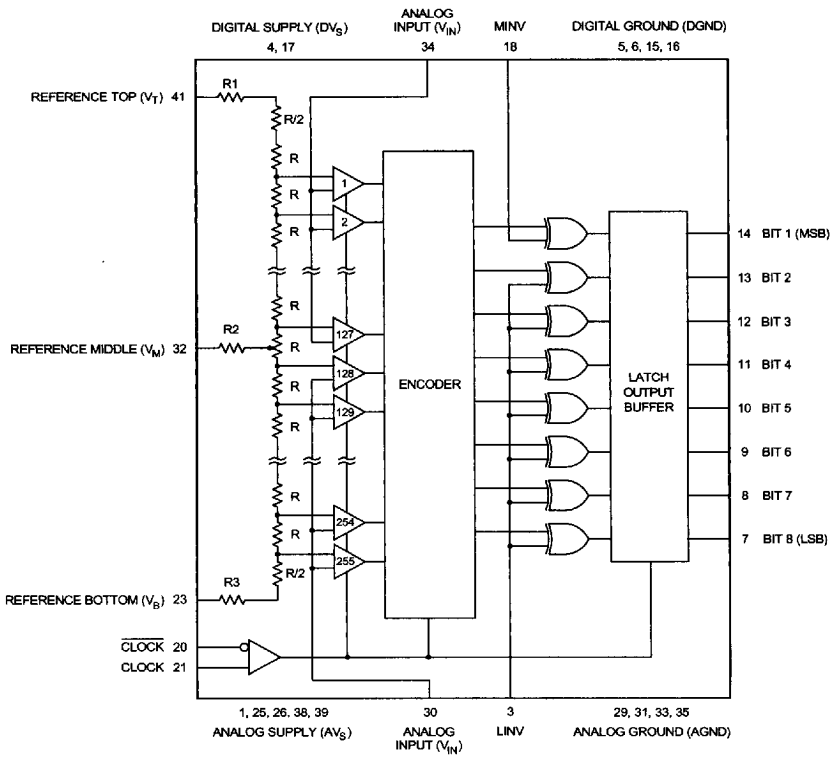


Figure 1. Functional Block Diagram

ABSOLUTE MAXIMUM RATINGS

PARAMETERS	LIMITS	UNITS
Supply Voltages AV_S, DV_S	+0.5 to –7	Volts
Input Voltage V_{IN}	+0.5 to –2.7	Volts
Reference Voltages V_T, V_B, V_M	+0.5 to –2.7	Volts
Reference Voltage $\lvert V_T - V_B \rvert$	2.5	Volts
Digital Inputs	+0.5 to –4	Volts
|Clock – $\overline{\text{Clock}}$|	2.7	Volts
V_M Input Current	–3 to +3	mA
Digital Output Currents	0 to –30	mA

FUNCTIONAL SPECIFICATIONS

(Specifications are typical at T_A = +25°C, AVs = DVs = –5.2V, V_T = 0V, V_B = –2.0V, fs = 125MHz unless otherwise specified.)

INPUTS	MIN.	TYP.	MAX.	UNITS
Analog Input Voltage	—	0 to –2	—	Volts
Analog Input Capacitance (V_{IN} = –1V + 0.07Vrms)	—	18	—	pF
Analog Input Resistance	50	190	—	kΩ
Analog Input Bias Current (V_{IN} = –1V)	+20	+130	+400	µA
Digital Input Voltage				
V_H	–1.13	—	—	Volts
V_L	—	—	–1.50	Volts
Digital Input Current				
I_H (@ V_H = –0.8V)	0	—	+50	µA
I_L (@ V_L = –1.6V)	–50	—	+50	µA
Digital Input Capacitance	—	7	—	pF
Clock Pulse Width				
T_{PW1}	3.8	—	—	ns
T_{PW0}	3.8	—	—	ns
REFERENCE INPUTS				
Reference Input Voltage ①				
V_B	–2.2	–2.0	–1.8	Volts
V_T	–0.1	0	+0.1	Volts
Reference Resistance, V_T to V_B	75	110	155	Ω
Offset Voltage				
V_B	0	+9	+24	mV
V_T	–8	–17	–32	mV
PERFORMANCE				
Resolution	8	—	—	Bits
Conversion Rate	125	160	—	MHz
Integral Non-linearity	—	±0.5	±0.8	LSB
Differential Non-linearity	—	±0.5	±0.7	LSB
Differential Gain Error	—	1.0	—	%
Differential Phase Error	—	0.5	—	deg.
Aperture Jitter (Tj)	—	10	—	ps
Sampling Delay (Tsd)	0.3	1.5	3.0	ns
DYNAMIC CHARACTERISTICS ②				
Full Scale Input Bandwidth (V_{IN} = 2V peak-to-peak Bandwidth (@ –3dB)	200	—	—	MHz
Signal-to-Noise Ratio				
Input = 1MHz, FS	—	46	—	dB
Input = 31.249MHz, FS	—	40	—	dB
Error Rate				
Input = 31.249MHz, FS (Error = 16 LSB min.)	—	10^{-14}	10^{-9}	TPS ③

OUTPUTS	MIN.	TYP.	MAX.	UNITS
Digital Output ④				
Logic High Level	–1.10	—	—	Volts
Logic Low Level	—	—	–1.62	Volts
Output Delay (Td)	3.0	3.6	4.2	ns
Output Rise Time (Tr)	0.5	0.9	1.2	ns
Output Fall Time (Tf)	0.5	1.0	1.3	ns
POWER REQUIREMENTS				
Supply Voltage AV_S, DV_S	–4.95	–5.2	–5.5	Volts
Supply Current	—	–160	–230	mA
Power Dissipation	—	870	—	mW
DGND - AGND	—	—	±50	mV
AV_S - DV_S	—	—	±50	mV
PHYSICAL/ENVIRONMENTAL				
Operating Temperature, Ambient	–20	—	+75	°C
Storage Temperature	–65	—	+150	°C
Thermal Impedance, θja	—	62	—	°C/W
Package	42-pin plastic DIP			
Weight	0.23 ounces (6.4 grams)			

Footnotes:
① Refer to Functional Block Diagram, Figure 1.
② For conversion rate of 125MHz.
③ TPS = Times per sample. Each unit is production tested for 10 seconds.
④ 220Ω pull-down resistors required on digital outputs.

TECHNICAL NOTES

1. Even with its low input capacitance of 18pF, the ADC-317 still requires an input amplifier with good drive capability. The amplifier will require wide bandwidth and high slew rate (±250V/µs typical) to take full advantage of the converter's input bandwidth.

2. The input impedance of the A/D is primarily capacitive which may result in the input amplifier becoming unstable and causing oscillations. Stop oscillations by placing a 2-to-4Ω resistor between the amplifier and the converter's input.

3. CLOCK and $\overline{\text{CLOCK}}$ (ECL) are usually differentially driven. The ADS-317 is operable without $\overline{\text{CLOCK}}$ input, but using complementary inputs is recommended to obtain stable high-speed performance.

4. The polarity of the output data is controlled by input MINV, which controls the MSB alone, and LINV, which controls bits 2 through 8 (LSB). The combination of "0" and "1" on these inputs offer the user various code options shown in Table 1. Leave the inputs open for a logic level "0"; connect a 3.9kΩ resistor to GND for logic level "1".

5. Digital output bits 1 through 8 require 220Ω pull-down resistors connected to the negative supply rail. Refer to Figure 2.

6. The reference voltage range (–2.0V to 0V typical) determines the dynamic range of the input voltage. Adjustments to this range can be made within the range of V_B = –2 ±0.2V and V_T = 0V ±0.1V. The reference input V_B should be decoupled to GND using 1µF and 0.01µF capacitors. Improvement in the high-frequency stability can be achieved by decoupling terminal V_M using a 0.01µF capacitor.

7. The V_M input (pin 32) is used to achieve a more accurate linearity than that specified. The connection diagram shows an external circuit designed to maximize the ADC-317's linearity.

8. Tie all pins not being used to ground.

9. Substantial analog and digital ground planes must be provided. It is recommended that these ground planes are taken to a common point, the power ground plane, as close to the ADC as possible.

10. The analog and digital power supply inputs (–5.2V) are internally connected through a resistance of 4 to 6 Ohms, and it is possible to use one power source for both inputs. For best performance, the power supplied to the analog and digital inputs (–5.2V) should be supplied from separate, isolated power supplies. If one of the power supplies fails or is shorted to ground for more than 1 second, the device may be destroyed. Both –5.2V lines should be decoupled using 1µF and 0.01µF capacitors located as close to the pins as possible.

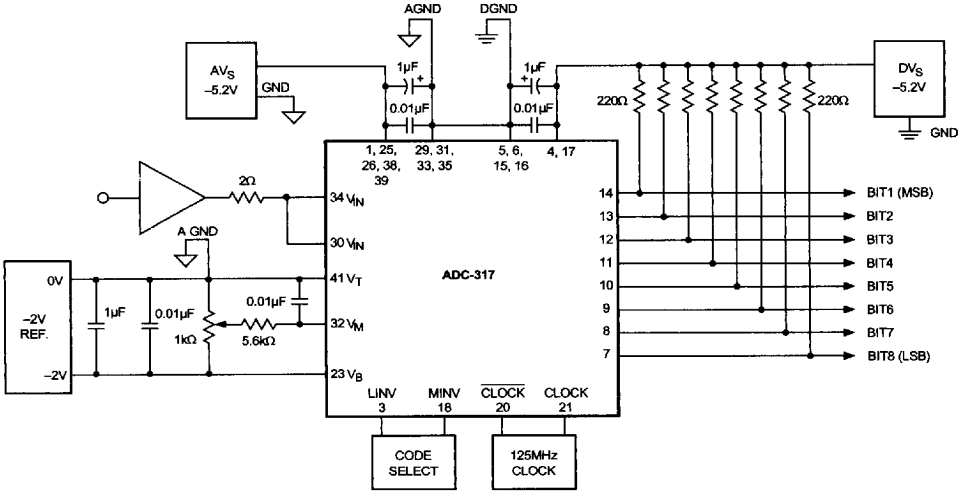


Figure 2. ADC-317 Typical Connection Drawing

Table 1. Digital Output

This table and the Timing Diagram indicate the compatibility between the analog input and the digital output code.

V_{IN}	MINV / LINV	1 / 1	0 / 1	1 / 0	0 / 0
0.0000V		000 . . . 00	100 . . . 00	011 . . . 11	111 . . . 11
–0.0078V		000 . . . 01	100 . . . 01	011 . . . 10	111 . . . 10
–0.9922V		011 . . . 11	111 . . . 11	000 . . . 00	100 . . . 00
–1.0000V		100 . . . 00	000 . . . 00	111 . . . 11	011 . . . 11
–1.9844V		111 . . . 10	011 . . . 10	100 . . . 01	000 . . . 01
–1.9922V		111 . . . 11	011 . . . 11	100 . . . 00	000 . . . 00

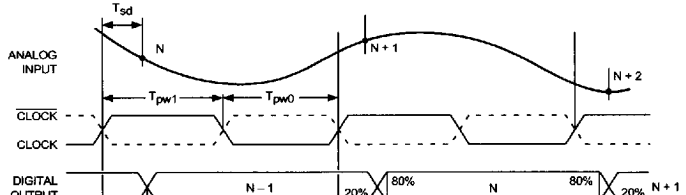


Figure 3. ADC-317 Simplified Timing Diagram

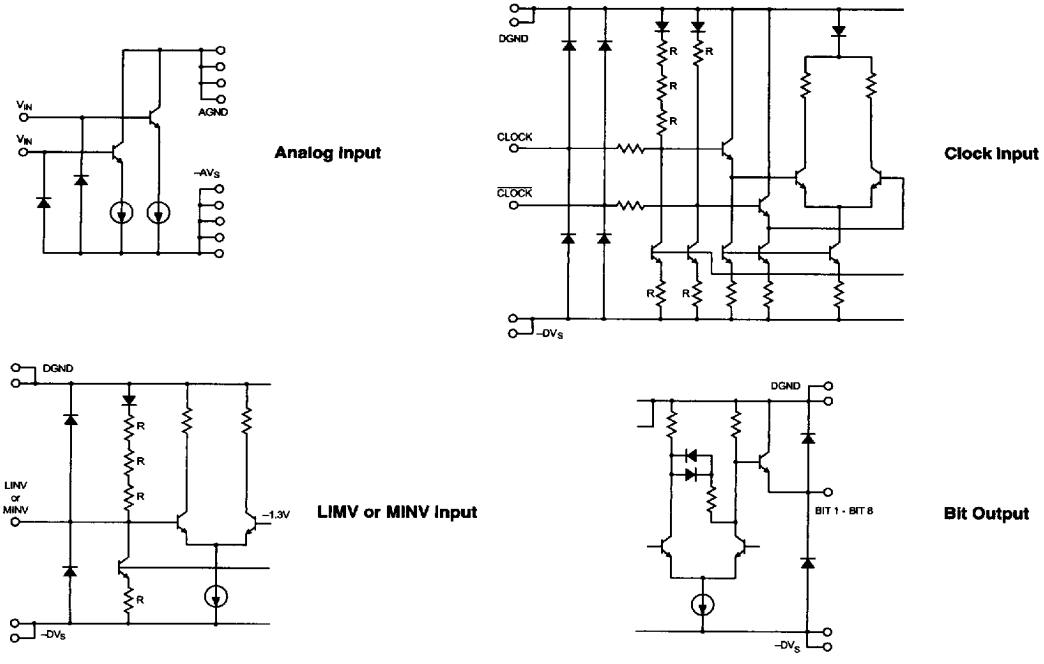


Figure 4. Equivalent Circuits

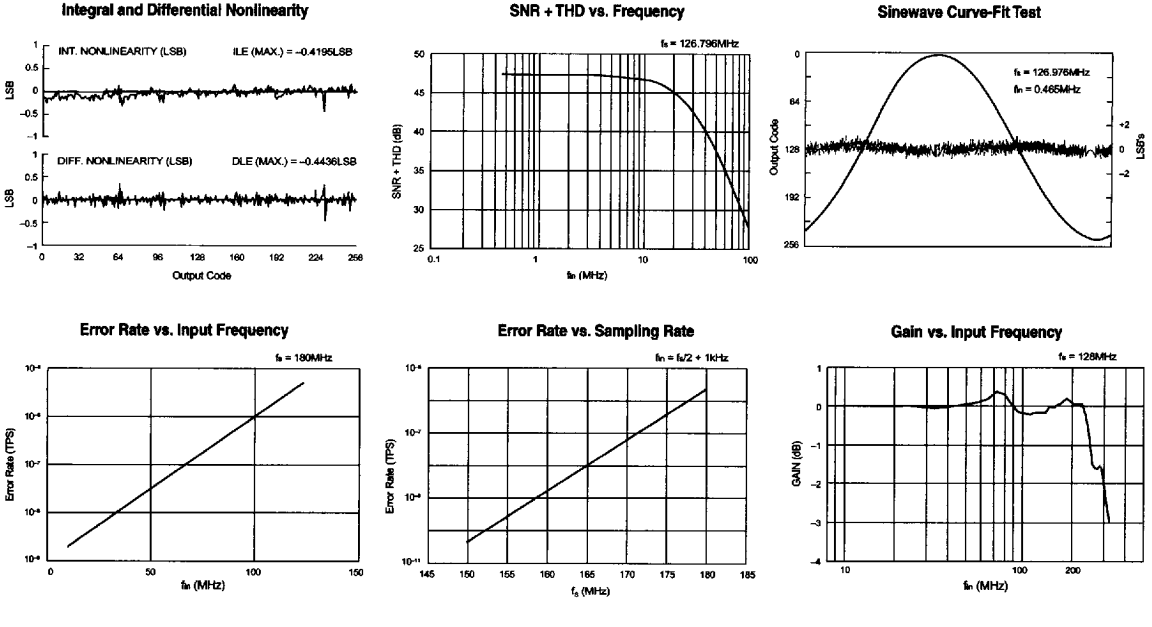


Figure 5. Typical Performance Curves

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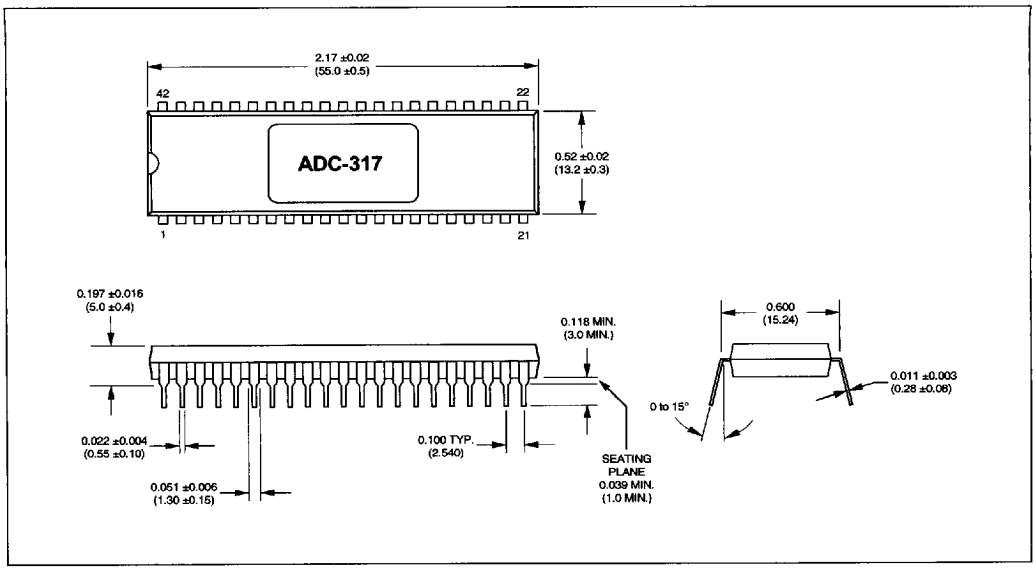
MECHANICAL DIMENSIONS
INCHES (mm)



INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	ANALOG SUPPLY (AV_S)	42	NO CONNECTION
2	NO CONNECTION	41	REFERENCE TOP (V_T)
3	LINV	40	NO CONNECTION
4	DIGITAL SUPPLY (DV_S)	39	ANALOG SUPPLY (AV_S)
5	DIGITAL GROUND	38	ANALOG SUPPLY (AV_S)
6	DIGITAL GROUND	37	NO CONNECTION
7	BIT 8 (LSB)	36	NO CONNECTION
8	BIT 7	35	ANALOG GROUND
9	BIT 6	34	ANALOG INPUT (V_{IN})
10	BIT 5	33	ANALOG GROUND
11	BIT 4	32	REF. MIDDLE (V_M)
12	BIT 3	31	ANALOG GROUND
13	BIT 2	30	ANALOG INPUT (V_{IN})
14	BIT 1 (MSB)	29	ANALOG GROUND
15	DIGITAL GROUND	28	NO CONNECTION
16	DIGITAL GROUND	27	NO CONNECTION
17	DIGITAL SUPPLY (DV_S)	26	ANALOG SUPPLY (AV_S)
18	MINV	25	ANALOG SUPPLY (AV_S)
19	NO CONNECTION	24	NO CONNECTION
20	$\overline{\text{CLOCK}}$	23	REF. BOTTOM (V_B)
21	CLOCK	22	NO CONNECTION

ORDERING INFORMATION

ADC-317	8-Bit, 125MHz Low-Power Flash A/D Converter