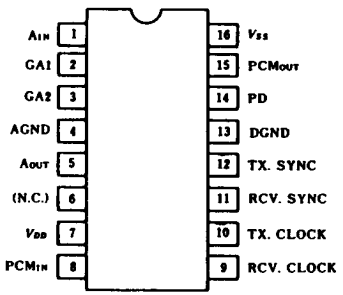
Single Chip CODEC with Filters (COMBO)

Features

- Single Chip CMOS CODEC with Filter in 16-pins DIL Package
- Power Supply Voltage ±5 V±5%, Low Power Dissipation (50 mW typ.)
- Follows A-Law (HD44237P)/μ-law(HD44238P)
- Exceeds CCITT and D4 Specifications
- Synchronous/Asynchronous Operation
- Internal Clock Generator Operation for 64 kHz to 2048 kHz PCM Rate as PLL Circuit
- Anti-Aliasing Filter (2nd order CR Active Filter)
- Voltage Reference (Internal-Trimmed)
- Input Amplifier with Uncommitted Plus/Minus Terminals
- Auto-Zero Cancel Circuit without External Component

Pin Configuration



(Top View)

Figure 1 Pin Assignment

Table 1. Pin Descriptions

HD44237P HD44238P No.	Symbol	Function	Remarks
1	A_{IN}	Analog Input	
2	G_{A1}	Gain Adjust 1	Feed-Back Input
3	G_{A2}	Gain Adjust 2	10 kΩ ≤ R_L C_L ≤ 100 pF
4	A_{GND}	Analog Ground	
5	A_{OUT}	Analog Output	R_L ≥ 600 Ω, C_L ≤ 100 pF
6	N.C.		Open
7	V_{DD}	Positive Pow.Sup.	5 V ± 5%
8	PCM_{IN}	PCM Data Input	(TTL)
9	RCV.CLK	PCM Bit Clock	(TTL) 64 to 2048 kHz
10	TX.CLK		
11	RCV.SYNC	Synchronization	(TTL) 8 kHz
12	TX.SYNC		
13	D_{GND}	Digital Ground	
14	P_D	Power Down	(TTL) "0" = down
15	PCM_{OUT}	PCM Data Output	Open Drain
16	V_{SS}	Negative Pow.Sup.	–5 V ± 5%

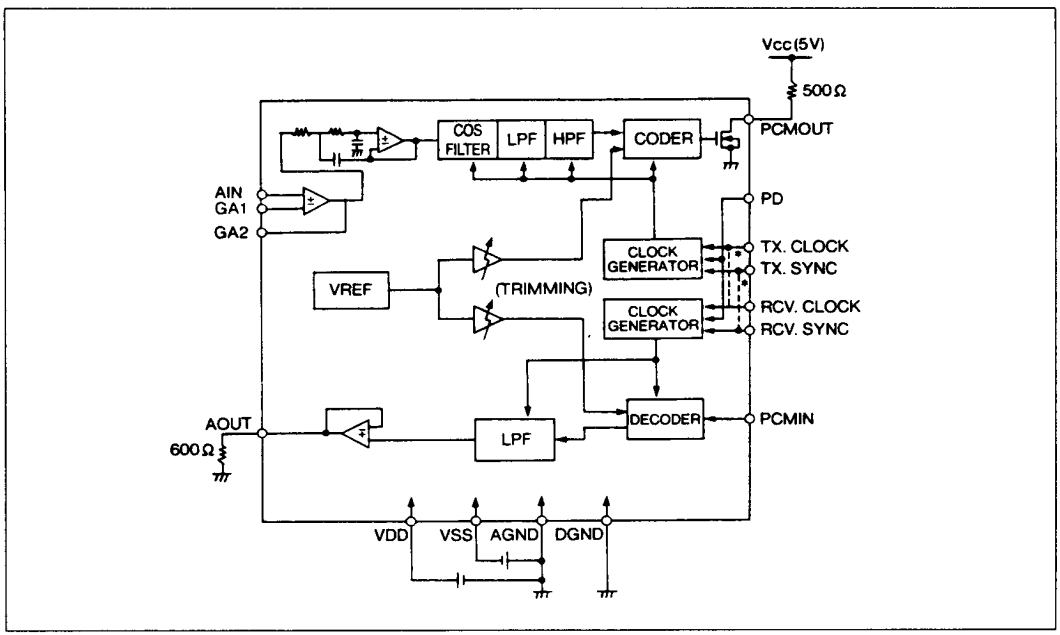


Figure 2 Block Diagram

General Description

The HD44237P, HD44238P are monolithic silicon gate CMOS Companding Encoder/Decoder chips designed to implement the per channel voice frequency Codecs used in PCM systems. The chips contain the band limiting filters and the analog/digital conversion circuits that conform to the A-Law or μ-Law companding characteristic.

HD44237P is A-Law. HD44238P is μ-Law.

These circuits provide the interface between the analog signals of the subscriber loop and digital signals of the PCM highway in a digital telephone switching system. The devices operate from dual power supplies of ± 5 V.

For a sampling rate of 8 kHz, PCM input/output data rate can be selected from 64 kHz to 2048 kHz in synchronous or asynchronous operation. Internal PLL circuits generate the internal clock from the 8 kHz synchronization clock.

Functional Description

Figure 2 shows the simplified block diagram of the HD44237P, HD44238P. The devices contain independent circuitry for processing transmit and receive signals. Switched capacitor filters provide the necessary bandwidth limiting of voice signals in both directions. Circuitry for coding and decoding operates on the principle of successive approximation, using charge redistribution in a binary weighted capacitor array to define segments and a resistor chain to define steps. The relationship between the PCM data word and the audio signal is defined just same as CCITT G711 Table 1 for HD44237P Table 2 for HD44238P respectively. A band-gap voltage generator supplies the reference level for the conversion process. 2nd Order CR Active Filter is implemented on chip to avoid the aliasing noise which is caused by the clock of transmit filter.

Transmit Section

Input analog signals first enter the chip at the uncommitted amplifier terminals. This op amp allows gain trim to be used if desired to set the 0 dB or 0 level in the system. This amplifier also operates as the 2nd order analog anti-aliasing filter. This filter eliminates the need for any off-chip filtering as it provides attenuation of 32 dB (typ) at 256 kHz and 40 dB (typ) at 512 kHz, the "effective" clock frequency of the following switched-capacitor Cosine Filter. From the Cosine Filter the signal enters a 5th Order Low-Pass Filter clocked at 128 kHz, followed by a 3rd Order High-Pass Filter clocked at 8 kHz. The resulting band-pass characteristics meet the CCITT, G.712 specifications. The output of the high pass filter is sampled by a capacitor array at the sampling rate of 8 kHz. The 8-bit PCM data is clocked out by the shift clock at one of 64 kHz to 2048 kHz. A auto-zero loop (without any external capacitor) provides DC offset cancellation by integrating the sign bit of the PCM data and feeding it back to the non-inverting input of the comparator.

An additional feature of the HD44237P is a signbit fixation circuit to reduce the idle channel noise during quiet periods. It is of particular importance because the A-Law transfer characteristic has "mid-riser" bias which enhances low level signals from crosstalk.

Receive Section

A shift clock, from 64 kHz to 2048 kHz, clock the PCM data into the input buffer register once every sampling period. A charge proportional to the received PCM data word appears on the decoder capacitor array. A sample and hold initialized to zero by a narrow pulse at the beginning of each sampling period integrates the charge and holds for the rest of the sampling period. A switched-capacitor 5th Order Low-Pass Filter clocked at 128 kHz smooths the sampled and held signal. It also performs the loss equalization to compensate for the sin x/x distortion due to the sample and hold operation. The filter output is available for driving electronic or transformer directly as long as the impedance is greater than 600 Ω.

Companding Law

The encoding and decoding characteristics of the Codecs comply with the requirements of CCITT G711 Table 1 or Table 2, corresponding to their comparing law. The even bits of PCM words are inverted for A-Law devices. Positive logic is used (the High level corresponds to '1').

Power Down Logic

Powering down the CODEC can be done in several ways. The most direct method is to drive the PD pin to a low level. Stopping SYNC input will also put the chip into the stand-by mode. The SYNC input can be held high, low or disconnected. After the chip being activated by these functions, the PCMOUT is in high impedance state and the AOUT is connected to AGND for about 1 ms to avoid the power-on noise.

Voltage Reference Circuit

A temperature compensated band-gap voltage generator provides a stable reference for the coder and decoder. Two amplifiers buffer the reference and supply it to the coder and decoder independently to minimize crosstalk. This reference voltage is trimmed to ensure a minimum gain error of ±0.1 dB at the nominal power supply voltage and the room temperature.

Timing Requirements

The CODECs do not require that the 8 kHz transmit and receive sampling strobes should be exactly 8 bit periods wide. The device has an internal bit counter that counts the number of data bits shifted. It is reset on the leading (+) edges of the strobe. The PCM output goes into a high impedance state after the 8th bit is shifted out. This allows the strobe signal to have any duty cycle as long as its repetition rate is 8 kHz and shift clock is synchronized to it. The clock rate can be selected from 64 kHz to 2048 kHz.

System Clock

The basic timing of the Codecs is provided by the internally generated clock from synchronization. The internal PLL (Phase Locked Loop) circuits generate 128 kHz clocks. These features make it possible that the clock rate of PCM bit shifting may be free in the range from 64 kHz to 2.048 MHz.

Bit Steal Control (HD44238P only)

For the bit steal period, the decoder output of μ-law CODEC should be shifted as half-bit of steps. For the CODECs, the power down control pin provides this function. If the low state of PD pin is less than 6 frames (0.75 ms), the device is not deactivated and the decoder output corresponding to the frame of the rising and falling edge of the pin is shifted as half-bit. And, if the low state is longer than 1.0 ms, the device is deactivated.

5

Pin/Function Descriptions

Pin	No	Descriptions
TX.CLOCK RCV.CLOCK	9 10	Any of 64 kHz to 2.048 MHz clock can be accepted with the pins. And they are automatically divided down to provide the internal clocks. These TTL compatible inputs shift PCM data out of the coder on the positive going edges and PCM data into the decoder on the negative going edges after receiving a positive edge on the SYNC, TX.SYNC/RCV.SYNC respectively.
TX.SYNC RCV.SYNC	11 12	These TTL compatible pulse inputs (typ. 8 kHz) are used for analog sampling and for initiating the PCM output from the coder and initiate clocking of PCM input data into the decoder. They must be synchronized with the CLOCK, TX.CLOCK/RCV.CLOCK with these positive going edges occurring after the falling edge of the CLOCK, TX.CLOCK/RCV.CLOCK respectively. The width of these signals are not critical. An internal bit counter generates the necessary timing for PCM output and input.
PCMOUT	15	This is a LS-TTL compatible open-drain output. It is active only during transmission of PCM output for 8 bit periods of CLOCK, TX.CLOCK/RCV.CLOCK signal following a positive edge on the SYNC, TX.SYNC/RCV.SYNC input. Data is clocked out by the positive edge of the CLOCK. One 500 Ω pull-up per 8 Codecs is required.
PCMIN	8	This is a TTL compatible input for supplying PCM input data to the decoder. Data is clocked in by the negative edge of CLOCK, RCV.CLOCK.
AIN GA1 GA2	1 2 3	These three pins are provided for connecting analog signals in the range of $-V_{REF}$ to $+V_{REF}$ to the device. The input stage can be connected as a unity gain amplifier, amplifier with gain or amplifier with adjustable gain. The adjustable gain configuration will facilitate calibration of the transmit channel. AIN is the input of analog signal of the amplifier. GA2 is the output of the amplifier. GA2 shall be loaded by the resistor above 10 kΩ or directly connected to GA1. GA1 is the negative feed back input of the amplifier. C_L should be less than 100 pF.
AOUT	5	This is the buffered output of the recreated analog signal from the received PCM data words. It can drive the impedance of 600 ohms. C_L should be less than 100 pF.
V_{DD} V_{SS} AGND DGND	7 16 4 13	These are power supply pins. V_{DD} and Vss are positive and negative supply pins respectively (typ. +5 V, –5 V). Analog and digital ground pins are separate for minimizing crosstalk.
PD	14	When this TTL compatible input is held low, the chip is put into the powered down mode regardless of strobes. The chip will also power down if the strobes stop. The strobes can be high, low or floating, but as long as they are static, the powered down mode is in effect. This pin should be pulled-up to V_{DD} to keep the device active or to control On/Off with strobes. For the μ-law devices, this pin also provides the half-bit decoder shift for the bit-steal frame according to alternating the state of the input.

Absolute Maximum Ratings

Item	Rating
V_{DD}	–0.3 to +7 V
Vss	+0.3 to –7 V
Storage Temperature	–55°C to 125°C
Power Dissipation	0.5 W
Digital Input/Output Voltage	–0.3 V < V_{IN} < V_{DD} + 0.3
Analog Input/Output Voltage	Vss – 0.3 V < V_{IN} < V_{DD} + 0.3

Electrical Characteristics

Static Characteristics (V_{DD} = 5 ± 0.25 V, Vss = –5 ± 0.25 V, V_{CC} = 5 ± 0.25 V, Ta = 0 to 70°C)

Sym.	Pin No.	Descriptions	Min	Typ	Max	Unit	Note/Conditions
I_{DD}	7	V_{DD} Current (OPE.)		5.5	10	mA	Note 1
Iss	16	Vss Current (OPE.)	–10	–4.5			AIN = 0 V
IDDST	7	V_{DD} Current (St.By.)		0.3	1		PCMIN = +0 CODE
ISSST	16	Vss Current (St.By.)	–0.2				R_L(GA2) = 10 kΩ
							R_L(AOUT) = 600 Ω
IL	1, 2, 8,	Leak Current	–10.0		10.0	µA	V_M = 0.8 V
	9, 10, 14		–10.0		10.0	µA	V_M = 2.0 V
					10.0	µA	V_{DD} = V_M = 5.25 V
IPL	11, 12	Pull Up Current	–100		0	µA	
IDL	15	Leak Current			10.0	µA	V_{DD} = V_M = 5.25 V
CAIN2	1, 2	Analog Input Cap.			10	pF	at 1 MHz Vbias = 0
CDIN	8, 9, 10,	Input Capacitance			10	pF	at 1 MHz Vbias = 0
	11, 12, 14						
ROUTA	5	AOUT Resistance		1	10	Ω	
ROUTG	3	GA2 Resistance			30	Ω	Note 1
VGSW	3	GA2 Output Swing	–3.0		3.0	V	R_L = 10 kΩ
VOFFIN	1	Analog Offset Input	–500		500	mV	Note 1
VOFFG	3	GA2 Offset Output	–50		50	mV	Note 1
VOFFA	5	AOUT Offset Output	–50		50	mV	PCMIN = +0 – Code
CDOUT	15	PCMOUT Capacitance			15.0	pF	at 1 MHz Vbias = 0 V
V_{OL}	15	PCMOUT Low Voltage			0.4	V	R_L = 500 Ω
							+I_{OL} = 0.8 mA
V_{OH}	15	PCMOUT High Voltage	V_{CC}–0.3			V	I_{OH} = –150 µA
V_{IH}	8, 10, 11,	Digital Input High	2.0			V	
	9, 12, 14	Voltage					
V_{IL}	8, 10, 11,	Digital Input Low Voltage			0.8	V	
	9, 12, 14						

Note 1) Analog Input Amplifier Gain = 0 dB (Ga1 is connected to GA2)

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Dynamic-Characteristics (V_{DD} = 5 ± 0.25 V, V_{SS} = –5 ± 0.25 V, V_{CC} = 5 ± 0.25 V, Ta = 0 to +70°C)

Sym.	Descriptions	Min	Typ	Max	Unit	Note
FS	Synchronization Rate		8		kHz	
FC	PCM Bit Clock Rate	64		2048	kHz	
twc	Clock Pulse Width	200			ns	
twsh	SYNC Pulse High Width	200			ns	
twsl	SYNC Pulse Low Width	8			µs	
tr	Logic Input Rise Time	5		50	ns	
tf	Logic Input Fall Time	5		50	ns	
tbcs	Previous Clock To SYNC Delay	40			ns	Note 1
tcs	Clock To SYNC Delay			100	ns	Note 1, 3
tcd1	Clock To PCM MSB Delay			170	ns	Note 1, 2, 4
tsd	SYNC To PCM MSB Delay			170	ns	Note 1, 2, 4
tcd	Clock To PCMOUT Delay			180	ns	Note 1, 2, 5
tsu	PCMIN Setup Time	65			ns	Note 1
thd	PCMIN Hold Time	120			ns	Note 1
tbs	PD (bit-steal) Setup	200			ns	Note 1, 6
tbh	PD (bit-steal) Hold	200			ns	Note 1, 6

Notes
1) tr, tf of digital input or clock is assumed 5ns for timing measurement.
2) PCMOUT Load Condition: 500 Ω+165 pF+ two LS-TTL Equivalent (I_{IL} = 0.8 mA, I_{IH} = –150 µA) Threshold Level (V_{OH} = 2.4 V, V_{OL} = 0.4 V)
3) Positive value shows SYNC delay from CLOCK.
4) tcd1, tsd are specified by CLOCK or SYNC which has slower rise time.
5) tcd specification is valid for the data except MSB.
6) Applicable HD44238P

System Related Characteristics (V_{DD} = 5 ± 0.25 V, V_{SS} = –5 ± 0.25 V, V_{CC} = 5 ± 0.25 V, Ta = 0 to +70°C, Input Amplifier Gain = 0 dB, GA2 Load = 10 kΩ, Aout Load = 600 Ω, Synchronous operation. fc (PCM Bit Clock) = 2048 kHz)

For HD44237P

Sym.	Descriptions	Test Conditions		Min	Typ	Max	Unit	Note
SDA	Signal to Dist. (A to A)	820 Hz tone	–45 dBm0	25			dB	p-wgt
			–40	30			dB	
			–30 to +3	35			dB	
SNA	Signal to Dist. (A to A)	Noise	–55 dBm0	14			dB	
			–40	29			dB	
			–34	34			dB	
			–27 to –6	36			dB	
			–3	28			dB	
SDX	Signal to Dist. (A to D)	820 Hz tone	–45 dBm0	26			dB	p-wgt
			–40	31			dB	
			–30 to +3	36			dB	
SNX	Signal to Dist. (A to D)	Noise	–55 dBm0	15			dB	
			–40	30			dB	
			–34	35			dB	
			–27 to –6	37			dB	
SDR	Signal to Dist. (D to A)	820 Hz tone	–45 dBm0	26			dB	p-wgt
			–40	31			dB	
			–30 to +3	36			dB	

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Sym.	Descriptions	Test Conditions		Min	Typ	Max	Unit	Note
SNR	Signal to Dist (D to A)	Noise		–55 dBm0	15			dB
			–40	30			dB	
			–34	35			dB	
			–27 to –6	37			dB	
GTA	Gain Track (A to A)	820 Hz tone	–55 to –50 dBm0	–1.0		1.0	dB	
		Relative to	–50 to –40	–0.5		0.5	dB	
		–10 dBm0	–40 to +3	–0.3		0.3	dB	
GNA	Gain Track (A to A)	Noise	–60 to –55 dBm0	–0.8		0.8	dB	
		Relative to	–55 to –10	–0.4		0.4	dB	
		–10 dBm0						
GTX	Gain Track (A to D)	820 Hz tone	–55 to –50	–0.8		0.8	dB	
		Relative to	–50 to –40	–0.4		0.4	dB	
		–10 dBm0	–40 to +3 dBm0	–0.2		0.2	dB	
GNX	Gain Track (A to D)	Noise	–60 to –55 dBm0	–0.6		0.6	dB	
		Relative to	–55 to –40	–0.4		0.4	dB	
		–10 dBm0	–40 to –10	–0.2		0.2	dB	
GTR	Gain Track (D to A)	820 Hz tone	–55 to –50	–0.8		0.8	dB	
		Relative to	–50 to –40	–0.4		0.4	dB	
		–10 dBm0	–40 to +3 dBm0	–0.2		0.2	dB	
GNR	Gain Track (D to A)	Noise	–60 to –55 dBm0	–0.4		0.4	dB	
		Relative to	–55 to –10	–0.2		0.2	dB	
		–10 dBm0						
FRX	Freq.Response (A to D) (Loss)	Relative to 820 Hz 0 dBm0	0.06 kHz	24			dB	
			0.2	0		2.0		
			0.3 to 3	–0.15		0.15		
			3.18	–0.15		0.65		
			3.4	0		0.8		
			3.78	6.5				
FRR	Freq.Response (D to A) (Loss)	Relative to 820 Hz 0 dBm0	0 to 3 kHz	–0.15		0.15	dB	
			3.18	–0.15		0.65		
			3.4	0		0.8		
			3.78	6.5				
AIL	Analog Input Level	820 Hz 0 dBm0	25°C nom.P.S.	1.217	1.231	1.246	Vrms	
AOL	Analog Output Level	820 Hz 0 dBm0	25°C nom.P.S.	1.217	1.231	1.246	Vrms	
ICNA	Idle Ch. Noise	A to A	AIN = AGND			–78	dBmOP	
ICNX	Idle Ch. Noise	A to D	AIN = AGND			–80	dBmOP	
ICNR	Idle Ch. Noise	D to A	PCMIN = +0–CODE			–80	dBmOP	
XTKA	AIN to AOUT Crosstalk	820 Hz	0 dBm0			–65	dB	
XTKD	PCMIN to PCMOUT	820 Hz	0 dBm0			–65	dB	

5

For HD44238P

Sym	Pin No.	Descriptions		Min	Typ	Max	Unit	Note
SDA	Signal to Dist. (A to A)	1020 Hz tone	–45 dBm0	25			dB	c-wgt
			–40	30			dB	
			–30 to +3	35			dB	
SDX	Signal to Dist. (A to D)	1020Hz tone	–45 dBm0	26			dB	c-wgt
			–40	31			dB	
			–30 to +3	36			dB	
SDR	Signal to Dist. (D to A)	1020 Hz tone	–45 dBm0	26			dB	c-wgt
			–40	31			dB	
			–30 to +3	36			dB	
GTA	Gain Tracking (A to A)	1020 Hz tone Relative to 10 dBm0	–55 to –50 dBm0	–1.0		1.0	dB	
			–50 to –40	–0.5		0.5	dB	
			–40 to +3	–0.3		0.3	dB	
GTX	Gain Tracking (A to D)	1020 Hz tone Relative to –10 dBm0	–55 to –50	–0.8		0.8	dB	
			–50 to –40	–0.4		0.4	dB	
			–40 to +3 dBm0	–0.2		0.2	dB	
GTR	Gain Tracking (D to A)	1020 Hz tone Relative to –10 dBm0	–55 to –50	–0.8		0.8	dB	
			–50 to –40	–0.4		0.4	dB	
			–40 to +3 dBm0	–0.2		0.2	dB	
FRX	Freq.Response (A to D) (Loss)	Relative to 1020 Hz 0 dBm0	0.06 kHz	24			dB	
			0.2	0		2.0	dB	
			0.3 to 3	–0.15		0.15	dB	
			3.18	–0.15		0.65	dB	
			3.4	0		0.8	dB	
			3.78	6.5			dB	
FRR	Freq.Response (D to A) (Loss)	Relative to 1020 Hz 0 dBm0	0 to 3 kHz	–0.15		0.15	dB	
			3.18	–0.15		0.65	dB	
			3.4	0		0.8	dB	
			3.78	6.5			dB	
AIL	Analog Input Level	1020 Hz 0 dBm0	25°C nom. P.S.	1.213	1.227	1.241	Vrms	
AOL	Analog Output Level	1020 Hz 0 dBm0	25°C nom. P.S.	1.213	1.227	1.241	Vrms	
ICNA	Idle Ch. Noise	A to A	AIN = AGND			16	dBrnCO	
ICNX	Idle Ch. Noise	A to D	AIN = AGND			16	dBrnCO	
ICNR	Idle Ch. Noise	D to A	PCMIN = +0–Code			10	dBrnCO	
XTKA	AIN to AOUT Crosstalk	1020Hz 0 dBm0				–65	dB	
XTKD	PCMIN to PCMOUT	1020 Hz 0 dBm0				–65	dB	

For HD44237P, HD44238P

Sym.	Descriptions	Test Conditions		Min	Typ	Max	Unit	Note
AT	AIL, AOL Variation with temp.	Relative to 25°C nominal P.S.			±20		ppm/°C	
AP	AIL,AOL Variation with P.S.	25°C, Supplies ± 5%			± 0.01		dB	
ALS	GAIN Variation over Temp. P.S.	A to D D to A	Initial	–0.2		–0.2	dB	Note 1)
AIP	Peak Analog Input			3.0			V	
AOP	Peak Analog Output			2.5			V	
PDL	Propagation Delay	A to A	0 dBmO		450	480	µs	
DD	Delay Distortion	A to A 0 dBmO	0.5 to 0.6 kHz			1.4	ms	
			0.6 to 1.0			0.7		rel. to min. delay
			1.0 to 2.6			0.2		
			2.6 to 2.8			1.4		
PSRR	PSRR	A to A AIN = AGND 0.3 – 50 kHz	V_{DD} Mod. = +5 V + 100 mVop	30			dB	
			Vss Mod. = –5 V + 100 mVop	30				
IM1	Intermodulation	A to A(2a-b) a; 0.47 kHz, –4 dBmO b; 0.32, –4				–38	dB	
IM2	Intermodulation	A to A(a-b) a; 1.02 kHz, –4 dBmO b; 0.05, –23				–52	dB	
ICS	Single Freq.Noise	A to A AIN = AGND	8,16,24, 32,40 kHz			–50	dBmO	
DIS	Discrimination	A to A 0 dBmO	4.6 to 200 kHz	30			dB	

Note 1) Total variation of GAIN including the initial fluctuation temperature variation and power supply dependence (0 to +70°C, V_{DD}/Vss = ± 5 V ± 5%)

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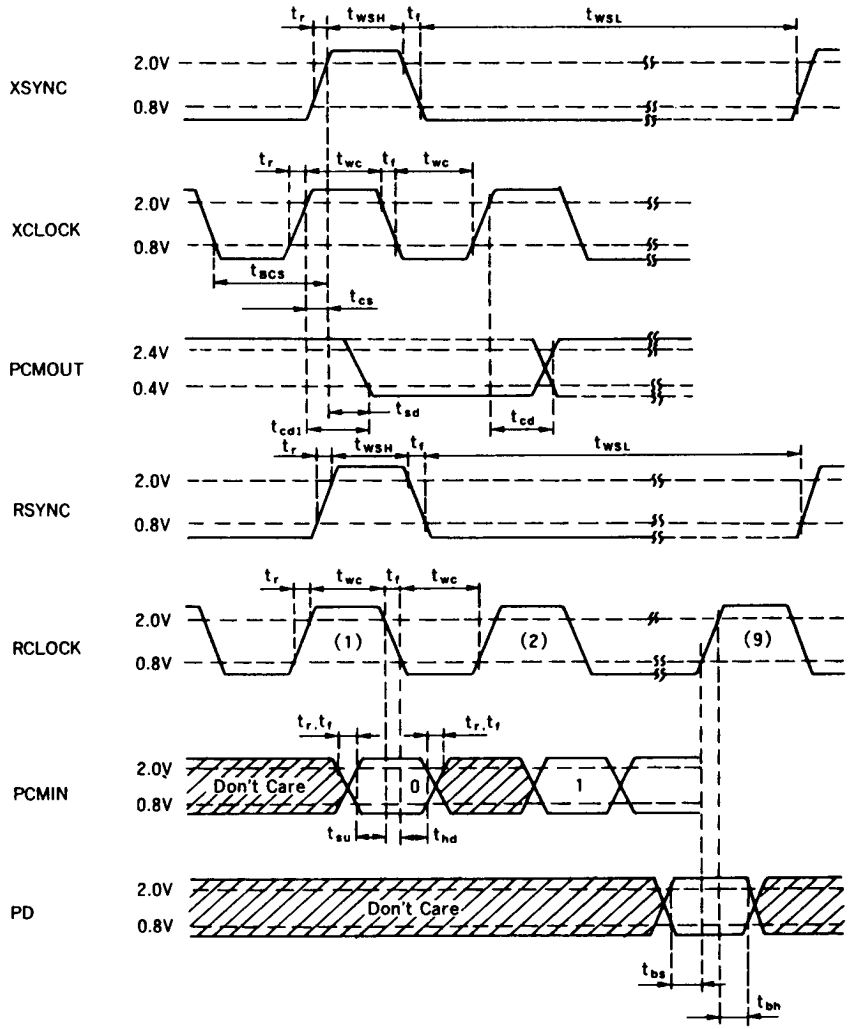
Timing Chart



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