A. HE8P160 Introduction

HE8P160 is a member of 8-bit microcontroller OTP series product developed by King Billion Electronics Ltd. This IC uses OTP (One Time Programming) ROM, which can be written by the OTP writer provided by King Billion. It can provide user with fast verification, pilot-run product, and more versatile application requests. HE8P160 is a super-set of seven ICs, HE82005、HE83000、HE83005、HE83115、HE83116、HE89A21、HE89R21) and internal build in 8 channel 12-bit ADC converter. If user wants to emulate any one of the seven ICs, the OTP EZ-Writer tool will automatically set the hardware resource, such as ROM、RAM size and it is very convenient to use .

This IC has build-in LCD driver which have many configuration and can use Mask Option to select the configuration, such as【128 pixel LCD driver + 16 Bit I/O Port】…【64 pixel LCD driver + 32Bit I/O Port】. Build-in voltage regulator let LCD display stable when external battery voltage drop. The built-in OP operation amplifier can be used with (light、voice、temperature、humility) sensor and used as battery low detection. The 7-bit current-type D/A converter and PWM device provide complete speech output mechanism.

The instruction set of HE8P160 is quite easy to learn and simple to use. Only about thirty instructions with four-type addressing mode are provided. Most of instructions take 3 oscillator clocks (machine cycles). The processing power is enough for most of battery operation system.

B. HE8P160 Features

- Operation Voltage: 2.4V – 5.5V
- System Clock: DC ~ 8MHz @ 5.0V
  DC ~ 4MHz @ 2.4V
- Internal ROM: 64K Bytes (64K Program ROM)
- Internal RAM: 512 Bytes.
- Dual Clock System: Normal (Fast) clock: 32.768K ~ 8MHz
  Slow clock: 32.768 KHz
- Operation Mode: DUAL、FAST、SLOW、IDLE、SLEEP Mode.
- Build-in WDT (WATCH DOG TIMER) to prevent deadlock or abnormal condition.
- 16~32 bit Bi-directional I/O port. Mask Option can select PUSH-PULL or OPEN DRAIN output mode for each I/O pin. The each of I/O PRTD[3:0] has 5 mA sink capability.
- Build-in OP amplifier. This OP operating range between 0 ~ (VDD-1), that is different from previous OP comparator operating range between 0.8~VDD, the user should notice this. Please set the operation range on 0.8 ~ (VDD-1) if users want to design a circuit working both on 8P160 and target IC.
- Build-in 125 KHz, 8-channel 12-bit ADC block.
- Build-in voltage regulator which provide LCD stable operating voltage.
- 4 COM*32 SEG LCD driver which have A, B type. Voltage regulator circuit pleases refer to application circuit. The LCD highest voltage LV3 must less than 9.0 V.
- Contain a 7-bit Current-type D/A converter.

- Provide PWM output device.(Users can select with or without Rate Selection, connect with "VDD+PWM" or "PWMP+PWMN")
- Two external interrupts and three internal timer interrupts.
- Two 16-bit timers and one Time Base timer.
- Instruction set: 32 instructions, 4 addressing mode. 9-bit DATA POINTER for RAM and 16-bit TABLE POINTER for ROM.

C. Mask Option Comparison Table

When user uses KB OTP writer(include application software& hardware) to write data to OTP, user can select specific IC from software application, in the mean time, the KB OTP writer will set all the configuration automatically. The following table describes the configuration relative setting, if users want to use HE8P160 full function setting, please reference following setting.

NAME	Description	82005	83000	83005	83115	83116	89A21	89R21
MO_LDVINC	0: TP not changed at LDV 1: TP++ at LDV	User	1	1	1	1	1	1
MO_FOSCE	0: internal fast OSC 1: external fast OSC, use it now	1	User	User	User	User	User	User
MO_FXTAL	0: R/C osc. For fast clock 1: X'tal osc. For fast clock	User	User	User	User	User	User	User
MO_FRCI_S[2:0]	000: RFRC_I ~= 500k 001: RFRC_I ~= 1M 010: RFRC_I ~= 1.5M 011: RFRC_I ~= 2M 100: RFRC_I ~= 2.5M 101: RFRC_I ~= 3M 110: RFRC_I ~= 3.5M 111: RFRC_I ~= 4M	000: not exist	User	User	User	User	User	User
MO_SXTAL	0: R/C osc. For 32k clock 1: X'tal osc. For 32k clock	0: not exist	User	User	User	User	User	User
MO_FCK/SCKN	00: slow clock only 01: illegal 10: dual clock 11: fast clock only	11	User	User	User	User	User	User
MO_WDTE	0: WDT disable 1: WDT enable	0	User	User	User	User	User	User
MO_CPP[7:4]	0: open-drain output 1: push-pull output	1	1	User	1	User	User	User
MO_CPP[3:0]	0: open-drain output 1: push-pull output	1	User	User	User	User	User	User
MO_DPP[7:0]	0: open-drain output 1: push-pull output	User	User	User	User	User	User	User
MO_14PP[7:0]	0: open-drain output 1: push-pull output	1	1	1	User	1	User	User
MO_15PP[7:0]	0: open-drain output 1: push-pull output	1	1	1	1	1	User	User
MO_LIO14[7:0]	0: IO pin 1: LCD pin	0	0	0	User	1	User	User

NAME	Description	82005	83000	83005	83115	83116	89A21	89R21
MO_LIO15[7:0]	0: IO pin 1: LCD pin	0	0	0	0	1	User	User
MO_DTMFSCK	0: DTMF clock source 3.58M Hz 1: DTMF clock source 32768 Hz	0	0	0	0	0	User	User
MO_LVRG	0: LCD regulator disable 1: LCD regulator enable	0	0	0	0	0	0	User
MO_PRTC_ADC[7:0]	0: I/O pin 1: ADC input	0	0	0	0	0	0	0
MO_PRTD_HIC[3:0]	0: 2mA IoL 1: 5mA IoL	0	0	0	0	0	0	0
MO_PROTECTN	0: OTP read protect 1: OTP not protect	User	User	User	User	User	User	User
MO_ROM[1:0]	00: ROM 4k byte 01: ROM 8k byte 10: ROM 16k byte 11: ROM 64k byte	11	00	11	11	11	10	10
MO_RAM[1:0]	00: RAM 64 byte 01: RAM 128 byte 10: RAM 256 byte 11: RAM 512 byte	01	00	01	10	10	11	11
MO_TC2	0: TC2 not exist 1: TC2 exist	0	1	1	1	1	1	1
MO_TB	0: TB not exist 1: TB exist	0	0	0	0	0	1	1
MO_PRT0C[1:0]	00: prt0C not exist 01: only prt0C[3:0] exist 10: only prt0C[7:4] exist 11: prt0C exist	00	01	11	01	11	11	11
MO_PRT14	0: prt14 not exist 1: prt14 exist	0	0	0	1	0	1	1
MO_PRT15	0: prt15 not exist 1: prt15 exist	0	0	0	0	0	1	1
MO_PRT14_SS	0: prt14[7:0]=SEG[19:12] 1: prt14[7:0]=SEG[23:16]	0	0	0	0	1	1	1
MO_LCD	0: LCD not exist 1: LCD exist	0	0	0	1	1	1	1
MO_PWM[1:0]	00: PWM not exist 01: PWM logic 10: PWM1 logic 11: PWM not exist	10	00	10	10	01	00	00
MO_PMD	0: PWMP/PWMN output 1: PWM/GND_PWM output	1	0	0	0	0	0	0
MO_VO	0: DAC not exist 1: DAC exist	1	0	1	1	1	0	0
MO_OPAMP	0: OP Amp. not exist 1: OP Amp. exist	0	1	1	1	1	0	0
MO_DTMF	0: DTMF not exist 1: DTMF exist	0	0	0	0	0	1	1

D. Pin Description

Pin#	Pin Name	I/O	Function	Description
52, 51	**FXI, FXO**	B/O	External fast clock pin. Connecting to crystal or RC to generate 32.768 kHz ~ 8MHz frequency.	Mask option setting： MO_FCK/SCKN= 00：Slow Clock only 01：Illegal 10：Dual Clock 11：Fast Clock only MO_FOSCE = 0：Internal fast osc. = 1：External fast osc. MO_FXTAL = 0：RC osc. for fast clock = 1：X'tal osc. for fast clock MO_SXTAL = 0：RC for 32768 Hz clock = 1：X'tal for 32768 Hz clock Use OP1 and OP2 to switch among different operation mode (NORMAL, SLOW, IDEL and SLEEP). In Dual Clock mode, the main system clock is still the Fast Clock. The 32768 Hz clock is for LCD and Timer 1 only.
55, 54	**SXI, SXO**	I/O	External slow clock pin. Connecting with 32768 Hz crystal or resistor as slow clock and providing clock source for LCD display, TIMER1, Time-Base and other internal blocks.	
50	**RSTP_N**	I	System Reset.	Level trigger, active low. Except for using this pin, using mask option (MO_PORE=1) could enable IC build-in Power-on reset circuit. Besides, MO_WDTE can set Watch Dog Timer： MO_WDTE=0：Disable Watch Dog Timer =1：Enable Watch Dog Timer
53	**TSTP_P**	I	Test Pin, active high.	Please bond this pin and add a test point on PCB for debugging. But for improving ESD, please connect this point with zero Ohm resistor to GND.
82, 83 1..6	**PRTC[7:0] /ADC[7:0];**	B	Port C bi-directional I/O pin，total 8 pin or **ADC[7:0] can be used as** 8-channel ADC Data Input Pin.	Mask options： MO_CPP[7..0]=1 ~ Push-pull. = 0 ~ Open-drain. When use them as input (No tri-state structure), it must Output "1" before reading.
70..77	**PRTD[7:0]**	B	8-pin bi-directional I/O port. PRTD[7..2] as wake-up pin. PRTD[7..6] as external interrupt pin.	Mask options： MO_DPP[7..0]=1 ~ Push-pull. = 0 ~ Open-drain. When use them as input (No tri-state structure), it must Output "1" before reading.
16..23	**PRT14[7:0]/ SEG[23:16]**	B/O	8-pin bi-directional I/O port that is shared with LCD segment pin.	Mask options： MO_LIO14[7..0]=1 ~ LCD Pin. = 0 ~ I/O Pin. MO_14PP[7..0]=1 ~ Push-pull. =0 ~ Open-drain. When use them as input (No tri-state structure), it must Output "1" before reading.
8..15	**PRT15[7:0]/ SEG[31:24]**	B/O	8-pin bi-directional I/O port that is shared with LCD segment pin.	Mask options： MO_LIO15[7..0]=1 ~ LCD Pin. =0 ~ I/O Pin. MO_15PP[7..0]=1 ~ Push-pull. =0 ~ Open-drain. Output must be "1" before reading whenever uses them as input (No tri-state structure).
40..43	**COM[3:0]**	O	LCD COM Output	Please reference LCD and RAM map.
24..31	**SEG[15:8]/ D[7:0]**	O	LCD segment Output/ OTP writing pin	These are LCD segment and OTP Writer shared pin, User Must refer standard interface to arrange these pins on PCB board, let KB writer can write data to OTP. These pins are LCD segment pin on normal mode.
32	**SEG[7]/SDO**	O	Segment/ OTP writing pin	
33	**SEG[6]/SDI**	O	Segment/ OTP writing pin	

Pin#	Pin Name	I/O	Function	Description
34	**SEG[5]/SCLK**	O	Segment/ OTP writing pin	
35	**SEG[4]/D_CN**	O	Segment/ OTP writing pin	
36	**SEG[3]/R_WN**	O	Segment/ OTP writing pin	
37	**SEG[2]/P_SN**	O	Segment/ OTP writing pin	
38, 39	**SEG[1:0]**	O	LCD segment Output	
45	**LC2**	B	Charge Pump Switch 1	
44	**LC1**	B	Charge Pump Switch 2	
48	**L V3**	B	Charge Pump V3	Refer to application circuit.
47	**L V2**	B	Charge Pump V2	
46	**L V1**	B	Charge Pump V1	
63	**PWM**	O	The PWM output can drive speaker or buzzer directly.	Set Bit2 (PWM=1) of VOC register to turn on PWM.
65	**PWMP**	O	The PWM positive output can drive speaker or buzzer directly.	Set Bit2 (PWM=1) of VOC register to turn on PWM.
64	**PWMN**	O	The PWM negative output can drive speaker or buzzer directly.	S Set Bit2 (PWM=1) of VOC register to turn on PWM.
69	**VO**	O	D/A voice output.	Set Bit1 (DA=1) of VOC register to turn on VO.
67	**OPIN**	I	Negative input of OP comparator	Set the bit0 (OP=1) of VOC register to turn on OP comparator. The operating range between 0 ~ (VDD-1).
68	**OPIP**	I	Positive input of OP comparator	
66	**OPO**	O	OPAMP output pin	
59	**DTMFO**	O	DTMF Output	Through Port12，can turn on/off **DTMF & write data**. Use Mask Option MO_DTMFSCK set clock source： MO_DTMFSCK=0, Clock Source=3.579545 MHz =1；Clock Source=32768 Hz
58	**MUTE**	O	MUTE Output for Dialer	**MUTE** can be turned on/off by Port12.
60	**SDO**	O	SDO for Dialer Application	**SDO & write data** can be turned on/off by Port12.
61	**KEYTONE**	O	1024 Hz 50% Duty square wave	**KEYTONE** can be turned on/off by Port12.
57	**LOADER**	I	Define Loader Mode	Used for program download
78	**VREFP**	I	ADC positive voltage reference	Tie this pin to reference Input: 1V to VDDA
79	**VREFN**	I	ADC negative voltage reference	Tie this pin to VSSA
56	**VDD**	P	Digital Positive Power	Adding 0.1 µF capacitor as by-pass capacitor on each set is necessary. VDDA and VSSA must always be tied to high and low.
49	**GND**	P	Digital Power Ground	
81	**VDDA**	P	Analog Positive Power	
80	**VSSA**	P	Analog Power Ground	
7	**VPP**	P	OTP high voltage power	
62	**GND_PWM**	P	Dedicated GND for PWM	

E. LCD RAM Map

Page 0:

F0H	SEG1	SEG0	F8H	SEG17	SEG16
	COM[3:0]	COM[3:0]		COM[3:0]	COM[3:0]
F1H	SEG3	SEG2	F9H	SEG19	SEG18
	COM[3:0]	COM[3:0]		COM[3:0]	COM[3:0]
F2H	SEG5	SEG4	FAH	SEG21	SEG20
	COM[3:0]	COM[3:0]		COM[3:0]	COM[3:0]
F3H	SEG7	SEG6	FBH	SEG23	SEG22
	COM[3:0]	COM[3:0]		COM[3:0]	COM[3:0]
F4H	SEG9	SEG8	FCH	SEG25	SEG24
	COM[3:0]	COM[3:0]		COM[3:0]	COM[3:0]
F5H	SEG11	SEG10	FDH	SEG27	SEG26
	COM[3:0]	COM[3:0]		COM[3:0]	COM[3:0]
F6H	SEG13	SEG12	FEH	SEG29	SEG28
	COM[3:0]	COM[3:0]		COM[3:0]	COM[3:0]
F7H	SEG15	SEG14	FFH	SEG31	SEG30
	COM[3:0]	COM[3:0]		COM[3:0]	COM[3:0]

F. Build-in 8-channel ADC

HE8P160 built in 8-channel 12-bit ADC with 125 KHz sampling rate are pin-shared with port C, it contain sample and hold circuit. User can set MO_PRTC_ADC [3:0] to select what kind of input. User can set the ADC control register by writing setting to PRTC or obtain the ADC converted data by reading the PRTC, refer to following table for more details; The read data is high byte or low nibble, depends on ADC control register setting. The ADC data register has only one set, so if there is more than one channel application, it should be saved previous ADC sample data, then switch to another channel to sample ADC data again.

When ADC[7]=0, the whole ADC block will turn on. This chip provides two kind of method to start ADC converting which are software interrupt and hardware interrupt (Timer). When ADC[5]=1, the start of covert ADC sample is triggered by rising edge of ADC[6]; the ADC hardware will begin to sample, the translation time must large than 150μs and the user should notice this point, otherwise it will fetch the unstable data. The disadvantage of software trigger is that ADC may produce jitter effect in sample data, such as voice sample, but the advantage of software trigger is that it can process 1 to 8 channel sample data; it is suitable for the application less sensitive on phase jitter issue.

The other way to trigger ADC to convert data is by Timer 1 interrupt; when interrupt happen, the sample data will be sampled and store in ADC data register, user can read back the sampled data. The advantage of using Timer 1 interrupt to trigger ADC is to avoid the phase jitter and calculation the delay sample time.

The ADC[4] bit is used to select the high byte or low nibble of sampled data and ADC[3] is the clock source selection used to select the clock source of ADC which comes from fast clock divided

by 4 or divided by 2. If fast clock is greater than 8 MHz, then set ADC[3]=0, otherwise set ADC[3]=1. The ADC[2:0] is used to select one of the 7 ADC input signal channel, there is only one channel selected at the same time.

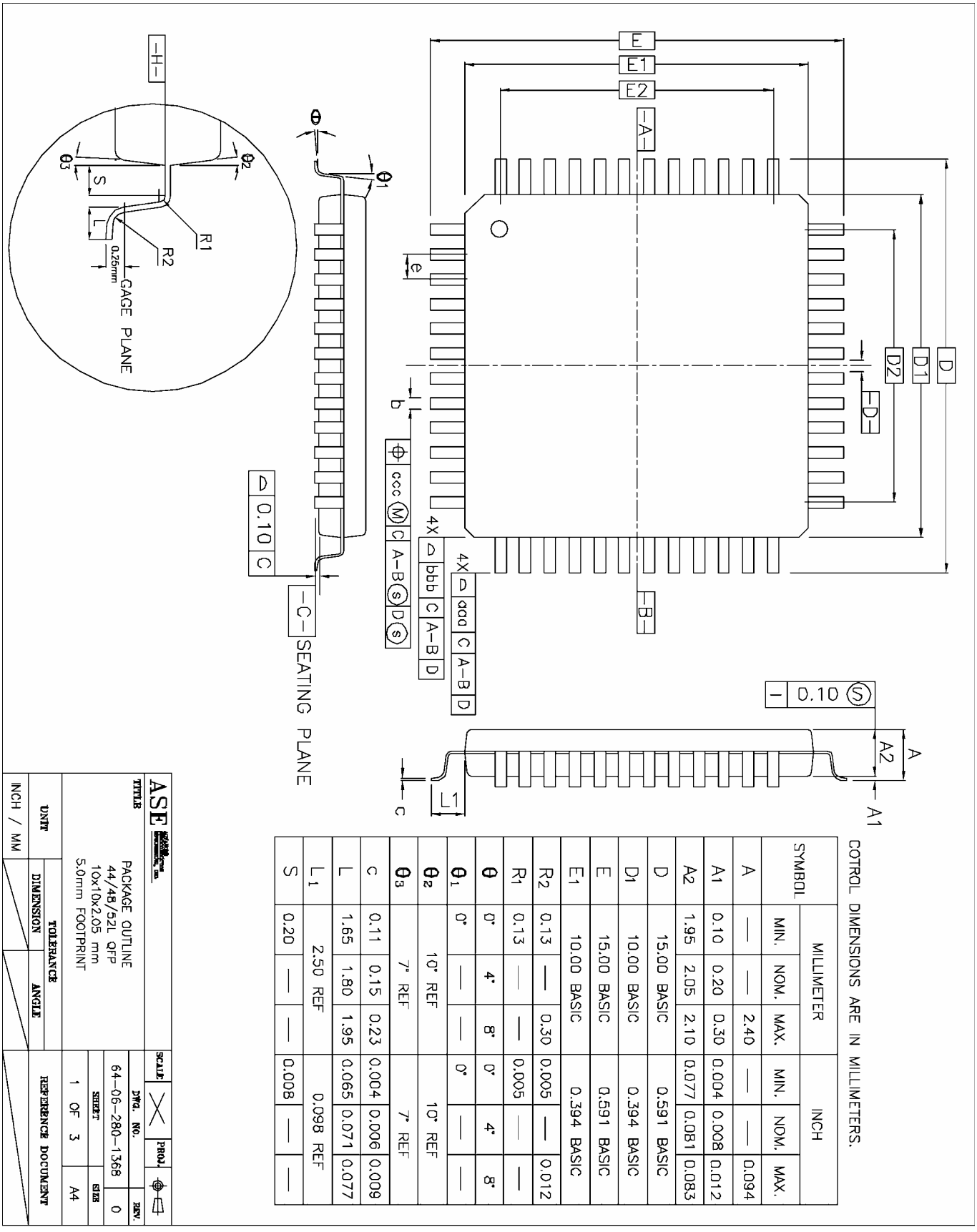
Address	Name	Function	R/W	Width	Reset
0ch: (PRTC)	ADC	ADC control/data register	R/W	8	ZZZZZZZZ
ADC Control Register (Write Bit Field)					
ADC[7]	ENB	0: ADC enable			
		1: ADC disable; Power-down			
ADC[6]	Start	0 -> 1: S/W start a ADC conversion			
ADC[5]	SELTM	0: select T2 interrupt as "start of conversion"			
		1: select ADC[6]'s rising edge as "start of conversion"			
ADC[4]	DATASEL	0: ADC read value = { data[3:0], 0, 0, 0, 0 }, High nibble= data[3:0]; low nibble= ”0000”.			
		1: ADC read value = data[11:4]			
ADC[3]	CLKS	0: ADC Clock= fast clock /4, (Clock > 8MHz)			
		1: ADC Clock = fast clock /2, (Clock < 8MHz)			
ADC[2:0]	CHNL	7~0: select ADC input channel 7~0			
ADC Data Register (Read Bit Field)					
ADC[7:0]		data[11:4], or { data[3:0], 0, 0 ,0, 0 }			

Following program is a ADC sample data example, please reference.

```
Timer2::
        :
; ADC section
; Use ADC channel: PC7

        lda     #00111111b
        sta     PRT17           ; write ADC Control Register
        lda     PRT17           ; Get result[11..4] from Result Register
        sta     MemA            ; Store in “Memory Location A”
        lda     #00101111b
        sta     PRT17           ; write ADC Control Register
        lda     PRT17           ; Get result[3..0] from Result Register
        sta     MemB            ; Store in “Memory Location B”
; END ADC sectio
        :
        reti
```

F. QFP 52 Packages



COTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	2.40	—	—	0.094
A1	0.10	0.20	0.30	0.004	0.008	0.012
A2	1.95	2.05	2.10	0.077	0.081	0.083
D	15.00 BASIC			0.591 BASIC		
D1	10.00 BASIC			0.394 BASIC		
E	15.00 BASIC			0.591 BASIC		
E1	10.00 BASIC			0.394 BASIC		
R2	0.13	—	0.30	0.005	—	0.012
R1	0.13	—	—	0.005	—	—
θ	0°	4°	8°	0°	4°	8°
θ1	0°	—	—	0°	—	—
θ2	10° REF			10° REF		
θ3	7° REF			7° REF		
c	0.11	0.15	0.23	0.004	0.006	0.009
L	1.65	1.80	1.95	0.065	0.071	0.077
L1	2.50 REF			0.098 REF		
S	0.20	—	—	0.008	—	—

ASE

TITLE: PACKAGE OUTLINE 44/48/52L QFP 10x10x2.05 mm 5.0mm FOOTPRINT

UNIT: INCH / MM

TOLERANCE: DIMENSION / ANGLE

REFERENCE DOCUMENT

SCALE: X

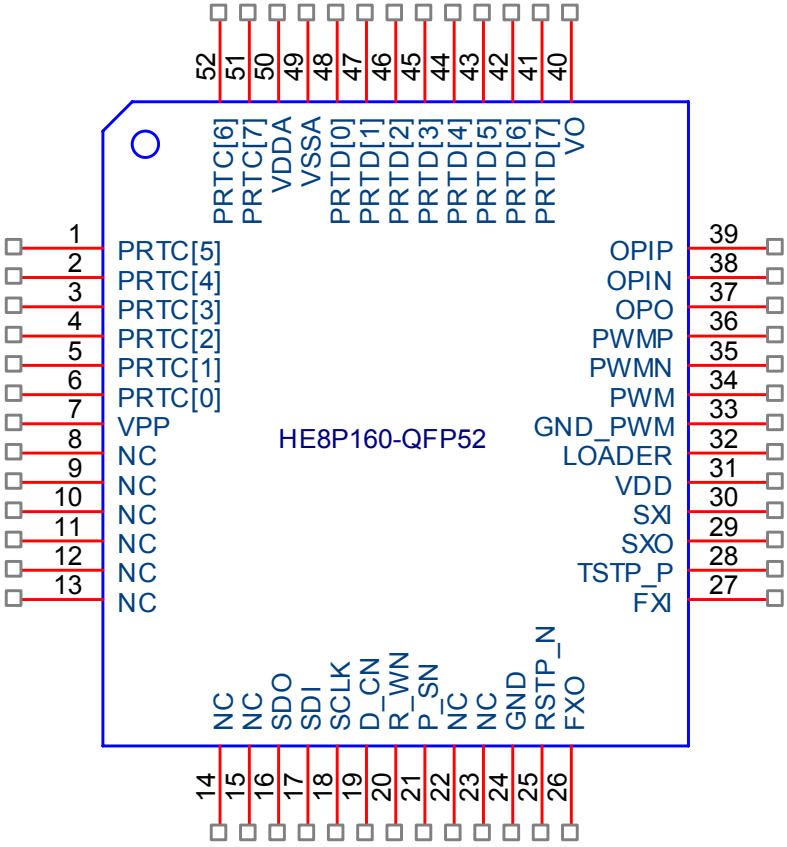
PROJ.:

DWG. NO.: 64-06-280-1368

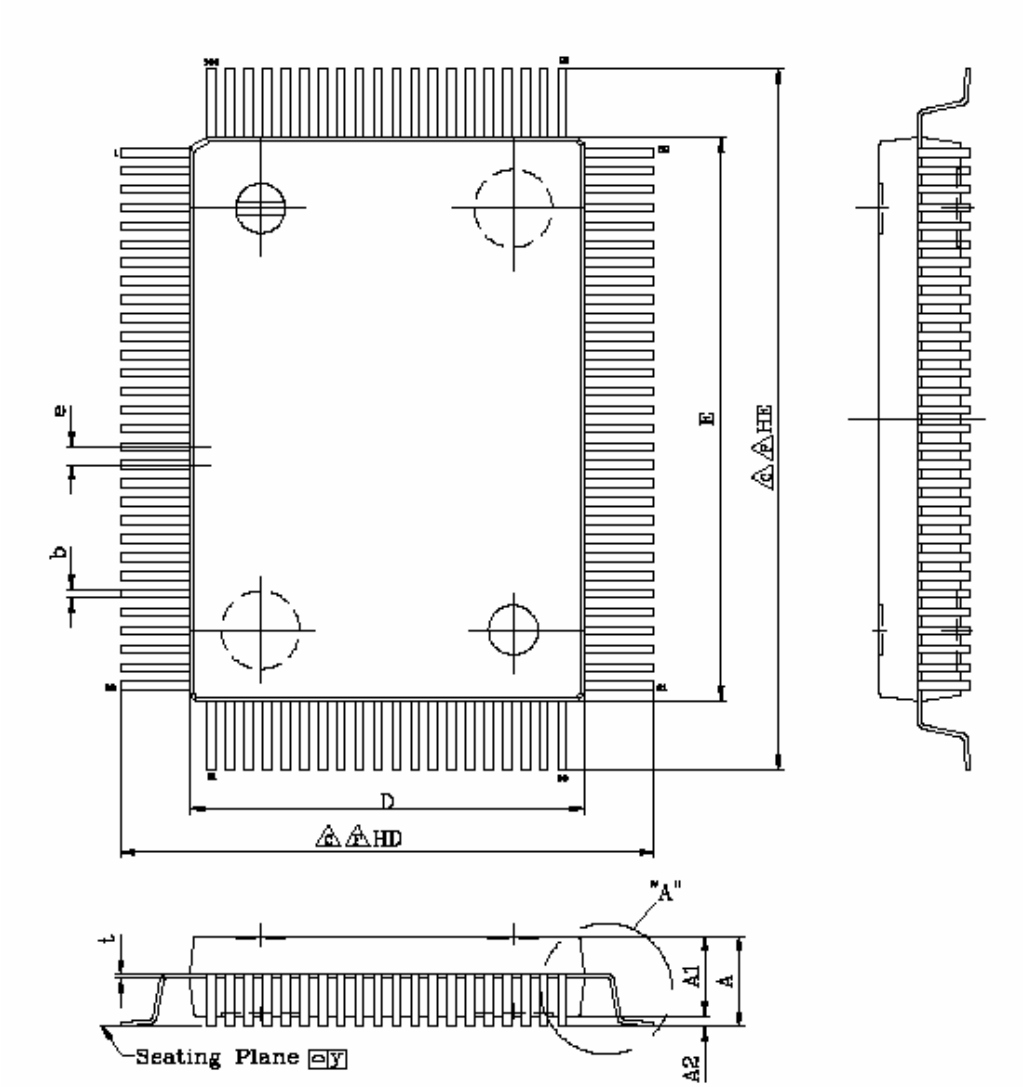
REV.: 0

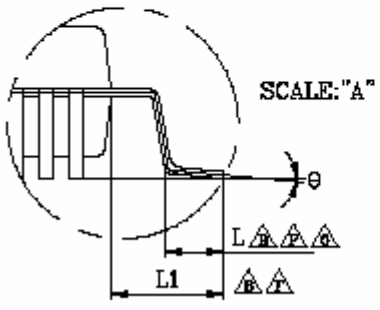
SHEET: 1 OF 3

SIZE: A4

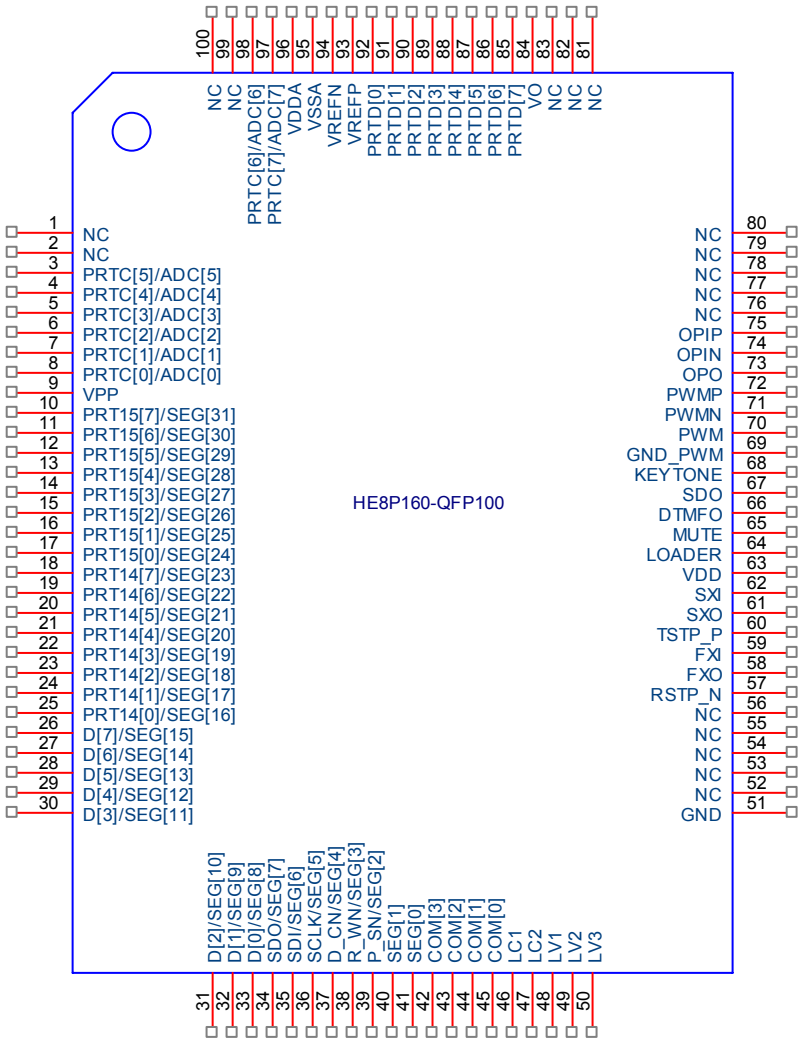

HE8P160-QFP52
1 PRTC[5]
2 PRTC[4]
3 PRTC[3]
4 PRTC[2]
5 PRTC[1]
6 PRTC[0]
7 VPP
8 NC
9 NC
10 NC
11 NC
12 NC
13 NC
14 NC
15 NC
16 SDO
17 SDI
18 SCLK
19 D_CN
20 R_WN
21 P_SN
22 NC
23 NC
24 GND
25 RSTP_N
26 FXO
27 FXI
28 TSTP_P
29 SXO
30 SXI
31 VDD
32 LOADER
33 GND_PWM
34 PWM
35 PWMN
36 PWMP
37 OPO
38 OPIN
39 OPIP
40 VO
41 PRTD[7]
42 PRTD[6]
43 PRTD[5]
44 PRTD[4]
45 PRTD[3]
46 PRTD[2]
47 PRTD[1]
48 PRTD[0]
49 VSSA
50 VDDA
51 PRTC[7]
52 PRTC[6]

G. QFP 100 Packages

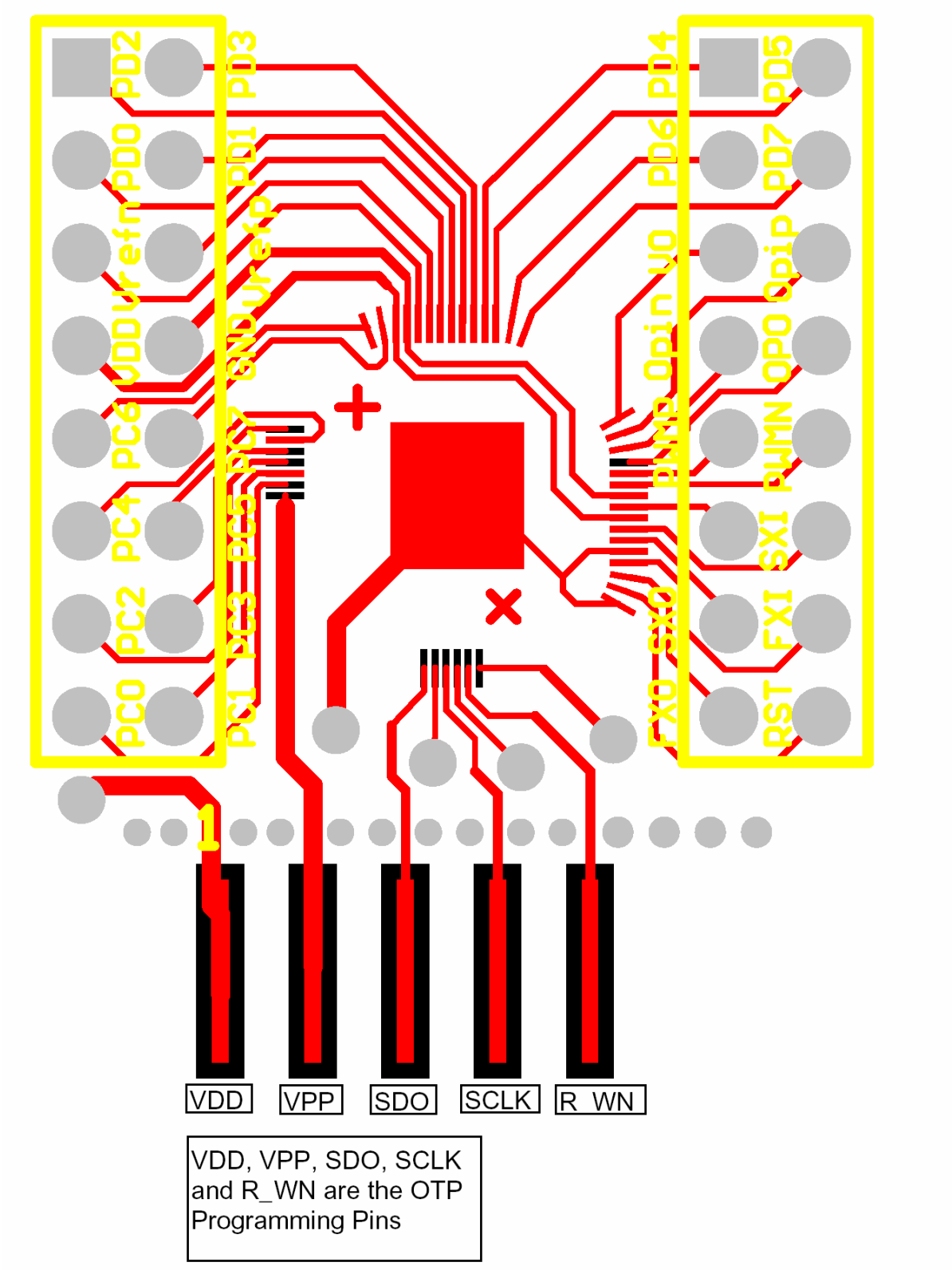




UNIT / SYMBOLS	INCH(REF)	MM(BASE)
A1	0.112±0.005	2.845±0.127
b	0.012(TYP)	0.300(TYP)
D	0.551±0.004	14.000±0.102
E	0.787±0.004	20.000±0.102
e	0.026(BSC)	0.650(BSC)
t	0.006(TYP)	0.150(TYP)
y	0.003 (MAX)	0.076 (MAX)
θ	0°~7°	0°~7°
(OPTION 1)		
A	0.130 (MAX)	3.302 (MAX)
A2	0.004(MIN)	0.102(MIN)
HD	0.740±0.010	18.800±0.254
HE	0.976±0.010	24.800±0.254
L	0.050±0.008	1.260±0.152
L1	0.094±0.006	2.400±0.152


HE8P160-QFP100
1 NC
2 NC
3 PRTC[5]/ADC[5]
4 PRTC[4]/ADC[4]
5 PRTC[3]/ADC[3]
6 PRTC[2]/ADC[2]
7 PRTC[1]/ADC[1]
8 PRTC[0]/ADC[0]
9 VPP
10 PRT15[7]/SEG[31]
11 PRT15[6]/SEG[30]
12 PRT15[5]/SEG[29]
13 PRT15[4]/SEG[28]
14 PRT15[3]/SEG[27]
15 PRT15[2]/SEG[26]
16 PRT15[1]/SEG[25]
17 PRT15[0]/SEG[24]
18 PRT14[7]/SEG[23]
19 PRT14[6]/SEG[22]
20 PRT14[5]/SEG[21]
21 PRT14[4]/SEG[20]
22 PRT14[3]/SEG[19]
23 PRT14[2]/SEG[18]
24 PRT14[1]/SEG[17]
25 PRT14[0]/SEG[16]
26 D[7]/SEG[15]
27 D[6]/SEG[14]
28 D[5]/SEG[13]
29 D[4]/SEG[12]
30 D[3]/SEG[11]
31 D[2]/SEG[10]
32 D[1]/SEG[9]
33 D[0]/SEG[8]
34 SDO/SEG[7]
35 SDI/SEG[6]
36 SCLK/SEG[5]
37 D_CN/SEG[4]
38 R_WN/SEG[3]
39 P_SN/SEG[2]
40 SEG[1]
41 SEG[0]
42 COM[3]
43 COM[2]
44 COM[1]
45 COM[0]
46 LC1
47 LC2
48 LV1
49 LV2
50 LV3
51 GND
52 NC
53 NC
54 NC
55 NC
56 NC
57 RSTP_N
58 FXO
59 FXI
60 TSTP_P
61 SXO
62 SXI
63 VDD
64 LOADER
65 MUTE
66 DTMFO
67 SDO
68 KEYTONE
69 GND_PWM
70 PWM
71 PWMN
72 PWMP
73 OPO
74 OPIN
75 OPIP
76 NC
77 NC
78 NC
79 NC
80 NC
81 NC
82 NC
83 VO
84 PRTD[7]
85 PRTD[6]
86 PRTD[5]
87 PRTD[4]
88 PRTD[3]
89 PRTD[2]
90 PRTD[1]
91 PRTD[0]
92 VREFP
93 VREFN
94 VSSA
95 VDDA
96 PRTC[7]/ADC[7]
97 PRTC[6]/ADC[6]
98 NC
99 NC
100

H.32-Pins COB Package



I. DC/AC Characteristics

Absolute Maximum Rating

Item	Symbol	Rating	Condition
Supply Voltage	V_{dd}	-0.5V ~ 8V	
Input Voltage	V_{in}	-0.5V ~ V_{DD} +0.5V	
Output Voltage	V_o	-0.5V ~ V_{DD} +0.5V	
Operating Temperature	T_{op}	0℃ ~ 70℃	
Storage Temperature	T_{st}	-50℃ ~ 100℃	

Recommended Operating Conditions

Item	Symbol	Rating	Condition
Supply Voltage	V_{dd}	2.4V ~ 5.5V	
Input Voltage	V_{ih}	0.9 V_{dd} ~ V_{dd}	
	V_{il}	0.0V ~ 0.1V_{dd}	
Operating Frequency	Fmax.	8MHz	V_{DD} =5.0V
		4MHz	V_{DD} =2.4V
Operating Temperature	T_{op}	0^0C ~ 70^0C	
Storage Temperature	T_{st}	-50^0C ~ 100^0C	

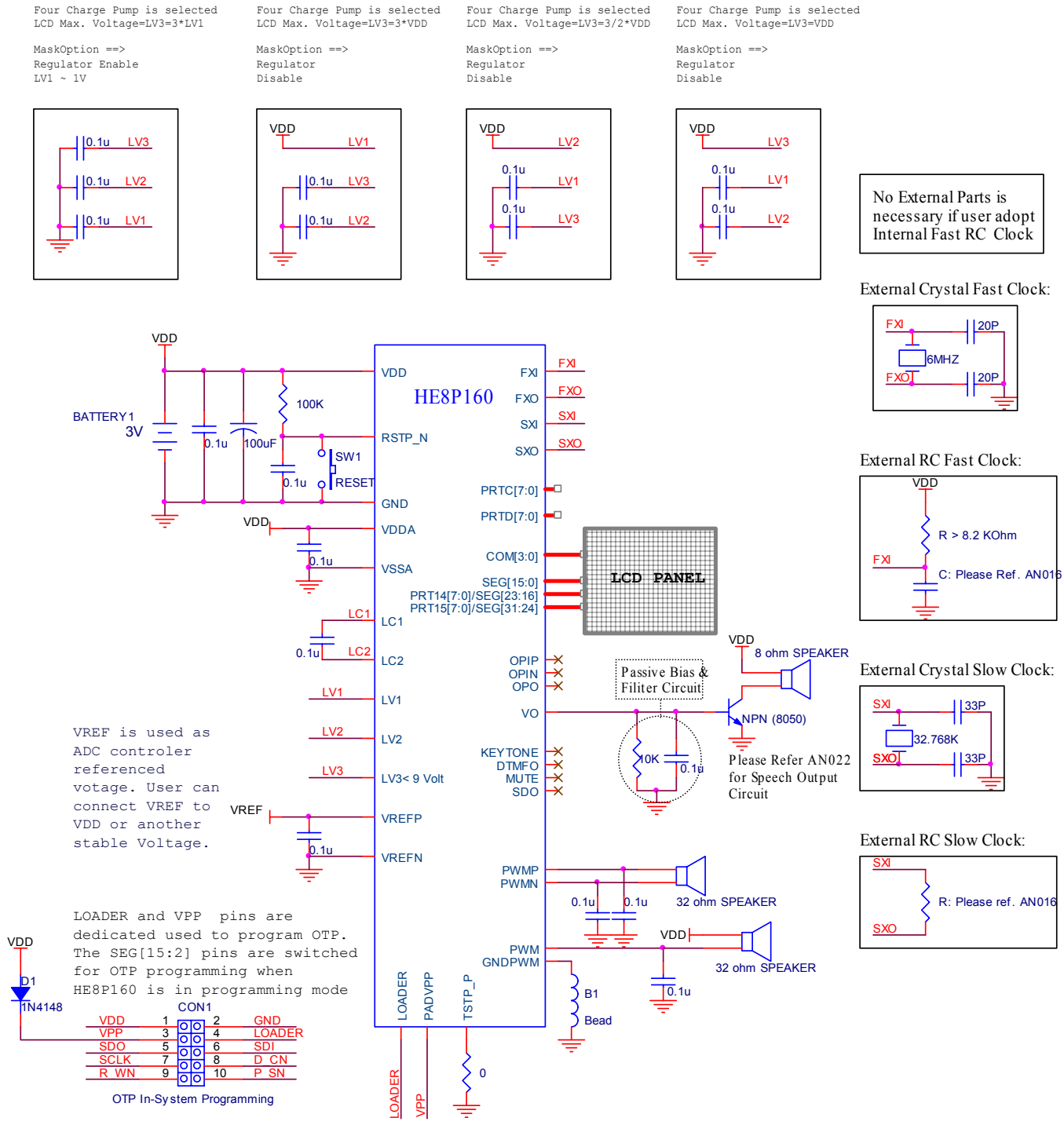
Testing Condition: TEMP. =25℃, V_{DD} =3V±10%, GND=0V

	Parameter		CONDITION	MIN	TYP	MAX	UNIT
I_{Fast}	NORMAL Mode Current	System	4M ext. crystal		1.90	2.0	mA
I_{Slow}	SLOW Mode Current	System	32.768KHz X'tal LCD Disable		50	60	μA
I_{Idle}	IDLE Mode Current	System	32.768KHz X'tal LCD Disable		12	15	μA
I_{LCD}	Extra Current if LCD ON	System	LCD Enable				μA
I_{Sleep}	Sleep Mode Current	System			2.0	3.0	μA
I_{PWM}	PWM Output Current	PWMP, PWMN*2	With 32Ω Loading	10	14		mA
			With 64Ω Loading	6	8		mA
			With 100Ω Loading	4	5		mA
I_{oVO}	DAC Output Current	VO	V_{DD}=3V;VO=0~2V,Data=7F	2.5	3		mA
V_{iH}	Input High Voltage	I/O pins		0.8 V_{DD}			V
V_{iL}	Input Low Voltage	I/O pins				0.2 V_{DD}	V
V_{hys}	Input Hysteresis Width	I/O, RSTP_N	Threshold=2/3V_{DD}(input from low to high) Threshold=1/3V_{DD}(input from high to low)		1/3 V_{DD}		V
I_{oH}	Output Drive Current	I/O pull-high*1	V_{oL}=2.0V	50			μA
I_{oL_1}	Output Sink Current	I/O pull-low*1	V_{oL}=0.4V	1.0			mA
I_{oL_2}	Output Sink Current	PRTD[3:0]	V_{oL}=0.4V	5.0			mA
I_{iL_1}	Input Low Current	RSTP_N	V_{iL}=GND, pull high Internally		20		μA
I_{iL_2}	Input Low Current	I/O	V_{iL}=GND, if pull high Internally by user		100		μA

Note: *1: Drive Current Specification ➔ for Push-Pull I/O port only
Sink Current Specification ➔ for both Push-Pull and Open-Drain I/O port.
*2: This Spec. bases on one driver only. There are five build-in drivers actually, so user can multiply the number of driver to obtain the necessary driver current to drive the speak.
(I_{PWM} * N; N=0, 1, 2, 3, 4, 5)

J. Application Circuit

About 82005、83000、83005、83115、83116、89A21、89R21 and general HE80000 series application, please refer individual data sheet. The following circuit is focus on ADC and Writer application.



Writer Mode Connection Pins Definition:

Pin Number	HE8P160 Pin Name	Writer Mode Pin Name
24	SEG[15]	Data[7]
25	SEG[14]	Data[6]
26	SEG[13]	Data[5]
27	SEG[12]	Data[4]
28	SEG[11]	Data[3]
29	SEG[10]	Data[2]
30	SEG[9]	Data[1]
31	SEG[8]	Data[0]
32	SEG[7]	SDO
33	SEG[6]	SDI
34	SEG[5]	SCLK
35	SEG[4]	D_CN
36	SEG[3]	R_WN
37	SEG[2]	P_SN

K. Updated Record

Version	Date	Section	Original Content	New Content
V1.1	Feb 7, 2002	F		ADC Software Conversion is not in pilot sample. Only T2 conversion in pilot version.
V1.11	Mar 7,2002	B	OP Comparator	OP Operating Amplifier …Operating range…
		D		VDDA tie high, VSSA tie low
V1.12	Mar 25, 2002	F. example	00110111b	00101111b
V1.13	Oct. 03, 2002	J		Add QFP100 Package Spec.
V1.2	Dec. 10, 2002	I		Add QFP52 Package Spec.
V1.2	Dec. 10, 2002	I		Add QFP52 Package Spec.
V1.3	Jan. 03, 2003	L		Power consumption error (slow mode current)