HARRIS

HS-CXXXXRH

T-42-41

CMOS Cell Library
Radiation Hardened Standard Cell

Features

- Low Power - CMOS Technology
- Single 5 Volt Supply
- Guaranteed Hardened Against Radiation
  - Total Dose: ..... $>2 \times 10^5$ Rad-Si
  - Data Upset:..... $>1 \times 10^9$ Rad-Si/sec
  - Latch-Up Free to:.....$>2 \times 10^{12}$ Rad-Si/sec
  - Functional After 10^6 Total Dose Radiation
- Military Temperature Range
- Proven Reliable and Manufacturable Processes
- CMOS and TTL Compatible Inputs and Outputs
- Large Library of SSI Primitive Cells
- 74XX Macro Function Library
- LSI Peripheral and Communication Macros
- Up to 40 MHz Clock Frequency
- Auto-Place and Auto-Route Capability
- Circuit Densities up to 10,000 2-input NAND Gate Equivalents
- I/O Cells Offer 10ns into 100pF Load
- Multiple Package Options

Description

The HSC-RH STANDARD CELL LIBRARY is a proven, high performance library. It is implemented using Harris Semiconductor's radiation hardened advanced CMOS processes. The library offers predesigned and precharacterized cells and macros for which the user prescribes the interconnections in order to develop an application specific IC.

The library has a wide assortment of SSI primitive cells, plus a group of macros which are functionally identical to the standard functions provided by the 74XX series of integrated circuits. Also included is a set of LSI macros representing various highly integrated microprocessor peripheral and communication functions. The designer has the choice of intermixing cells or macros from any of the three groups to optimize his design implementation. The designer may choose the design method and group of functions that is most familiar to him.

The library is supported by a design automation system. The software includes schematic capture, logic simulation, auto-place, autoroute, electrical and design rule verification. If preferred, the system allows the customer to perform the logic entry and simulation phases of the design process either at his own facility or at Harris with engineering support.

Package Options

Ceramic DIP.....14-64 pins

Ceramic Chip Carrier.....14-84 pins (leadless)

Ceramic chip carrier.....48-132 pins (leaded)

Pin grid array.....68-140 pins (contact factory for current availability.)

Supported Processes

The HSC library is supported on the following Harris Radiation Hardened Processes:

SAJI IV — 3 Micron — Single Level Metal
Scaled SAJI IV — 2.5 Micron — Single Level Metal
SAJI VH (2 + 2) — 2.0 Micron — Double Level Metal

CAUTION: Electronic devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings
(Note 1 and 2)

Supply Voltage ..... -0.5V to 7.0V
Input/Output Voltage ..... VSS -0.5V
VDD +0.5V
Input Diode Current 10mA
VI < 0 or VI > VDD
Output Diode Current 10mA
VO < 0 or VO > VDD
Power Dissipation 1000mW
Continuous Supply Pin Current VDD or VSS 100mA
Storage Temperature ..... -65 to 150°C
Continuous Current per Output 10mA

NOTES:

1. Stresses beyond those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under RECOMMENDED OPERATING CONDITIONS is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
2. All applied voltages are with reference to ground (VSS).

Recommended Operating Conditions:

D. C. Electrical Specifications VDD 5V ±10% T_A = Operating Temperature Range

SYMBOL	PARAMETER	TYPE	MIN	MAX	UNIT	CONDITIONS
VDD	Operating Supply Voltage		4.5	5.5	V	
T_A	Operating Temperature		-55	125	°C	
VIH	Input High Voltage	TTL CMOS	2.2 70% VDD		V V	
VIL	Input Low Voltage	TTL CMOS		0.8 30% VDD	V V	
II	Input Current Standard Pull Up Pull Down Pull Up* Pull Down*		 -1.0 -500 -1.0 -50	 +1.0 +1.0 +500 +50	 µA µA µA µA µA	 VSS < VI < VDD VI = 2.2 VI = 0.8
VOH	Output Voltage		2.4		V	IOH = -6.0mA
VOL	Output Voltage			0.4	V	IOL = 6.0mA
IOZ	Output Leakage		-10.0	+10.0	µA	VSS < VO < VDD HI-Z
CI**	Input Capacitance			7.0	pF	VI = VDD or VSS F = 1 MHz
CO**	Output Capacitance			10.0	pF	VO = VDD or VSS F = 1 MHz
CIO**	Input/Output Capacitance			15.0	pF	VO = VDD or VSS F = 1 MHz
IDDSB	Stand-By Supply			100	µA	VI = VDD or VSS II = 0; IO = 0

* Maximum input current for which specified VI will be maintained.

** Sampled and guaranteed but not 100% tested. These values may vary by package type.

A. C. Performance

The propagation delay time of a CMOS gate depends on many factors. Supply voltage, temperature, processing parameters, and output loading are the main influencing factors. Each HSC-RH data sheet has an equation for every delay time associated with that cell to accurately predict the propagation delay for any combination of parameters. Propagation delay times can be estimated for each electrical net in the design using information such as fanout, interconnect capacitance, and the parameters listed above.

The simple example shown in Figure 1 will help illustrate the procedure. Assume that an SC1220 2-input NAND gate is driving two other inputs of a similar gate. To calculate the propagation delay for the conditions, TA = 125°C, VDD = 4.75 volts, and nominal processing parameters appropriate multipliers would be chosen for each condition from the tables on the next page.

125°C 1.32
4.75 volts 1.05
Nominal case processing 1.00

Additional assumptions include an after routing, interconnect capacitance of 0.2pF. From the data sheet for the SC1220, the equation for TPLH at 25°C, 5.0 volts, and nominal process is:

TPLH = .97ns = .28ns(fo) = .94ns (pF-interconnect)
TPLH = .97ns = .28ns(2) = .94ns (0.2)
TPLH = 1.72ns

The effects of temperature, voltage, and processing conditions must be accounted for. By multiplying the nominal value for TPLH from above by the appropriate derating factors we get:

TPLH = 1.72ns* 1.32* 1.05* 1.00
TPLH = 2.38ns (125°C, 4.75 volts, nominal process parameters)

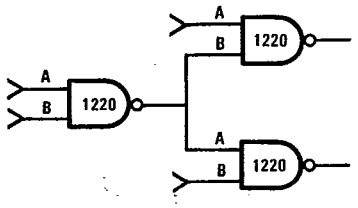
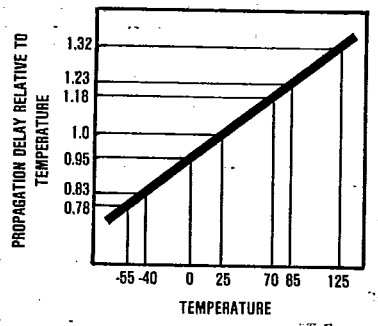


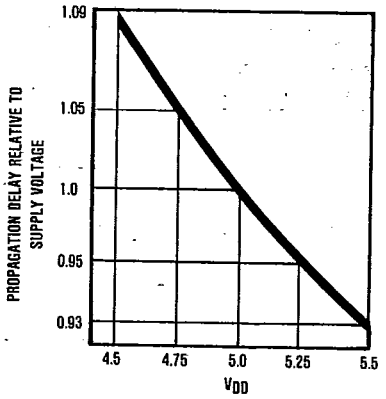
FIGURE 1.

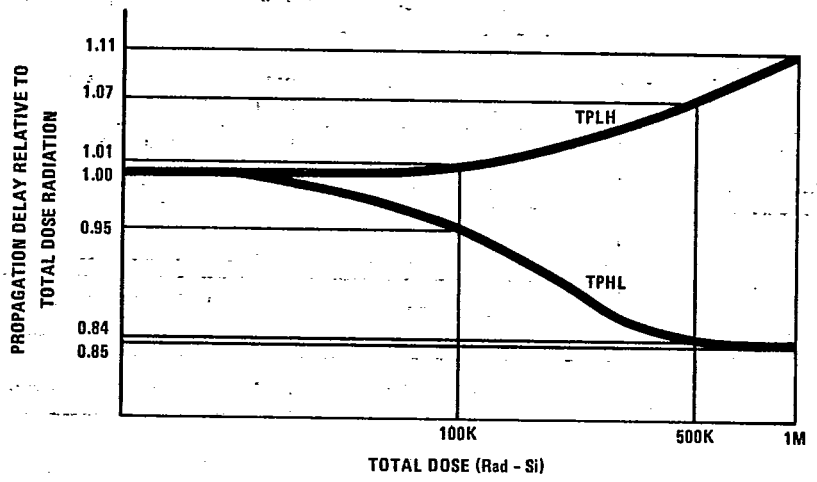
Derating Curves (Scaled SAJI IV)

Process Parameters Derating

P-channel	N-channel	Multiplier
Best	Best	0.76
Nominal	Nominal	1.0
Worst	Worst	1.62



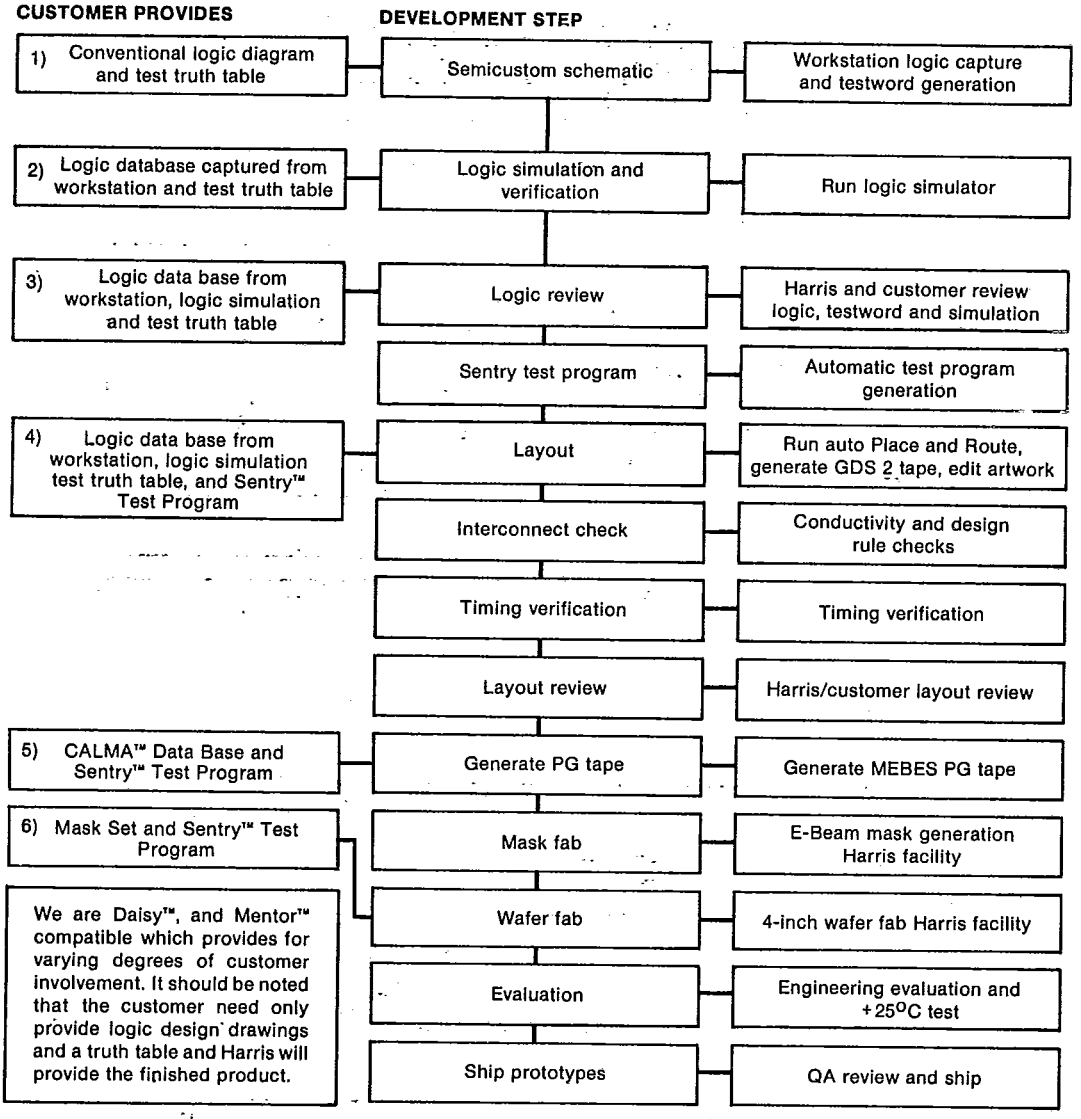




PROPAGATION DELAY DERATING CURVES

NOTE: Due to the fact that N-channel transistors are much more susceptible to the effects of radiation, changes in propagation delay caused by radiation are heavily dependent on cell design. Although most cells will respond to radiation as shown in the propagation delay derating curve shown above, some variation will be seen.

RH Semicustom Design Process Flow



1) Conventional LSTTL Logic Diagram

Submit a conventional LSTTL logic diagram and test truth table. Harris will perform logic simulation/verification and generate a test program. Harris will then perform layout and fabrication phases, then ship prototypes to you.

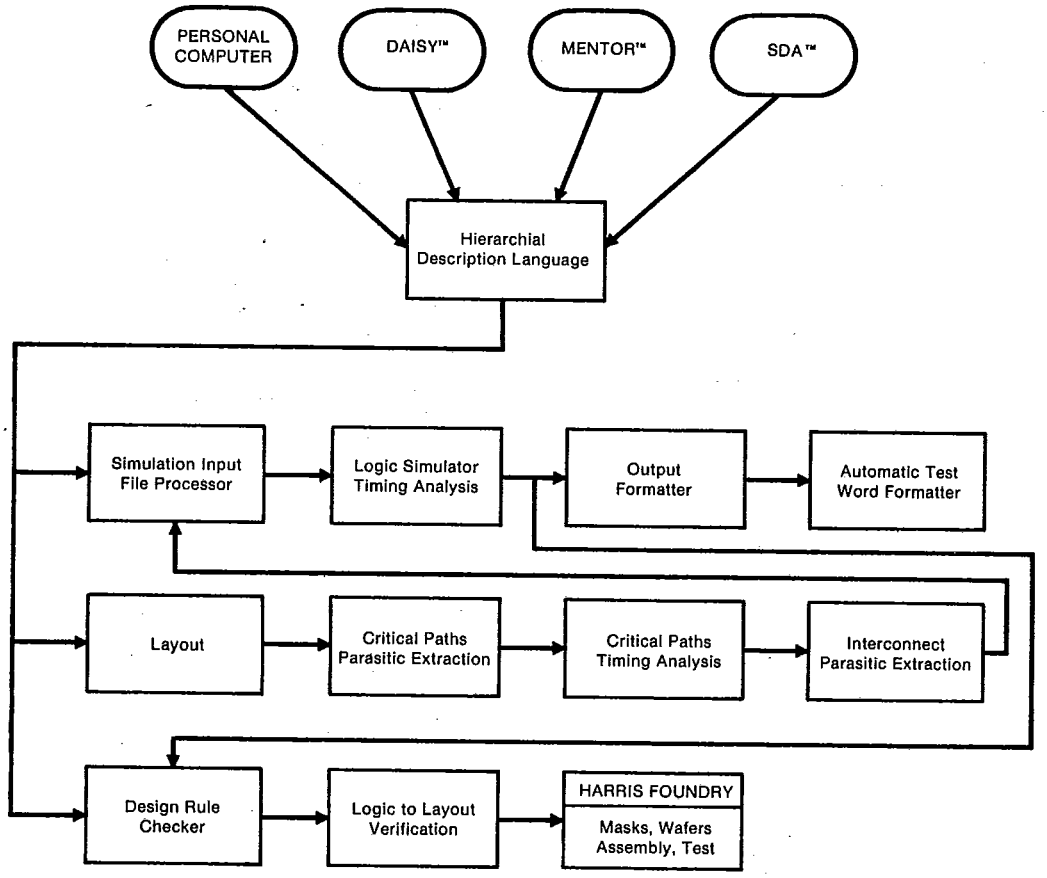
2) Coded Logic

Capture your logic on a workstation using Harris Standard Cells and provide a test truth table. Harris will perform simulation, layout and fabrication phases, then ship the prototypes to you.

3) Coded Logic and Simulation

Capture logic on a workstation, simulate, and provide a test truth table. Harris will perform the layout and fabrication, then ship prototypes to you.

RH Standard Cell - Software



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Cell Functions

SC1010RH	N-CHANNEL BUS PULL DOWN
SC1020RH	P-CHANNEL BUS PULL UP
SC1100RH	INVERTER 1X
SC1100RH	INVERTER 2X
SC1220RH	2 INPUT NAND
SC1230RH	3 INPUT NAND
SC1240RH	4 INPUT NAND
SC1250RH	5 INPUT AND
SC1320RH	2 INPUT NOR
SC1330RH	3 INPUT NOR
SC1340RH	4 INPUT NOR
SC1420RH	EXCLUSIVE OR
SC1430RH	EXCLUSIVE NOR
SC1440RH	2 TO 1 MUX
SC1450RH	NOR LATCH
SC1460RH	A* NOT(B)
SC1470RH	3-STATE INVERTER 1X
SC1480RH	BUFFER 3X
SC1490RH	3-STATE INVERTER 2X
SC1510RH	NOT ((A * B) +C)
SC1520RH	NOT ((A + B)*C)
SC1530RH	D LATCH (Q)
SC1540RH	D LATCH (Q, NOT (Q))
SC1580RH	D LATCH WITH 3-STATE OUTPUT NOT(Q) 1X
SC1590RH	D LATCH (Q, R)
SC1610RH	NAND LATCH
SC1620RH	NOR LATCH WITH 2 RESETS
SC1630RH	A + NOT (B)
SC1640RH	NOT ((A + B + C) * D)
SC1650RH	NOT ((A * B) + C + D)
SC1660RH	SET NOT (RESET) LATCH
SC1710RH	2 OR
SC1720RH	2 AND
SC1730RH	3-STATE INVERTER NOT (G) 1X
SC1770RH	SMALL D FLIP-FLOP (C,R,Q,CO)
SC1780RH	SMALL D FLIP-FLOP (C,R,Q,NOT(Q),CO)
SC1790RH	SMALL D FLIP-FLOP WITH MUX (C,R,Q, NOT(Q),CO)
SC1800RH	D FLIP-FLOP (74LS74 EQUIVALENT)
SC1810RH	D FLIP-FLOP (C,Q,NOT(Q),R)
SC1820RH	D FLIP-FLOP (C,Q,NOT(Q),R,S)
SC1830RH	MUX D FLIP-FLOP (C,Q,NOT(Q),S,R)
SC1840RH	D FLIP-FLOP (C,Q,NOT(Q),S)
SC1850RH	TOGGLE FLIP-FLOP (C,Q,NOT(Q),S)
SC1860RH	TOGGLE FLIP-FLOP WITH SYNCHRONOUS LOAD
SC1870RH	JK FLIP-FLOP (S)
SC1880RH	JK FLIP-FLOP (R)
SC1890RH	JK FLIP-FLOP (S,R)
SC1900RH	3-STATE INVERTER NOT(G) 4X
SC1910RH	3-STATE 2 INPUT NOR
SC1920RH	NOT ((A + B) * C * D * E)
SC1930RH	DELAY INVERTER 12ns
SC1940RH	3-STATE 2 INPUT NOR NOT (G)
SC1950RH	ONE SHOT 20ns PULSE
SC1960RH	NOT (((A*B)+)*D)
SC1970RH	NOT ((A*B)+(C*D)
SC1980RH	NOT (((A + B)*C)+D)
SC2000RH	3-STATE INVERTER NOT(G) 2X
SC2030RH	3 INPUT AND
SC2060RH	NOT((A + B) * C * D)
SC2080RH	NOT((A * B * C)+D)
SC2090RH	DELAY INVERTER 6ns
SC2100RH	NOT((A + B)*(C + D)
SC2110RH	NOT((A * B * C) + D + E)
SC2120RH	3 INPUT OR
SC2130RH	3-STATE INVERTER 4X
SC2160RH	1 BIT FULL ADDER
SC2310RH	BUS HOLD CIRCUIT
SC7100RH	TTL INPUT BUFFER WITH PULL UP
SC7110RH	TTL INPUT BUFFER WITH PULL DOWN
SC7150RH	TTL INPUT BUFFER
SC7160RH	CMOS INPUT BUFFER
SC7200RH	OUTPUT BUFFER
SC7120RH	OUTPUT BUFFER-OPEN DRAIN P CHANNEL
SC7220RH	OUTPUT BUFFER-OPEN DRAIN N CHANNEL
SC7230RH	OUTPUT BUFFER-3-STATE ACTIVE LOW ENABLE
SC7240RH	LATCHED INPUT BUFFER-TTL
SC7250RH	BI-DIRECTIONAL BUFFER WITH TTL INPUT
SC7260RH	BI-DIRECTIONAL BUFFER WITH TTL INPUT WITH PULL UP
SC7270RH	BI-DIRECTIONAL BUFFER WITH TTL INPUT WITH PULL DOWN
SC7280RH	BI-DIRECTIONAL BUFFER WITH CMOS INPUT
SC7300RH	OUTPUT BUFFER-INVERTING
SC7400RH	OSCILLATOR 2 TO 30MHz
SC7900RH	VSS PAD
SC7910RH	VCC PAD
SC7920RH	AUXILIARY VSS PAD
SC7930RH	AUXILIARY VCC PAD

74XX Macro Functions

SN7400RH	SN7436RH	SN74109RH	SN74152RH	SN74173RH	SN74237RH	SN74259RH
SN7402RH	SN7442RH	SN74112RH	SN74153RH	SN74174RH	SN74238RH	SN74273RH
SN7404RH	SN7451RH	SN74113RH	SN74154RH	SN74175RH	SN74240RH	SN74280RH
SN7407RH	SN7473RH	SN74114RH	SN74157RH	SN74180RH	SN74241RH	SN74283RH
SN7408RH	SN7474RH	SN74126RH	SN74158RH	SN74181RH	SN74242RH	SN74292RH
SN7410RH	SN7475RH	SN74133RH	SN74160RH	SN74182RH	SN74243RH	SN74298RH
SN7411RH	SN7476RH	SN74137RH	SN74161RH	SN74190RH	SN74244RH	SN74352RH
SN7420RH	SN7477RH	SN74138RH	SN74162RH	SN74191RH	SN74245RH	SN74373RH
SN7421RH	SN7483RH	SN74139RH	SN74163RH	SN74192RH	SN742454RH	SN74374RH
SN7427RH	SN7485RH	SN4147RH	SN74164RH	SN74193RH	SN74251RH	SN74377RH
SN7430RH	SN7486RH	SN74148RH	SN74165RH	SN74194RH	SN74253RH	SN74393RH
SN7432RH	SN74107RH	SN74151RH	SN74166RH	SN74195RH	SN74257RH	SN74645RH
					SN74258RH	

LSI Macro Functions*

SM4702RH	PROGRAMMABLE BIT RATE GENERATOR
SM6402RH	UART
SM6406RH	PROGRAMMABLE ASYNCHRONOUS COMMUNICATIONS INTERFACE
SM6408RH	ASYNCHRONOUS MANCHESTER ADAPTER
SM6409RH	MANCHESTER ENCODER/DECODER
SM15530RH	MANCHESTER ENCODER/DECODER
SM15531RH	PROGRAMMABLE MANCHESTER ENCODER/DECODER
SM15531BRH	PROGRAMMABLE MANCHESTER ENCODER/DECODER-HIGH SPEED
SM82C37ARH	PROGRAMMABLE DMA CONTROLLER
SM82C52RH	FULL DUPLEX UART WITH BIT RATE GENERATOR
SM82C54RH	PROGRAMMABLE INTERVAL TIMER
SM82C55ARH	PROGRAMMABLE PERIPHERAL INTERFACE
SM82C56ARH	MUART
SM82C59ARH	PRIORITY INTERRUPT CONTROLLER
SM82C84ARH	CLOCK GENERATOR/DRIVER
SM82C82RH	OCTAL BUS DRIVER WITH LATCHED INPUTS
SM82C83RH	OCTAL BUS DRIVER WITH LATCHED INPUT-INVERTING
SM82C86RH	OCTAL BUS TRANSCEIVER
SM82C87RH	OCTAL BUS TRANSCEIVER-INVERTING
SM82C88RH	BUS CONTROLLER
SM82C89RH	BUS ARBITER
SM82C85RH	STOP CLOCK GENERATOR

*Contact Factory on availability

Radiation Screening Procedure

1. At least 20% of the yielding wafers contribute equally to a population of dice. From that population, a radiation test sample is selected. The sample has a size equivalent to 2 dice taken from 20% of the yielding wafers in a diffusion run.
2. The sample die shall be assembled and tested to the customer's specification for proper operation.
3. The sample devices shall be subjected to a Total Dose Radiation level of 2 x 10^5 Rad-Si (±10%) from a Gammacell 220 Cobalt 60 source or equivalent. The samples shall be biased at V_{DD} with all inputs high. The dose rate shall be between 100 rads/sec and 300 rads/sec.
4. The samples will be tested to the data sheet limits within one hour after irradiation. The lot will be accepted only if all units, exclusive of nonradiation failures, meet the specified limits.
5. Radiation screening to a higher total dose is available. Customers should contact their local representative for details.

Radiation Effects

The HSC-CELL LIBRARY has been designed to survive in a radiation environment and to meet the electrical characteristics after exposure to 100K Rad-Si. Latch-up free operation is achieved by the use of epitaxial starting material. Improved total dose hardness is obtained with special low temperature processing cycles. On a production basis, Harris performs screens for total dose hardness to a level of 2 x 10^5 Rad-Si. Transient radiation tests have shown the following results:

- Latch-up free to doses $\geq 1 \times 10^{12}$ rads/sec.
- Upset (loss of stored data) $\geq 10^9$ rads/sec.