PRELIMINARY DATA SHEET

NEC ELECTRON DEVICE

MOS INTEGRATED CIRCUIT
μPD6480

MOTION DETECTION & Y/C SEPARATION LSI CHIP FOR EDTV

The μPD6480 has a function to separate the luminance signal (Y signal) and color signal (C signal) from the composite video signal digitalized in units of 8 bits with an optimum filter according to the condition of the screen.

The LSI chip also incorporates a motion detecting function to discriminate each screen condition and thus by using the μPD6480 alone as a signal processing LSI chip, three-dimensional Y/C signal separation can be implemented.

Furthermore, the μPD6480 incorporates line buffers which helps reduce the number of peripheral components and also logical comb filters which enhance the quality of pictures, especially moving pictures.

By combining this LSI chip with three other LSI chips (YCP II, YCI II, and TIG II), even a signal processing system for enhanced-definition television (EDTV) may be configured.

FEATURES

- Incorporates both the Y/C signal separation function and the motion detection function on a signal chip.
- Selects a Y/C separation filter most suitable for the screen condition from among the following three: a filter for inter-frame Y/C separation, a filter for intra-field Y/C separation (logical comb filters), and a filter for frequency separation.
- Built-in line buffers (capacity: 4.5 lines)
- Built-in logical comb filters (for improving the quality of pictures)
- Built-in one-frame-period differential type motion detection circuit (for luminance/color signal differential detection)
- Built-in motion signal extension circuit (for signal extension in the vertical, horizontal, and temporal directions)
- Built-in vertical aperture compensation circuit
- Can handle S-terminal inputs.
- Built-in external memory floating function
- Allows data setting by serial bus control.
- 5 V single power supply
- 100-pin plastic QFP (14 x 20 mm)

ORDERING INFORMATION

PART NUMBER	PACKAGE	QUALITY GRADE
μPD6480GF-3BA	100-pin plastic QFP	Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

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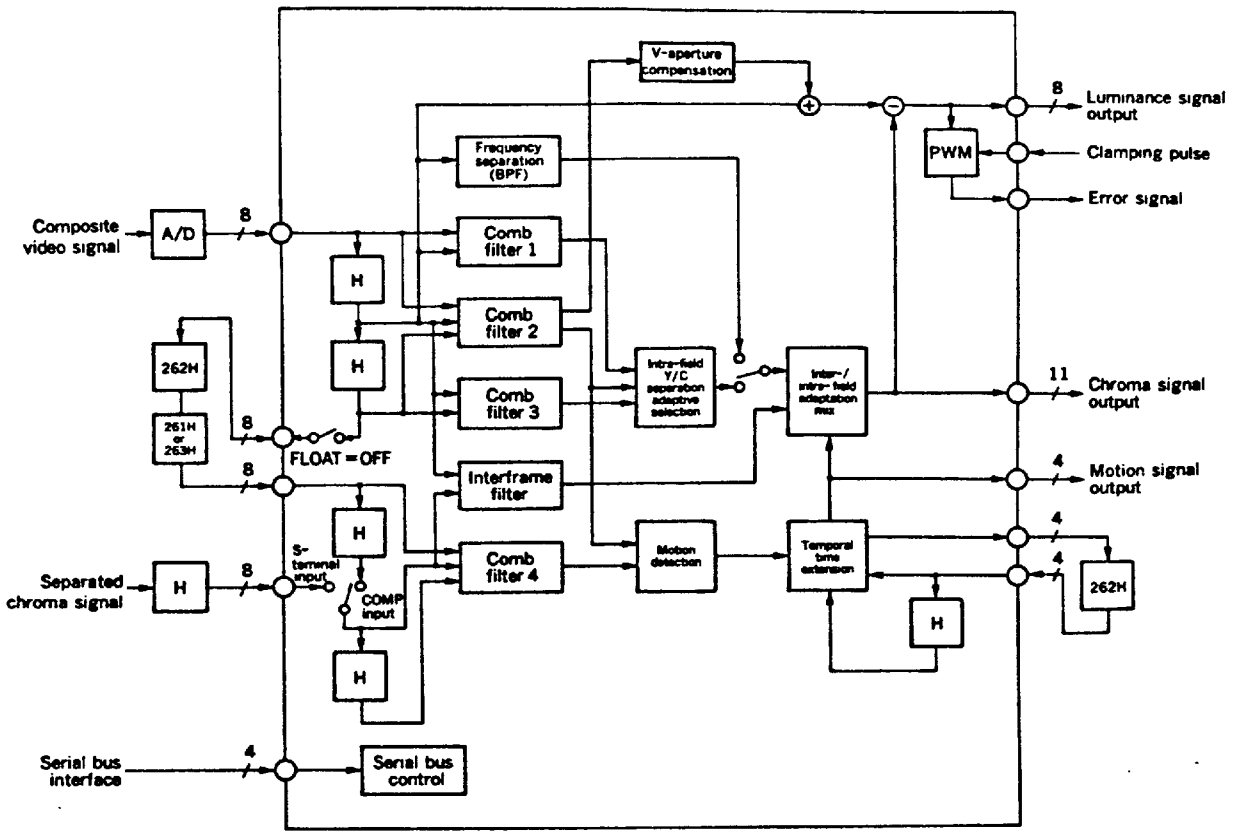
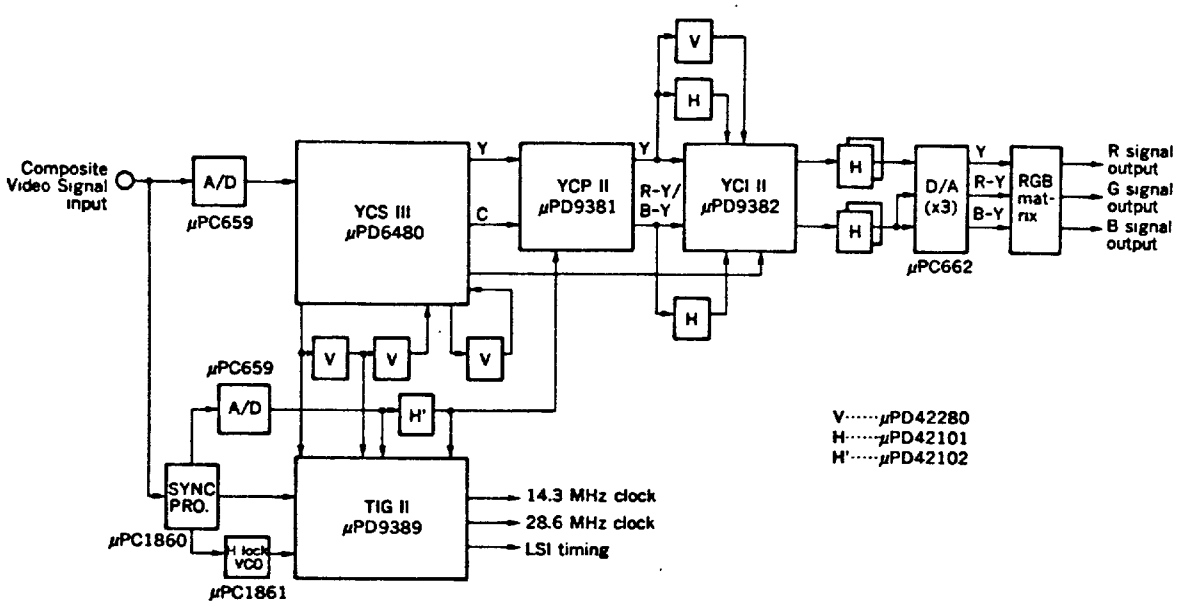
BLOCK DIAGRAM

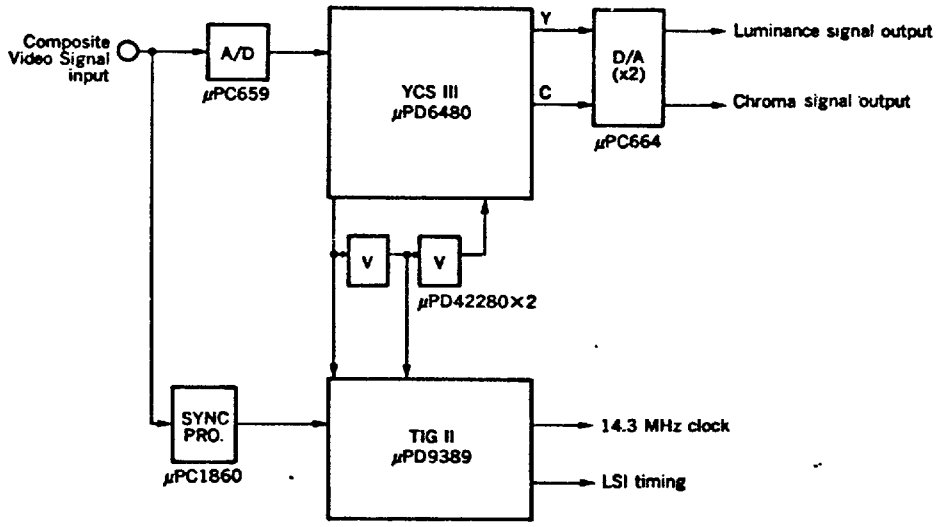


SYSTEM APPLICATION BLOCK DIAGRAMS

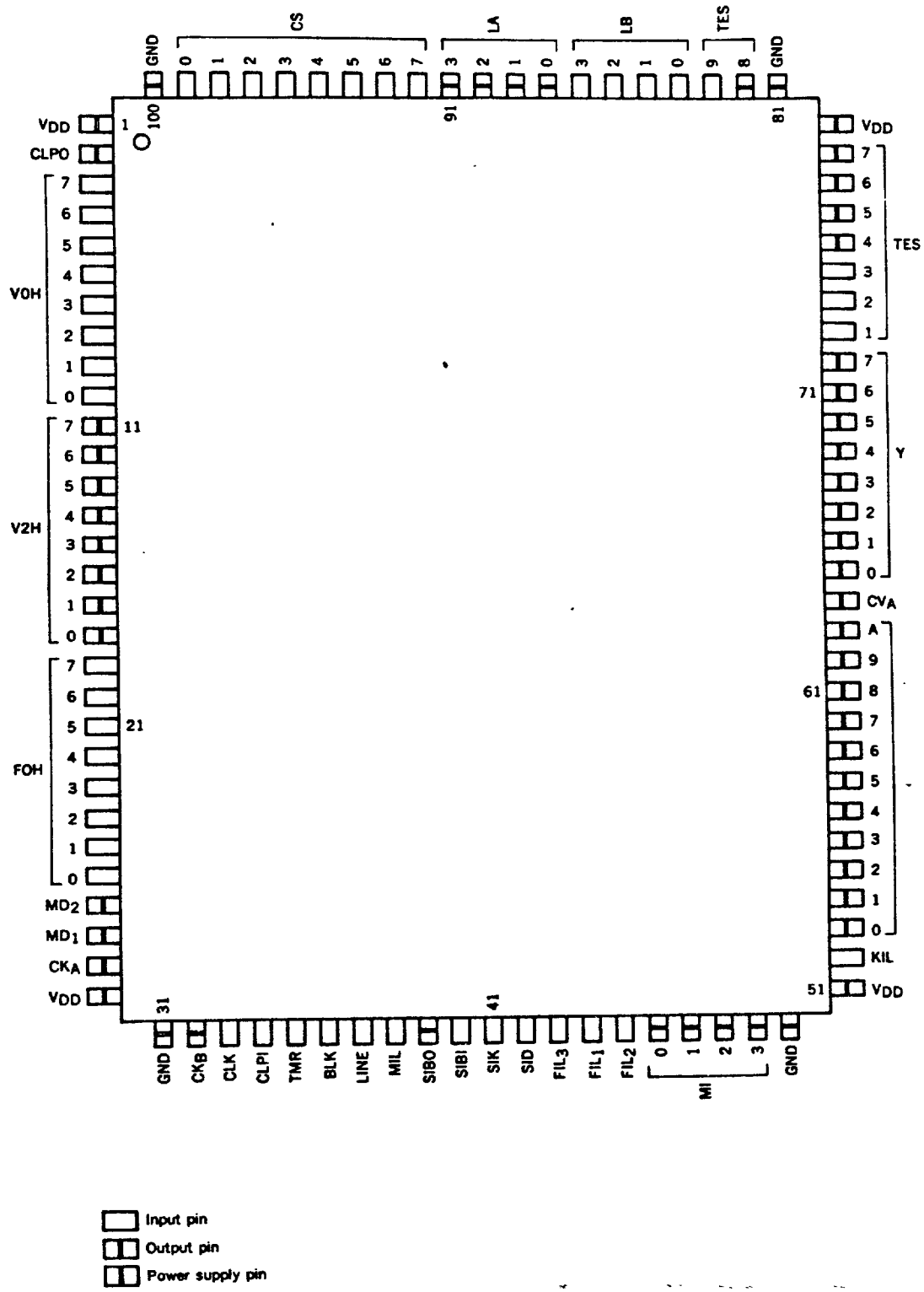
(1) EDTV System



(2) Three-Dimensional Y-C Separation System



PIN CONFIGURATION (Top View)



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	V_{DD}	−0.3 to +7.0	V	
Input Voltage	V_I	−0.3 to V_{DD} +0.3	V	
Output Voltage	V_O	−0.3 to V_{DD} +0.3	V	
Power Dissipation (package)	P_D	500	mW	T_a = 70 °C
Operating Temperature	T_{opt}	−20 to +70	°C	
Storage Temperature	T_{stg}	−40 to +125	°C	

RECOMMENDED OPERATING CONDITIONS (T_a = 25 °C unless otherwise specified)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Supply Voltage	V_{DD}	4.5	5.0	5.5	V	
Input Voltage	V_I	0		V_{DD}	V	
Output Voltage	V_O	0		V_{DD}	V	
Clock Input Frequency	f_{CK}		14.318		MHz	

ELECTRICAL CHARACTERISTICS (T_a = −20 °C to +70 °C, V_{DD} = 5.0 ±0.5 V, GND = 0 V)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS	
Supply Voltage	V_{DD}	4.5	5.0	5.5	V		
Current Consumption	I_{DD}			80	mA		
High-Level Input Voltage	V_{IH}	0.7 V_{DD}		V_{DD}	V	CMOS Level Input	
Low-Level Input Voltage	V_{IL}	0		0.3 V_{DD}	V		
High-Level Input Voltage	V_{IH}	2.0		V_{DD}	V	TTL Level Input	
Low-Level Input Voltage	V_{IL}	0		0.8	V		
High-Level Threshold Voltage	V_{T^+}	0.35 V_{DD}	0.55 V_{DD}	0.70 V_{DD}	V	CMOS Schmitt Level Input	
Low-Level Threshold Voltage	V_{T^-}	0.20 V_{DD}	0.40 V_{DD}	0.55 V_{DD}	V		
Hysteresis Voltage	V_H	0.05 V_{DD}	0.15 V_{DD}	0.45 V_{DD}	V		
High-Level Threshold Voltage	V_{T^+}	0.20 V_{DD}	0.40 V_{DD}	0.55 V_{DD}	V	TTL Schmitt Level Input	
Low-Level Threshold Voltage	V_{T^-}	0.05 V_{DD}	0.25 V_{DD}	0.40 V_{DD}	V		
Hysteresis Voltage	V_H	0.05 V_{DD}	0.15 V_{DD}	0.45 V_{DD}	V		
Input Leak Current	I_I	−10	0	10	μA	Ordinary Input	V_I = V_{DD} or GND
High-Level Input Current	I_{IH}	40	100	270	μA	Pulled-down Input	V_I = V_{DD}
Low-Level Input Current	I_{IL}	−270	−100	−40	μA	Pulled-up Input	V_I = GND
High-Level Output Current	I_{OH}		−3.5	−1.6	mA	CMOS Level Output (−1.6/3.0 mA)	V_{OH}=V_{DD}−0.4 V
Low-Level Output Current	I_{OL}	3.0	6.5		mA		V_{OL}=0.4 V
High-Level Output Current	I_{OH}		−7.0	−3.2	mA	CMOS Level Output (−3.2/6.0 mA)	V_{OH}=V_{DD}−0.4 V
Low-Level Output Current	I_{OL}	6.0	13.0		mA		V_{OL}=0.4 V
Low-Level Output Current	I_{OL}	6.0	13.0		mA	N-Open-Drain	V_{OL}=0.4 V
Output Leak Current	I_O	−10	0	10	μA	Tri-state, O-Dr	V_O=V_{DD} to GND

SWITCHING CHARACTERISTICS

(T_a = −20 °C to +70 °C, V_{DD} = 5.0±0.5 V, GND = 0 V, C_L = 15 pF, t_r = t_f = 2 ns)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS	
Clock Input Frequency	f_{CK}		14.31818		MHz		
Rise Time	t_{TLH}		7.3	16.0	ns	CMOS Level Output (−1.6/3.0 mA)	V_O = "L" → "H"
Fall Time	t_{THL}		3.6	7.8	ns		V_O = "H" → "L"
Rise Time	t_{TLH}		2.5	5.5	ns	CMOS Level Output (−3.2/6.0 mA)	V_O = "L" → "H"
Fall Time	t_{THL}		1.7	3.7	ns		V_O = "H" → "L"
Propagation Delay Time	t_{PHL}	5	19	40	ns	CMOS Level Output	V_O = "H" → "L"
	t_{PLH}	5	19	40	ns		V_O = "L" → "H"
	t_{PHZ}	5	19	40	ns	Tri-state Output	V_O = "H" → "Z"
	t_{PZH}	5	19	40	ns		V_O = "Z" → "H"
	t_{PLZ}	5	19	40	ns	Tri-state, O-Drain Output	V_O = "L" → "Z"
	t_{PZL}	5	19	40	ns		V_O = "Z" → "L"
Setup Time	t_{SET}	10			ns		
Hold Time	t_{HOLD}	10			ns		
Input Capacitance	C_I		5	10	pF	CMOS/TTL Level Input	V_{DD} = V_I = 0 V, f = 1 MHz

FUNCTIONAL DESCRIPTION OF EACH PIN

Pin			I/O characteristics			Functional description
No.	Symbol	Pin name	I/O	Level	PU/PD [kΩ] I_{OH}/I_{OL} [mA]	
1	V_{DD}	Power supply				This pin supplies a supply voltage of 5 V (typ).
2	CLPO	Clamping D/A output	O	CMOS	−3.2/6.0	This pin outputs the difference between the clamping level and the video level (pedestal level) via PWM. This output signal makes the pulse width variable between 1/16 and 15/16 at a cycle of 4.4 μs.
3 to 10	VOH_7 to VOH_0	Video input (0 H delay)/Luminance input	I (SB)	TTL		These eight pins input an 8-bit digital signal converted from the analog video signal. In the S-terminal mode, these pins input the luminance signal. The pedestal level must be at level 64. (VOH_7: MSB, VOH_0: LSB)
11 to 18	$V2H_7$ to $V2H_0$	Video output (2 H delay)/Burst-added main signal output	O (SB)	CMOS tri-state	−1.6/3.0	These eight pins output a signal with a delay of 2H (two horizontal scanning periods) from the video signal. In the S-terminal mode, these pins output a main signal to which the burst part of the chroma signal input from Pins 92 to 99 (CS_7 to CS_0) has been added. ($V2H_7$: MSB, $V2H_0$: LSB)
19 to 26	FOH_7 to FOH_0	Video input (1 frame delay)	I (SB)	TTL		These eight pins input a signal with a delay of one frame from the video signal. In the S-terminal mode, these pins input a signal with a delay of one frame from the main signal for detection of ΔY between frames. (FOH_7: MSB, FOH_0: LSB)
27 28	MD_2 MD_1	S-terminal mode output	O	CMOS tri-state	−1.6/3.0	In the S-terminal mode, these two pins output a signal to control the output enabling or the amount of delay (delay length) of a memory to be externally connected. S-terminal mode: MD_2 = "H", MD_1 = "L"
29	CK_A	Clock output	O	CMOS tri-state	−3.2/6.0	This pin is used to output a clock for the A/D converter or a memory to be externally connected. This output has a delay of 10 ns (typ.) to the CLK (Pin 33) input.
30	V_{DD}	Power supply				This supplies a supply voltage of 5 V (typ.).
31	GND	Ground				This pin must be zero (0 V) potential with respect to ground.
32	CK_B	Clock output	O	CMOS tri-state	−3.2/6.0	This pin is used to output a clock for the A/D converter or a memory to be externally connected. This output has a delay of 10 ns (typ.) to the CLK (Pin 33) input.
33	CLK	Clock input	I	CMOS		This pin inputs a clock of 4 f_{SC} (14.318 18 MHz).
34	CLPI	Clamping pulse input	I	TTL, Schmitt	PD: 50	At the leading edge of the active-high clamping pulse, the μPD6480 takes in the video signal and compares it with the clamping level (at level 64).
35	TMR	Test input	I	CMOS	PU: 50	Input pin for testing. Either connect this pin to the V_{DD} pin or leave it open.
36	BLK	Blanking input	I	CMOS	PD: 50	This pin inputs a signal which becomes High during the blanking period, with a delay of 3 clocks from the main signal. During the blanking period, the V aperture compensation function and the synchronous protection function are turned off and as the Y/C separation function, the frequency separation type Y/C separation mode is selected.
37	LINE	Forced line comb-filter input for Y-C separation	I	CMOS	PD: 50	Set this pin to High if the Y/C Separation mode is to be fixed to intra-field Y/C separation.
38	MIL	Forced motion input for motion detection output	I	CMOS	PD: 50	Set this pin to High if the motion detection output signal to be output from Pins 46 to 49 (MI_0 to MI_3) is to be set to High by force.
39	SIBO	Serial bus busy output	O	N-Open-Drain	/6.0	This pin outputs a Busy signal for reply to the Serial Bus Acknowledge signal. Connect this pin to Pin 40 (SIBI) by the wired OR method and output "L" in reply to the Acknowledge signal.

Pin			I/O characteristics			Functional description
No.	Symbol	Pin name	I/O	Level	PU/PD [kΩ] I_{OH}/I_{OL} [mA]	
40	SIBI	Serial bus busy input	I	CMOS Schmitt		This pin inputs a Busy signal for receiving serial bus data. The μPD6480 starts receiving serial bus data if this pin goes Low and returns to the initial condition (internal data fetching) if this pin goes High.
41	SIK	Serial bus clock input	I	CMOS Schmitt		This pin inputs a clock for receiving serial bus data. The μPD6480 reads data input to Pin 42 (SID) at the leading edge of this clock.
42	SID	Serial bus data input	I	CMOS Schmitt		This pin inputs serial bus data. The μPD6480 reads data in synchronization with the clock input to Pin 41 (SIK).
43	FIL_3	Filter selection 3	I	CMOS	PD: 50	This pin selects the filter for interframe ΔY detection. Normally, connect this pin to the GND pin or leave it open.
44	FIL_1	Filter selection 1	I	CMOS	PD: 50	Input a High level to this pin if the intra-field Y/C separation is to be changed to the Frequency separation mode. Normally, this pin is used to connect the interleave detection output of the TIG (μPD9383).
45	FIL_2	Filter selection 2	I	CMOS	PD: 50	This pin selects the band of the chroma signal for intra-field Y/C separation. If this pin becomes High, a narrow band will be selected. Normally, this pin set to Low for use.
46 to 49	MI_0 to MI_3	Motion detection output	O (SB)	CMOS	−1.6/3.0	These four pins the extended motion signal output with a delay of 13 clocks from the main signal. (MI_3: MSB, MI_0: LSB)
50	GND	Ground				This pin must be zero (0 V) potential with respect to ground.
51	V_{DD}	Power supply				This pin supplies a supply voltage of 5 V (typ.).
52	KIL	Killer input	I	CMOS	PD: 50	Input a High level to this pin if the luminance signal is to be output without subtracting the chroma signal from the main signal.
53 to 63	C_0 to C_A	Chroma output	O (2'S)	CMOS	−1.6/3.0	These 11 pins output the chroma signal obtained by separating Y and C signals from the video signal with a delay of 17 clocks from the main signal. Gain becomes X2 at composite input or X1 in the S-terminal mode. Each gain may be halved by serial bus control. (C_A: MSB [SIGN], C_0: LSB)
64	CV_A	Chroma inversion output	O	CMOS	−1.6/3.0	This pin outputs the inversion of the MSB of the chroma output which is to be output to Pin 63 (C_A). When connecting the D/A converter to the chroma output, use this pin as MSB.
65 to 72	Y_0 to Y_7	Luminance output	O (SB)	CMOS	−1.6/3.0	These eight pins output the luminance signal obtained by separating Y and C signals from the video signal with a delay of 17 clocks from the main signal. (Y_7: MSB, Y_0: LSB)
73 to 75	TES_1 to TES_3	Test input	I	CMOS	PD: 50	Input pin for testing. Eighter connect this pin to the GND pin or leave it open.
76 to 79	TES_4 to TES_7	Test output	O	CMOS	−1.6/3.0	Output pin for testing.
80	V_{DD}	Power supply pin				This pin supplies a supply voltage of 5 V (typ.).
81	GND	Ground				This pin must be zero (0 V) potential with respect to ground.
82	TES_8	Test output	O	CMOS	−1.6/3.0	Output pin for testing.
83	TES_9	Test input	I	CMOS	PD:50	Input pin for testing. Either connect this pin to the GND pin or leave it open.
84 to 87	LB_0 to LB_3	Motion extension input	I (SB)	TTL		These four pins input the output signal for motion extension to be output to Pins 89 to 91 (LA_0 to LA_3), with a delay of 262 H. (LB_3: MSB, LB_0: LSB)
88 to 91	LA_0 to LA_3	Motion extension output	O (SB)	CMOS tri-state	−1.6/3.0	Pins to extend the motion signal (LA_3: MSB, LA_0: LSB)

Pin			I/O characteristics			Functional description
No.	Symbol	Pin name	I/O	Level	PU/PD [kΩ] I_{OH}/I_{OL} [mA]	
92 to 99	CS_7 to CS_0	Chrome input	I (SB)	TTL		These eight pins input the chroma signal in the S-terminal mode. When not using the S-terminal mode, ground these pins. . (CS_7: MSB, CS_0: LSB)
100	GND	Ground				This pin must be zero (0 V) potential with respect to ground.

(SB) indicates that the digital data format is Straight Binary code.
(2'S) indicates 2's complement code.

FUNCTIONAL DETAILS

1. Y/C SEPARATION

The μPD6480 incorporates three types of Y/C separation filters, the most suitable of which can be selected according to the input signal.

(1) Interframe Y/C separation filter

The filter performs Y/C separation by utilizing the correlativity of NTSC signals and the interframe characteristics of the color signal phase. This filter is used at the still picture part of any NTSC standard signal.

(2) Interline Y/C separation filter

This filter is one of intra-field Y/C separation filters and performs Y/C separation by utilizing the correlativity of NTSC signals and the interframe characteristics of the color signal phase. This filter consists of logical comb filters and functions to minimize dot disturbance.

(3) Frequency separation type Y/C separation filter

This filter is one of intra-field Y/C separation filters and separates the color signal from the luminance signal with a frequency.

1.1 SWITCHING BETWEEN INTERFRAME Y/C SEPARATION FILTER AND INTRA-FIELD Y/C SEPARATION FILTER

Switching from the interframe Y/C separation filter to an intra-field Y/C separation filter or vice versa is basically controlled by a motion signal from the motion detection section of this LSI chip. This filter switching may also be controlled with serial bus data.

First, how the filter switching is controlled by the motion signal will be explained. Because the motion signal consists of four bits, 16 different bit combinations of the motion signal can be used for filter switching as follows:

Motion signal	Intra-field Y/C separation	Interframe Y/C separation	Motion signal	Intra-field Y/C separation	Interframe Y/C separation
0	0	1	8	0.5	0.5
1	0.0625	0.9375	9	0.5625	0.4375
2	0.125	0.875	10	0.625	0.375
3	0.1875	0.8125	11	0.6875	0.3125
4	0.25	0.75	12	0.75	0.25
5	0.3125	0.6875	13	0.8125	0.1875
6	0.375	0.625	14	0.875	0.125
7	0.4375	0.5625	15	1	0

This table shows the ratio when adaptively synthesizing the filter outputs. In other words, the output is the sum of interframe Y/C separation and intra-field Y/C separation with "1" taken as a reference value. The unit of motion signal is indicated by hexadecimal code.

Next, for the filter switching by serial bus data, the MSD and MSC bits of subaddress SA_6 are used. This filter switching is not by 16 different bit combinations as shown in the above table, but selects either the interframe Y/C separation or the intra-field Y/C separation. If the MSC bit is "1" and the MSD bit is "0", the intra-field Y/C separation will be selected. If both the MSC and MSD bits are "1", the interframe Y/C separation will be selected. If the MSC bit is "0", filter switching will be carried out by the motion signal as shown in the above table.

A Y/C separation filter can also be selected with the external LINE pin (Pin 37). If a High level is input to the LINE pin, the intra-field Y/C separation will be selected by force. If the LINE pin is Low, filter switching will be carried out by the motion signal as shown in the above table. Set this LINE pin to High when a signal other than NTSC standard signals, which cannot perform three-dimensional processing such as a playback signal for home-use VCR is input.

1.2 FILTER SELECTION IN INTRA-FIELD Y-C SEPARATION

Switching between the interline Y/C separation mode and the frequency separation mode when the intra-field Y/C separation has been selected can be performed with the external FIL_1 pin (Pin 44) or serial bus data.

The FIL_1 pin is normally controlled by an output from the interleave detection circuit of the μPD9383 (TIG). This interleave detection output signal is intended for output when the interleave relation between the chroma signal and the horizontal sync signal is signicantly disordered. By using this detection output, Y/C separation can be performed accurately for even a signal which has a disordered interleave relation.

If a High level is input to the FIL_1 pin, the frequency separation type Y/C separation filter will be selected. If a Low level is input to this pin, the interline Y/C separation filter will be selected.

To control the filter switching with serial bus data, the BPFS bit of subaddress SA_6 is used. If the BPFS bit is set to "1", the frequency separation type Y/C separation filter will be selected. If this bit is set to "0", the interline Y/C separation filter will be selected.

1.3 FILTER CHARACTERISTICS FOR Y/C SEPARATION

Fig. 1-1 shows a block diagram of the Y/C separation section. The filters used internally are all configured with FIR filters. The filter characteristics of intra-field Y/C separation (interline Y/C separation and frequency separation type Y/C separation) and interframe Y/C separation are as shown in Figs. 1-2 and 1-3, respectively. In these characteristics, the characteristics of comb filters are not included.

Fig. 1-1. Block Diagram of Y/C Separation Section

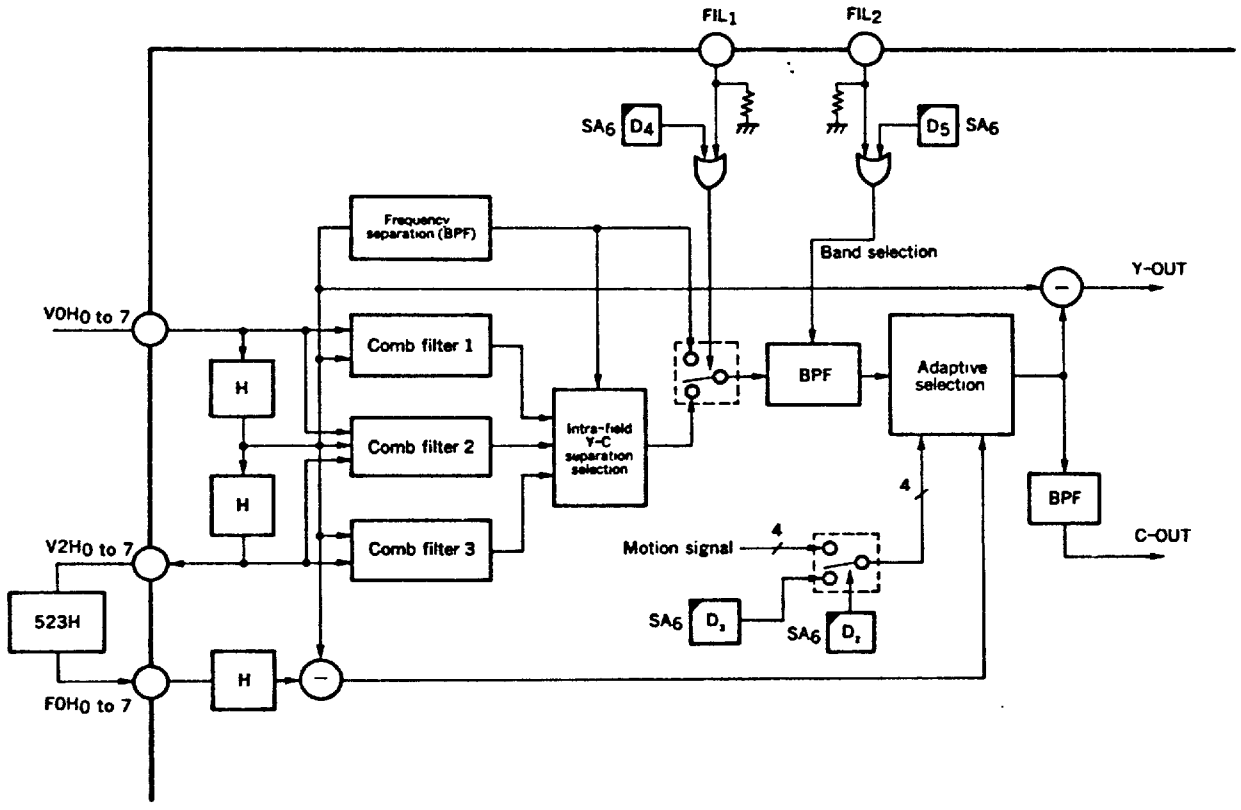


Fig. 1-2. Filter Characteristics of Interline Y/C Separation and Frequency Separation Type Y/C Separation (Calculated Values)

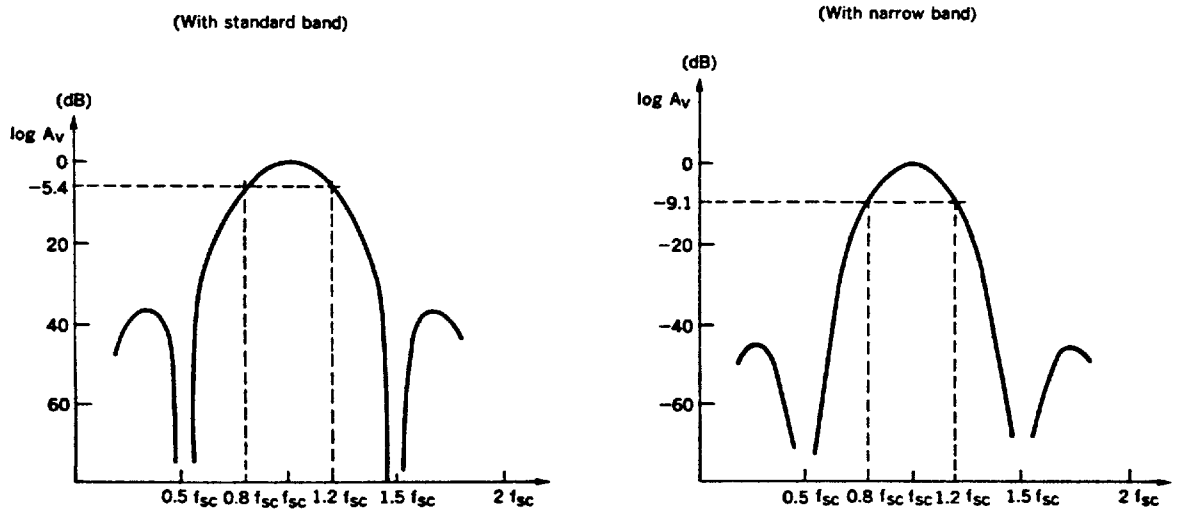
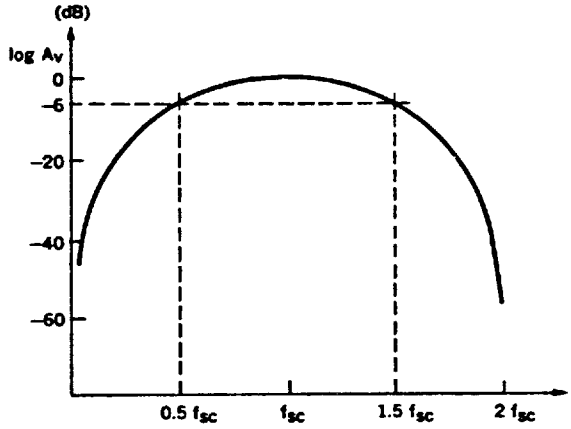


Fig. 1-3. Filter Characteristics of Interframe Y/C Separation (Calculated Values)



2. A/D INPUT

As the video signal input of the μPD6480, a signal whose pedestal level is at level 64 (full scale: 256 levels) must be input. The dynamic range of the video signal input should be determined by taking into account the non-uniformity of input signals. Fig. 2-1 shows the input waveform of a video signal with the sync signal section taken on a full scale basis.

In the EDTV system, sync signals will be protected to the last. Sync signals separated from the luminance signal after the double scanning speed conversion may be used as deflection related signals. For this reason, each sync signal is important information and must be input by converting it from an analog to a digital form.

The μPD6480 has a feedback loop to assist in adjusting this pedestal level. In this circuit, the pedestal level of the input video signal is sampled with a clamping pulse input from the external CLPI pin and sampled level is compared with Level 64 which is an internally fixed value. The difference in value between the two compared levels is then output through the D/A converter in the PWM unit. This output is converted into a DC voltage with an external filter and fed back to the pedestal level adjustment before the A/D conversion.

Fig. 2-1. Video Signal Input Waveform (with Sync Signal Section Taken on Full Scale Basis)

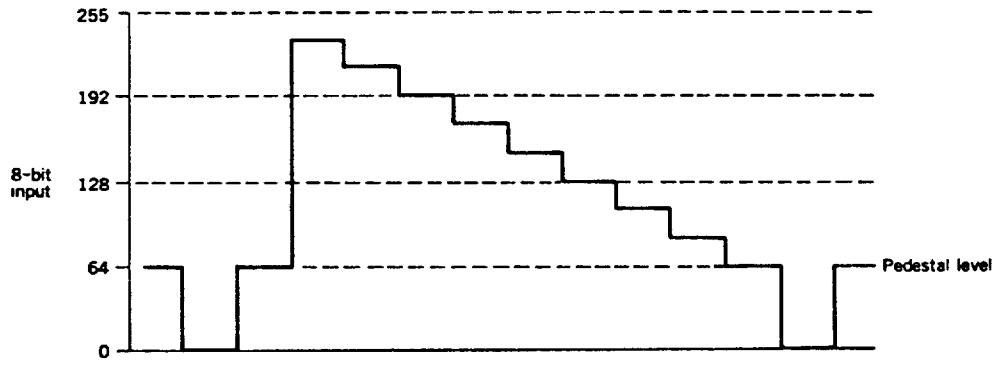
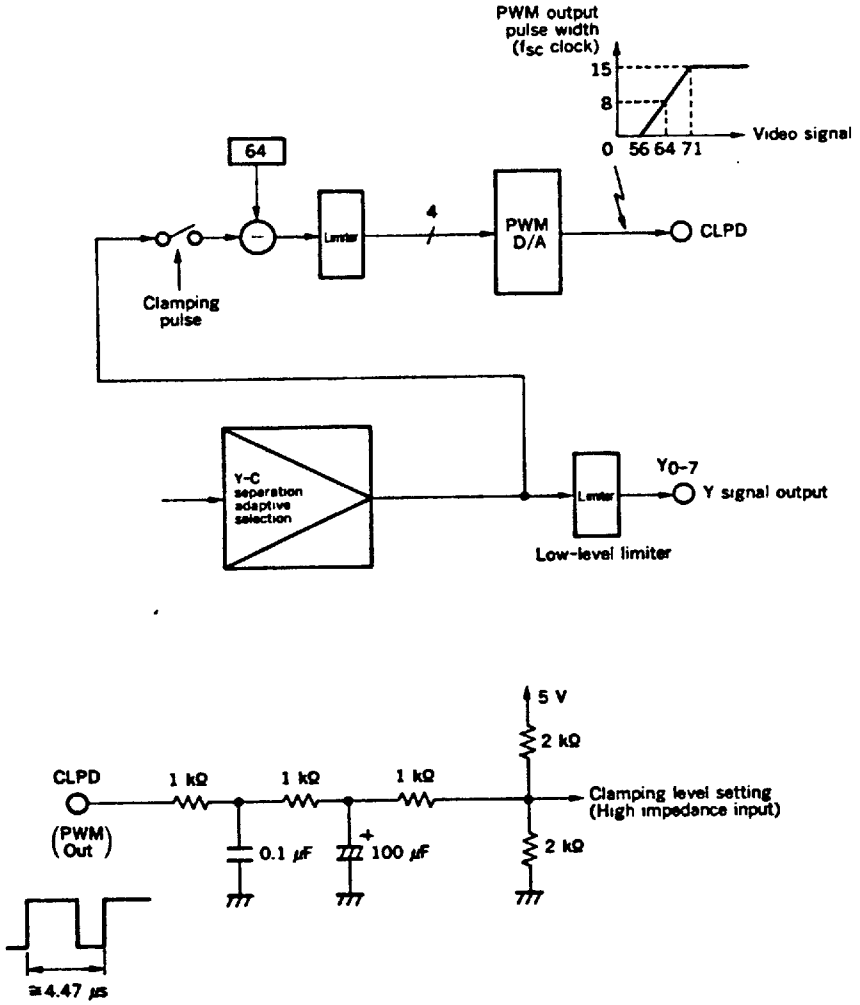


Fig. 2-2. Block Diagram of Clamping Level Feedback Loop

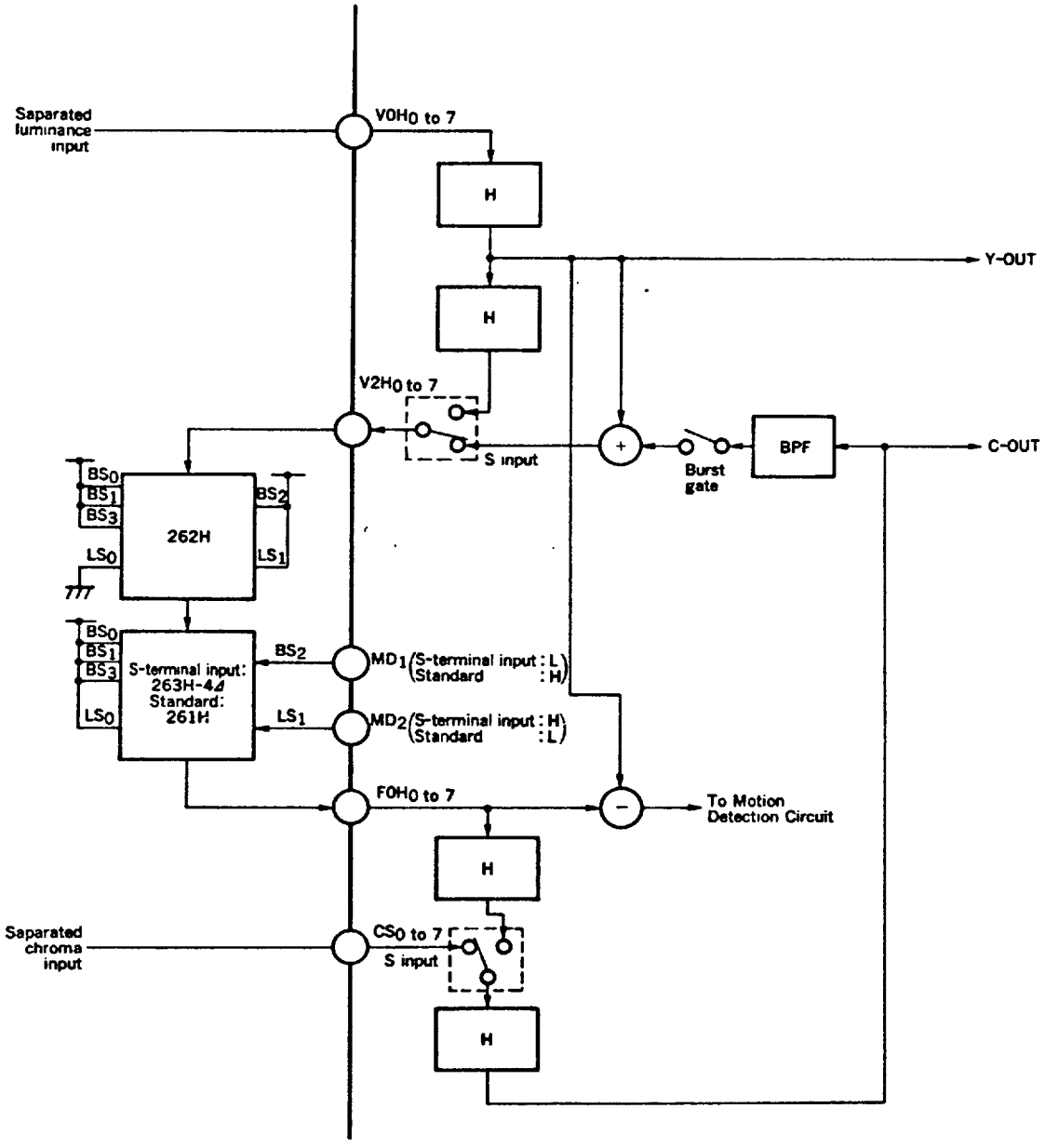


3. HANDLING OF S-TERMINAL INPUT

When the luminance signal and color signal which have been separated beforehand from the composite video signal are to be input, they can be handled by using the video input pin and the separated chroma input pins (CS_0 to CS_7). Because the luminance signal and color signal are input in the form of being separated from the composite video signal, they will be output without being subjected to Y/C separation in this LSI chip. Fig. 3-2 shows the flow of each signal in the S-terminal Input mode. In this mode, the delay length of the field buffer must be changed. This can be handled with the MD_1 and MD_2 pins. Switching between these pins is carried out with the serial bus.

In the S-terminal Input mode, set all the data of SA_7 and D_3 to D_0 to "1".

Fig. 3-1. Block Configuration in S-terminal Input Mode (with μPD42270 Used as Memory)



4. V-APERTURE COMPENSATION

This circuit is used to enhance the contour of an image in the vertical direction. The vertical edge component is detected with the secondary comb filter in the vertical direction and the color signal component and the oblique component of the luminance signal are removed with a low-pass filter. This signal is passed through the nonlinear processing section consisting of a coring circuit, a gain control circuit, and a limiter circuit and is added to the luminance signal on the main line.

In the limiter circuit, for a signal exceeding a certain level, the level of the signal is clipped to a fixed value or the signal may conversely be provided with an attenuation characteristic (x-1). The operating point of this clipping and the gain of the gain control circuit can be set with serial bus data. In the coring circuit, the level is fixed to 1.

(1) Coring circuit

This circuit subtracts 1 from the input signal, by which a dead band for one level is provided to prevent the degradation of S/N ratio.

(2) Limiter circuit

Signals requiring V-aperture compensation are more or less those with smaller levels. Uniform contour enhancement on signals with large levels may result in excessive contour enhancement. Therefore, by providing an attenuation characteristic to a signal whose level is exceeding a certain value, the level of contour enhancement is changed for signals with large levels. This level setting may be changed with serial bus data within the range of Level 0 to Level 127.

(3) Gain control circuit

This circuit changes the enhancement level of the vertical contour. This level setting may be changed with serial bus data in 8 steps within the range of 0 to 7/8 times the original level.

Fig. 4-1. V-Aperture Compensation Nonlinear Processing Characteristics

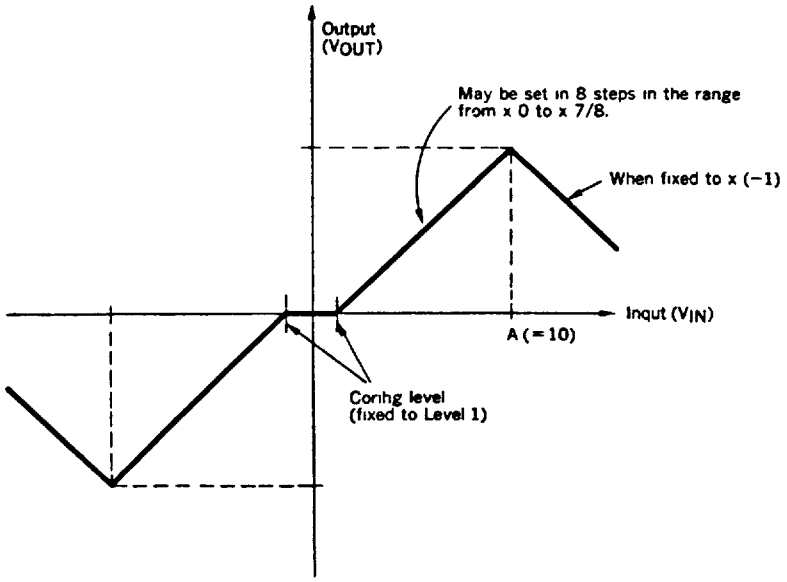
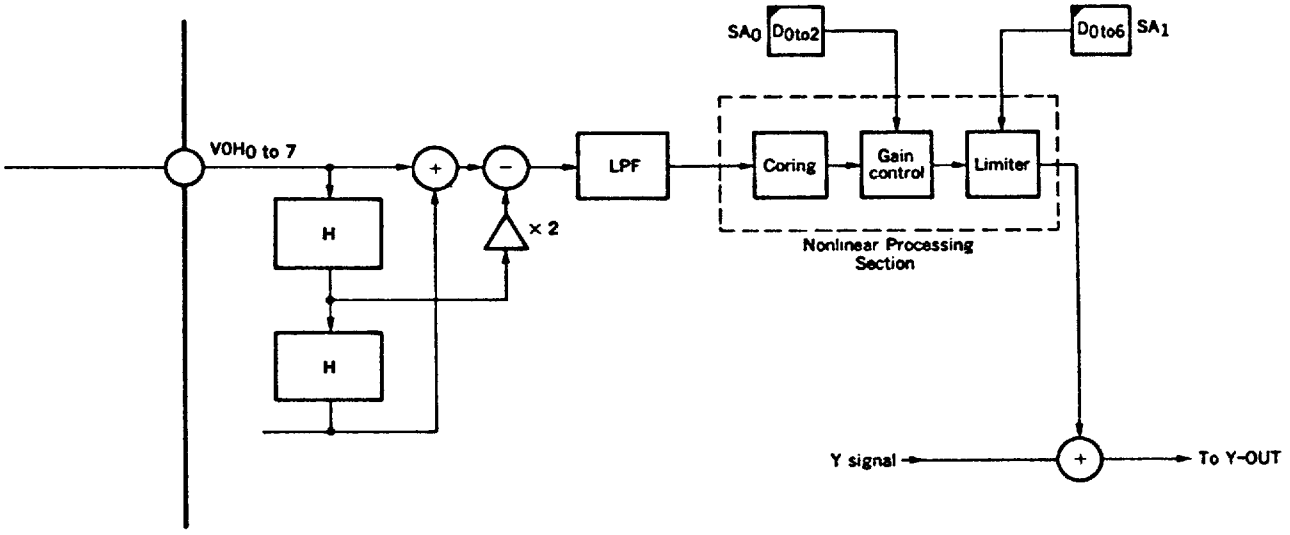


Fig. 4-2. Block Diagram of V-Aperture Compensation Circuit



5. SYNCHRONOUS PROTECTION

In this EDTV system, sync signals will be protected to the last. For this reason, a signal to protect the sync signal period is input from the BLK pin (Pin 36). While this BLK pin remains High, synchronous protection is carried out.

This BLK signal is supplied from the μPD9383 (TIG).

6. MOTION DETECTION

The μPD6480 has a function to identify whether the input signal is a still picture part of a moving picture part by detecting a one-frame-period differential signal in dot units and generates a motion signal according to the amount of motion. This motion detection function consists mainly of the following four blocks:

(1) Y differential detection circuit

This circuit detects a one-frame-period difference in the level between two luminance signals.

(2) C differential detection circuit

This circuit detects a one-frame-period difference in the level between two color signals.

(3) Motion coefficient generation circuit

This circuit generates a 4-bit motion signal which controls Y/C separation and Y interpolation from the Y differential and C differential.

(4) Motion signal extension circuit

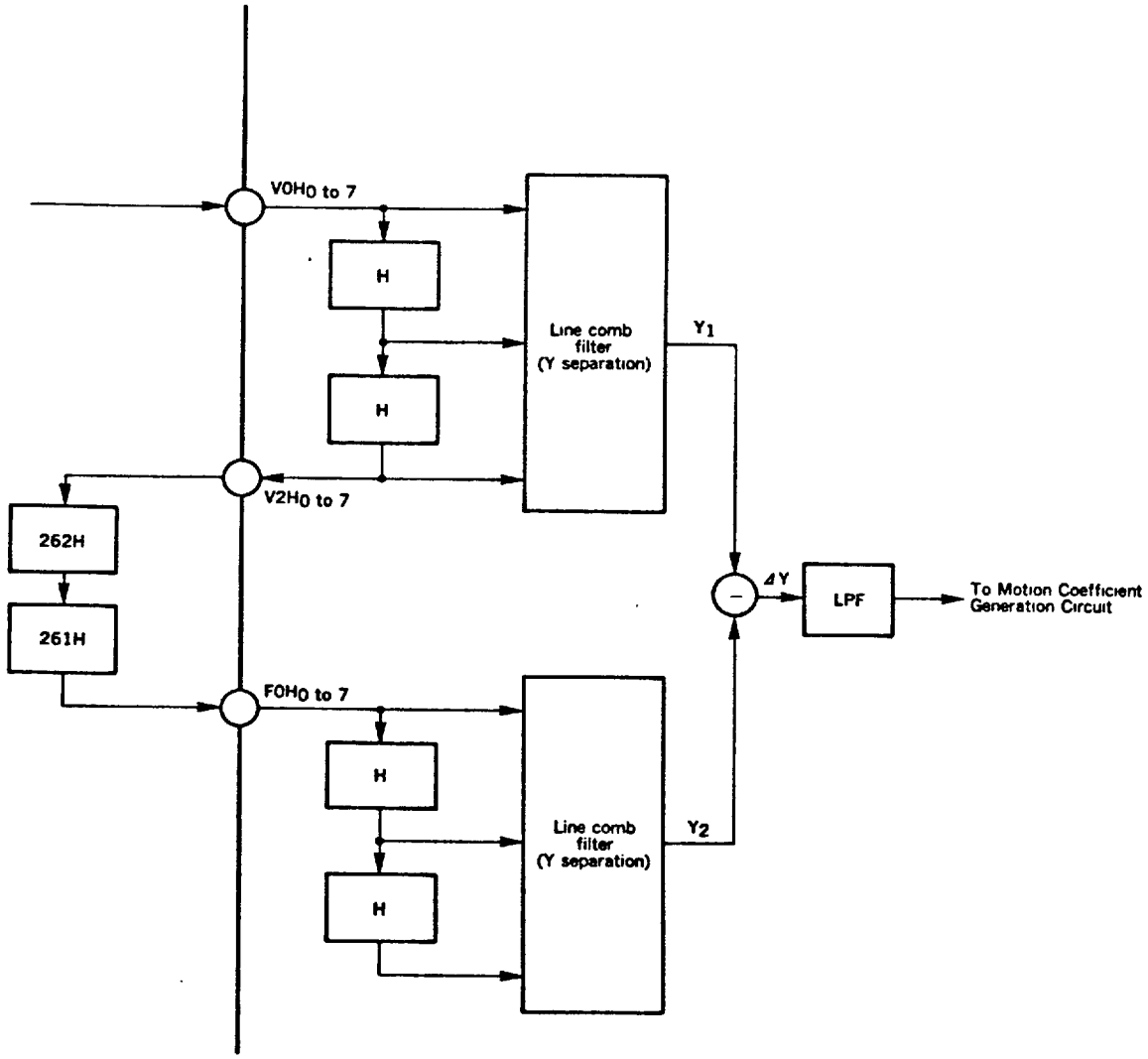
This circuit extends the motion signal generated by the motion signal generation circuit in the horizontal, vertical (line), and temporal (field) direction.

6.1 Y DIFFERENTIAL DETECTION CIRCUIT

By the differential detection circuit to detect a difference in level between the original luminance signal and the luminance signal arriving with a delay of one frame, a one-frame-period differential is taken to detect the frame differential ΔY of the luminance signal. In this case, if only the one-frame differential of the composite video signal is taken, the added signal 2C of the color signal will appear in addition to the ΔY component. This LSI chip has been devised to remove this 2C component as by installing secondary comb filters before the frame differential detection.

The ΔY component thus extracted is passed to the motion coefficient generation circuit after removing the high band component from it with a LPF.

Fig. 6-1. Y Differential Detection Circuit

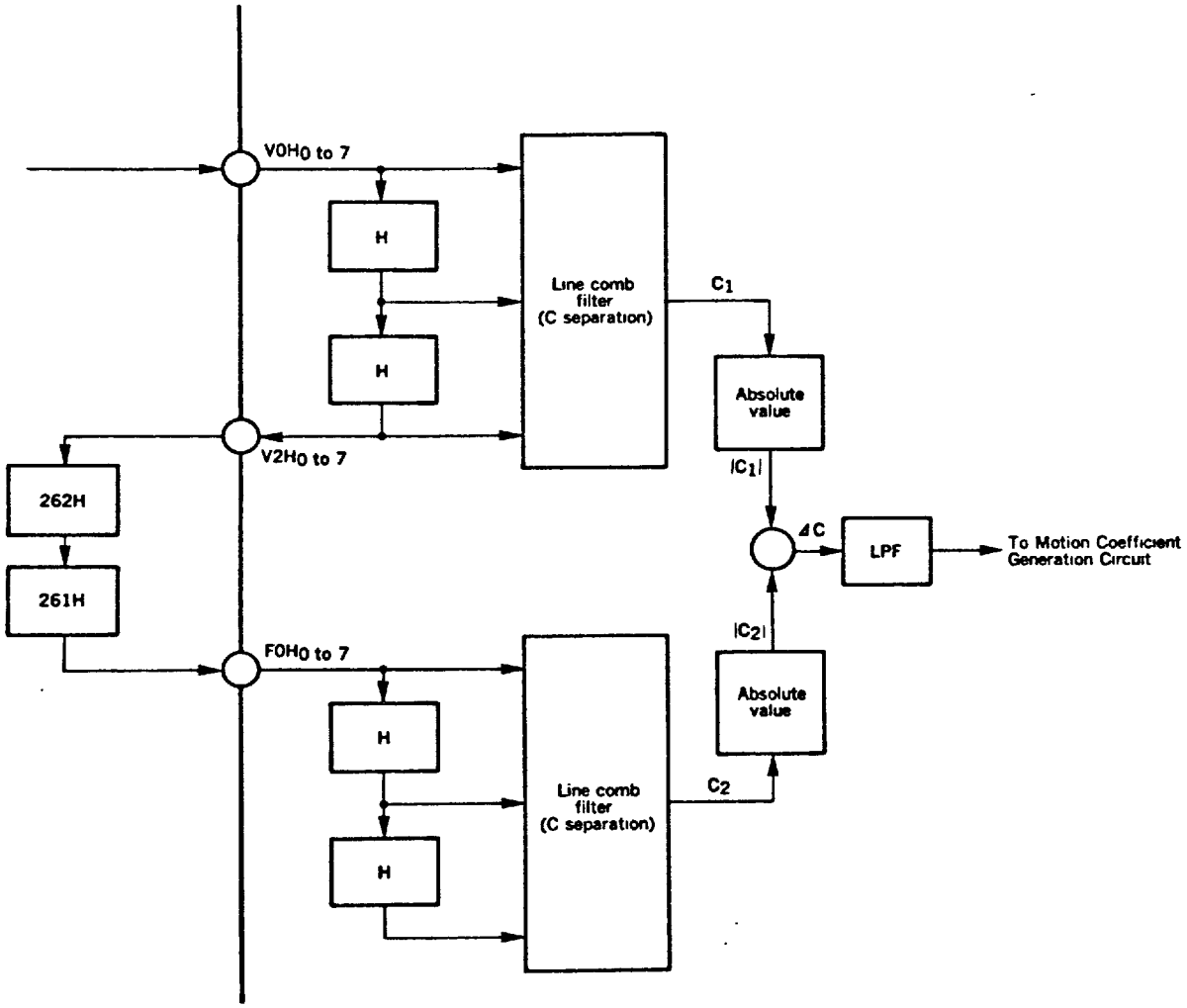


6.2 DIFFERENTIAL DETECTION CIRCUIT

By the differential detection circuit to detect a difference in level between the original color signal and the color signal arriving with a delay of one frame, a one-frame-period differential is taken to detect the frame differential ΔC of the color signal. The color signal is extracted beforehand by the secondary comb filters installed before the frame differential detection. This color signal takes an absolute value.

The ΔC component thus extracted is passed to the motion coefficient generation circuit after removing the high band component with a LPF.

Fig. 6-2. C Differential Detection Circuit



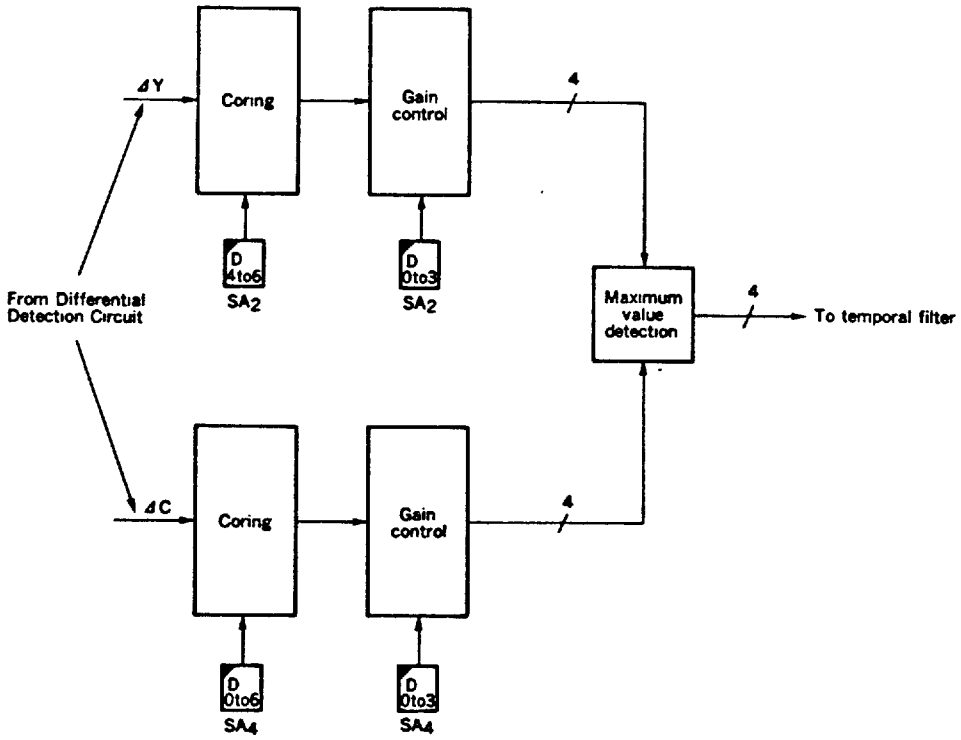
6.3 MOTION COEFFICIENT GENERATION CIRCUIT

This circuit generates a 4-bit motion signal for Y/C separation or Y interpolation from the Y differential (ΔY) and C differential (ΔC).

The luminance interframe differential signal from the Y differential detection circuit is first input to the coring circuit, in which a differential signal with a small level is removed. This coring level may be set with serial bus data. After the coring processing, the differential signal is input to the gain control circuit, in which the size of a motion signal is controlled. The output from the gain control circuit is processed through a limiter and becomes a 4-bit motion signal. The gain of the gain control circuit can be set with serial bus data. By changing this gain, the motion control sensitivity can be set. The color interframe differential signal from the C differential detection circuit is similarly processed.

Both the 4-bit luminance motion signal and the 4-bit color motion signal thus generated are input to the maximum value detection circuit and whichever is greater in level is output as a motion processing control signal. This output signal is input to the motion signal extension circuit for extension in the horizontal, vertical, and temporal directions.

Fig. 6-3. Motion Coefficient Generation Circuit



7. SERIAL BUS INTERFACE

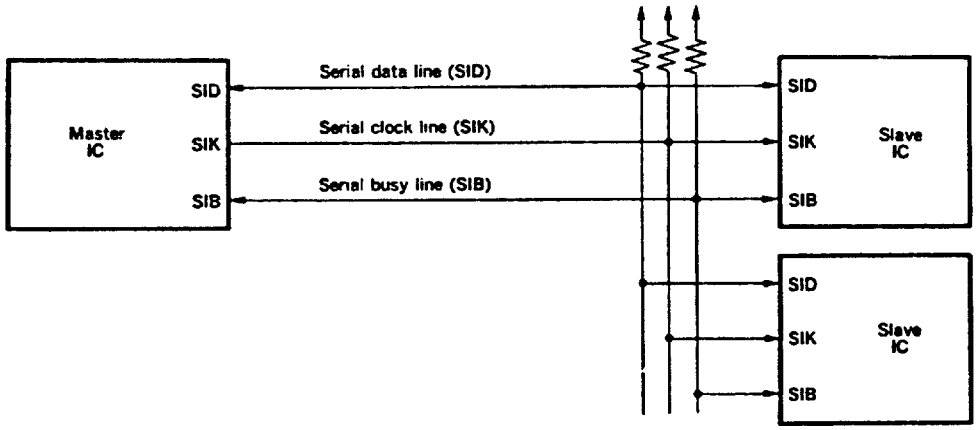
7.1 HARDWARE

The μPD6480 uses a serial bus which has three-wire system addresses. The serial bus consists of three lines.

(1) SID (Serial Data line)
The master CPU outputs serial data through this line in synchronization with the clock signal (SIK).

(2) SIK (Serial Clock line)
The master CPU outputs a serial clock through this line and the μPD6480 takes in the serial data in synchronization with this clock.

(3) SIB (Serial Busy line)
The master CPU outputs a busy signal through this line to operate the bus. When this line becomes Low, the μPD6480 starts receiving data. When this line becomes High, the internal circuits of the μPD6480 are forced to return to their initial states. In this case, however, the subaddress register inside the μPD6480 will not be initialized.



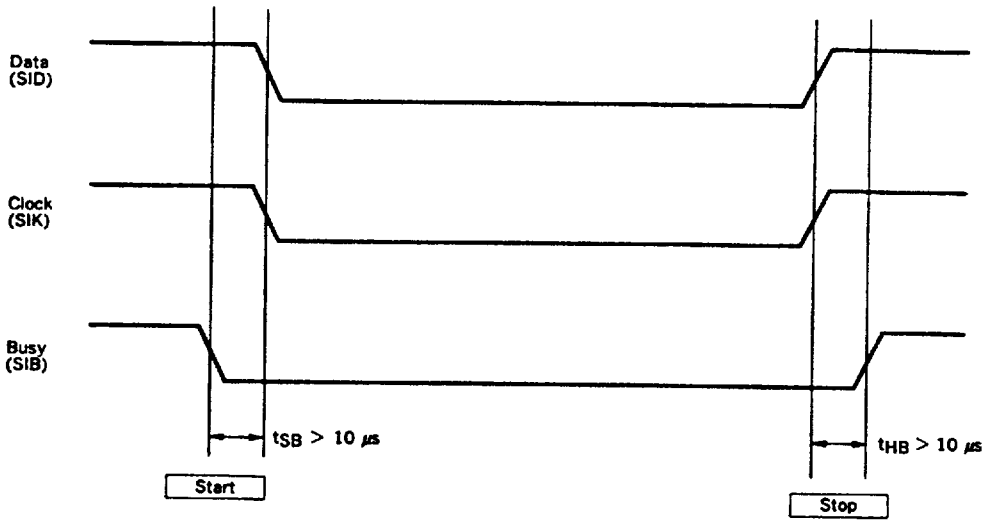
SID, SIK, and SIB are CMOS Schmitt inputs and are almost free from malfunctioning. The SIBO output is of the n-channel open drain configuration and can be also used by connecting it with SIB.

7.2 SOFTWARE SPECIFICATION

The master CPU controls the LSI chip connected to the serial bus as follows:

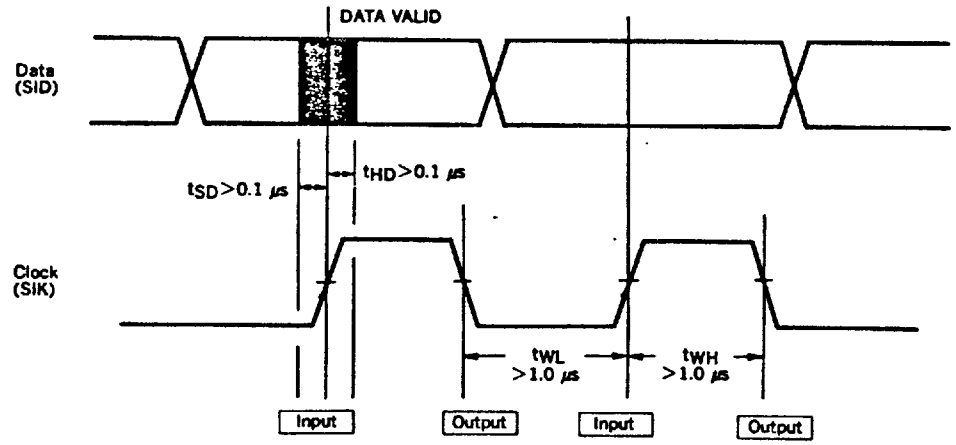
Start-up

To start up the serial bus, the master CPU first changes the state of the SIB (Serial Busy) line from High to Low. In this case, the SID (Serial Data) and SIK (Serial Clock) lines must stay in the High sate. If the SIB line is set to High, the serial bus will be forced to reset.



Data read/write (Write mode)

In the Write mode, serial data is taken in at the trailing edge of the SIK signal. Therefore, data switching at the master CPU should be performed at the trailing edge of the SIK signal.



Data transfer

One byte of data consists of a total of 10 bits: eight data bits, one parity bit, and one ACK (Acknowledge) bit.

To send one byte of data from the master CPU, three bytes (a main address byte, a subaddress byte, and a data byte) are required. However, because this LSI chip incorporates a function to automatically increment the subaddress byte counter, data bytes can be transmitted in succession.

Main address byte	Specifies the main address of each LSI chip to be selected by the master CPU.
Subaddress byte	Selects the subaddress byte and function address of each LSI chip selected by the master CPU with its main address.
Data byte	Transmits data in the selected function address.

The master CPU must add a parity bit to the 9th bit position of each byte data to be sent. Even parity is used for the parity check and parity must be selected so that the total number of 1s in the 9-bit data including the parity but becomes even.

The receiving LSI chip detects the parity bit. If the number of 1s in the data is even, it sets the SIBO (Serial Bus Busy Output) pin to "Low" at the 10th clock pulse. If the number of 1s is not even, the LSI chip stops receiving the subsequent data, holds the SIBO pin in the High Impedance state, and stops its internal operation until the next start-up of the serial bus.

Following the start-up of the serial bus, the master CPU first transmits the main address of the LSI chip to which data is to be sent, with a main address byte. The μPD6480 will be selected if "44_H" is specified as the main address.

If this main address is not the own address, the receiving LSI chip stops receiving data from the master CPU and stops its internal operation until the next start-up of the serial bus. If the main address is its own address, the LSI chip sends a Low level to the SIBO pin at the 10th clock pulse.

A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	P	ACK
"0"	"1"	"0"	"0"	"0"	"1"	"0"	"0"	"0"	"0"

μPD6480 ..... "44_H" (main address)

P : Parity
ACK : Acknowledge

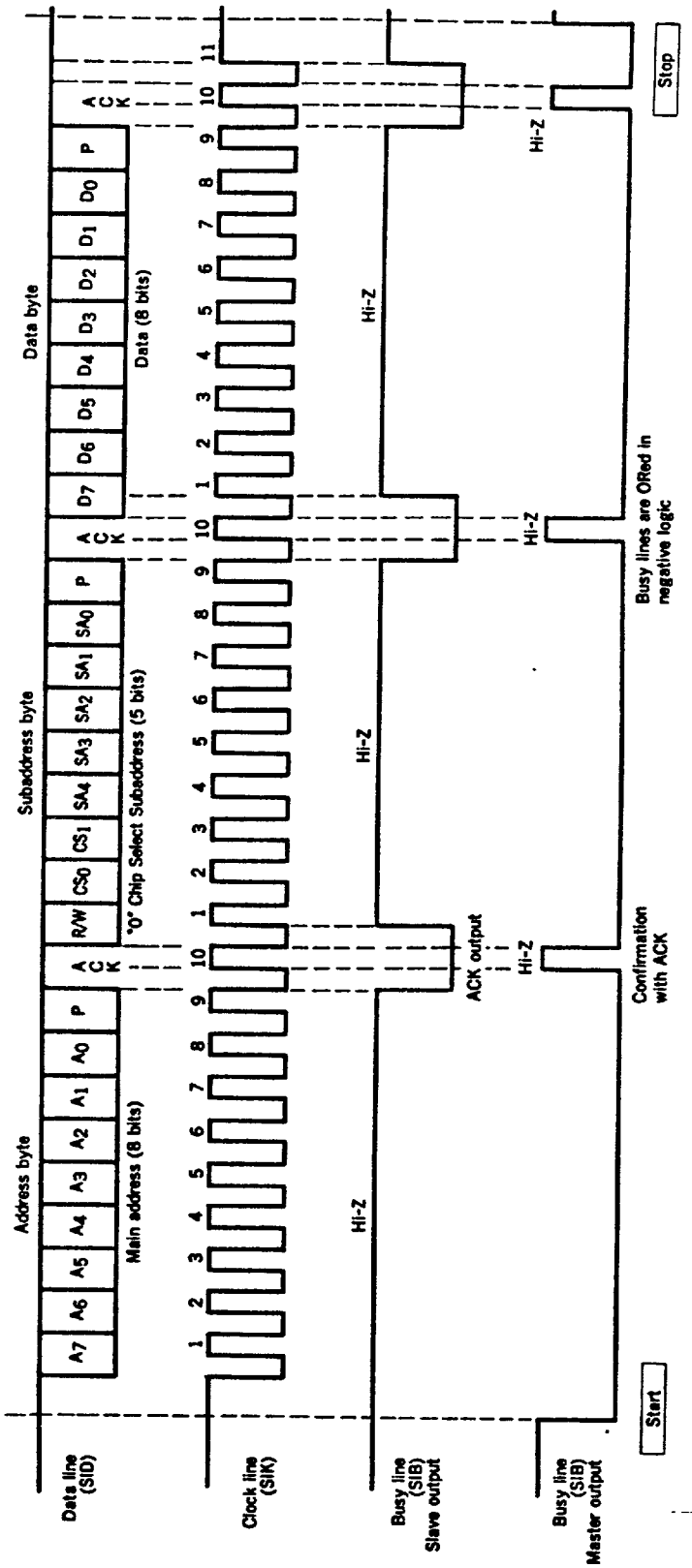
With one byte following the main address byte, specify the subaddress of the LSI chip selected by the main address byte.

The subaddress byte consists of 10 bits; one R/W bit, two Chip Select bits, five subaddress bits, one parity bit, and one acknowledge bit.

R/W bit	Specifies the transfer direction of the data following the subaddress byte. "L": Write mode (From master CPU to the specified LSI chip) "H": Read mode (From specified LSI chip to master CPU)
Chip Select bits	When two or more LSI chips having the same main address are connected, these two bits are used to select a specific chip. With the μPD6480, the Chip Select bits are not used. Therefore, set these bits as follows: $CS_0 = 0$, $CS_1 = 0$
Subaddress bits	Specify a function address within the LSI chip. When loading initial data, data can be written successively by setting the subaddress as "00_H" and using the subaddress increment function.

R/W	CS_0	CS_1	SA_4	SA_3	SA_2	SA_1	SA_0	P	ACK
"0"	"0"	"0"	"0"	"0"	"0"	"0"	"0"	"0"	"0"

Example of 1-byte data write (Write mode · · · · · Master IC writes one byte of data into Slave IC)



List of Serial Bus Functions (when applied to EDTV)

Sub address	Data							
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
SA_0	"0"	"0"	"0"	"0"	KILS Color killer select 1: Killer ON 0: Killer OFF	V-AP GAIN V-aperture gain 111: 7/8 to 000: 0/8 (OFF) D_2	D_1	D_0
SA_1	SYNCS Synchronous protect select 1: Sync not protected 0: Sync protected	V-AP INV V-aperture compensation inverting 1111111: Maximum aperture compensation to 0000000: No aperture compensation D_6	D_5	D_4	D_3	D_2	D_1	D_0
SA_2	"0"	DY COR ΔY coring level D_2	D_1	D_0	DY GAIN ΔY gain select 1111: 15/2 to 0000: 0/2 (OFF) D_3	D_2	D_1	D_0
SA_3	SVHS S-terminal input select 1111: S-terminal input 0000: Composite input				"0"	"0"	"0"	"0"
SA_4	"0"	DC COR ΔC coring level D_2	D_1	D_0	DC GAIN ΔC gain select 1111: 15/2 to 0000: 0/2 (OFF) D_3	D_2	D_1	D_0
SA_5	"0"	"1"	"0"	"0"	"0"	"0"	"0"	"0"
SA_6	"0"	MSTFS MS signal select 1: Extension 0: No extension	CFILS Chroma FIL select 1: Narrow band 0: Standard band	BPFS BPF select 1: BPF 0: Interline filter	MSD MS data 1: Interframe 0: Intra-field	MSC MS control 1: MSD control 0: Motion detection control	"0"	"1"
SA_7	"0"	"0"	"0"	"0"	"1"	"0" (1)	"0" (1)	"0" (1)
SA_8	"0"	"0"	"1"	"1"	"0"	"0"	"1"	"0"
SA_9	"0"	CGAIN Chroma output gain select 1: x 1/2 0: Normal	"0"	"1"	"0"	"1"	"0"	"1"
SA_A	FLOAT Floating select 1: Floating 0: Normal	"0"	"0"	"1"	"0"	"0"	"0"	"0"

List of Serial Bus Functions (when applied to 3-dimensional Y-C separation)

Sub address	Data							
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
SA_0	"0"	"0"	"0"	"0"	KILS Color killer select 1: Killer ON 2: Killer OFF	V-AP GAIN V-aperture gain 111: 7/8 to 000: 0/8 (OFF)		
						D_2	D_1	D_0
SA_1	SYNCS Synchronous protect select 1: Sync not protected 0: Sync protected	V-AP INV V-aperture inverting 1111111: Maximum aperture compensation to 0000000: No aperture compensation						
		D_6	D_5	D_4	D_3	D_2	D_1	D_0
SA_2	"0"	DY COR ΔY coring level			DY GAIN ΔY gain select 1111: 15/2 to 0000: 0/2 (OFF)			
		D_2	D_1	D_0	D_3	D_2	D_1	D_0
SA_3	SVHS S-terminal select 1111: S-terminal input 0000: Composite input				"0"	"0"	"0"	"0"
SA_4	"0"	DC COR ΔC coring level			DC GAIN ΔC gain select 1111: 15/2 to 0000: 0/2 (OFF)			
		D_2	D_1	D_0	D_3	D_2	D_1	D_0
SA_5	"0"	"1"	"0"	"0"	"0"	"0"	"0"	"0"
SA_6	"0"	MSTFS MS signal select 1: Extension 0: No extension	CFILS Chroma FIL select 1: Narrow band 0: Standard band	BPFS BPF select 1: BPF 0: Interline filter	MSD MS data 1: Interframe 0: Intra-field	MSC MS control 1: MSD control 0: Motion detection control	"0"	"1"
SA_7	"0"	"0"	"0"	"0"	"1"	"0" (1)	"0" (1)	"0" (1)
SA_8	"0"	"0"	"1"	"0"	"0"	"1"	"0"	"1"
SA_9	"0"	CGAIN Chroma output gain select 1: x 1/2 0: Normal	"0"	"1"	"0"	"1"	"0"	"1"
SA_A	FLOAT Floating select 1: Floating 0: Normal	"0"	"0"	"0"	"1"	"1"	"1"	"0"

7.3 SERIAL BUS ADDRESS

7.3.1 V-AP GAIN (V-Aperture Gain)

SA_0	0	0	0	0	X	D_2	D_1	D_0

The V-AP GAIN bits of subaddress SA_0 control the gain of the V-aperture compensation signal. If these three bits are set to "000", the V-aperture compensation signal will be turned off (0/8). If these bits are "111", the gain of the V-aperture compensation will become maximum (7/8). The gain of the V-aperture compensation signal may be controlled in 8 steps.

Step	D_2	D_1	D_0	GAIN
0	0	0	0	0
1	0	0	1	1/8
2	0	1	0	2/8
3	0	1	1	3/8
4	1	0	0	4/8
5	1	0	1	5/8
6	1	1	0	6/8
7	1	1	1	7/8

7.3.2 V-AP INV (V-Aperture Inverting)

SA_1	X	D_6	D_5	D_4	D_3	D_2	D_1	D_0

The V-AP INV bits of subaddress SA_1 set a point at which the gain of the V-aperture compensation signal starts to decline. If these seven bits are all set to "1", V-aperture compensation will become maximum. If these bits are all "0", V-aperture compensation will be turned off.
If this point is to be set as point A in Fig. 4-1, the V-aperture inverting point will become as calculated below assuming V_{IN} = 10 and G_V = 0.5.

V-AP INV = $(V_{IN}-1) \times (G_V + 1)$
= $(10-1) \times (0.5 + 1) \fallingdotseq 13$

7.3.2 KILS (Killer Select)

SA_0	0	0	0	0	D_0	X	X	X

The KILS bit of subaddress SA_0 specifies whether or not the composite video signal is to be directly output the Y-OUT pin without color signal separation. If this bit is set to "1", the color killer will operate.

"1" ..... Killer ON
"0" ..... Killer OFF (standard operation)

7.3.4 SYNCS (Synchronous Protect Select)

SA_1	D_0	X	X	X	X	X	X	X

The SYNCS bit of subaddress SA_1 specifies whether or not the synchronous part of the Y output is to be protected.
If this bit is set to "1", synchronous protection will not be provided irrespective of the presence or absence of the BLK (Blanking) signal.
If this bit is set to "0", signals above Level 48 will be limited to Level 48 during the non-blanking period.

7.3.5 SVHS (SVHS Select)

SA_3	D_3	D_2	D_1	D_0	0	0	0	0

Set all these four bits of subaddress SA_3 to "1" of the video signal from which Y and C signals have already been separated is to be input (S-terminal Input mode).

"1111" ..... S-terminal input

"0000" ..... Composite input

If the S-terminal Input mode is selected, set the D_0 to D_3 bits of subaddress SA_7 as follows:

D_3 = "1", D_2 = "1", D_1 = "1", D_0 = "1"

7.3.6 DY GAIN (ΔY Gain Select)

SA_2	0	X	X	X	D_3	D_2	D_1	D_0

The DY GAIN bits of subaddress SA_2 select the gain of the 4-bit interframe Y differential detection output.

Step	D_3	D_2	D_1	D_0	GAIN
0	0	0	0	0	0.0
1	0	0	0	1	0.5
2	0	0	1	0	1.0
3	0	0	1	1	1.5
4	0	1	0	0	2.0
5	0	1	0	1	2.5
6	0	1	1	0	3.0
7	0	1	1	1	3.5
8	1	0	0	0	4.0
9	1	0	0	1	4.5
10	1	0	1	0	5.0
11	1	0	1	1	5.5
12	1	1	0	0	6.0
13	1	1	0	1	6.5
14	1	1	1	0	7.0
15	1	1	1	1	7.5

By setting these four bits to "0000", the Y differential detection output can be turned off. By combining DY GAIN with DC GAIN, the MIX ratio of ΔY and ΔC may be changed.

7.3.7 DY-COR (Δ-Y Coring)

SA_3	0	D_2	D_1	D_0	X	X	X	X

The DY-COR bits subaddress SA_3 indicate whether or not the small signal level for interframe Y differential detection is to be cored. By this reference data, a small signal is regarded as noise and is nulified.

"111" ..... Maximum coring

"000" ..... Coring OFF

7.3.8 DC GAIN (Δ-C Gain Select)

SA_4	0	X	X	X	D_3	D_2	D_1	D_0

The DC GAIN bits of subaddress SA_4 select the gain of the 4-bit interframe C differential detection output.

Step	D_3	D_2	D_1	D_0	GAIN
0	0	0	0	0	0.0
1	0	0	0	1	0.5
2	0	0	1	0	1.0
3	0	0	1	1	1.5
4	0	1	0	0	2.0
5	0	1	0	1	2.5
6	0	1	1	0	3.0
7	0	1	1	1	3.5
8	1	0	0	0	4.0
9	1	0	0	1	4.5
10	1	0	1	0	5.0
11	1	0	1	1	5.5
12	1	1	0	0	6.0
13	1	1	0	1	6.5
14	1	1	1	0	7.0
15	1	1	1	1	7.5

By setting these four bits to "0000", the C differential detection output can be turned off. By combining DC GAIN with DY GAIN, the MIX ratio of ΔY and ΔC may be changed.

7.3.9 DC-COR (Delta-C Coring)

SA_4	0	D_2	D_1	D_0	X	X	X	X

The DC-COR bits of subaddress SA_3 indicate whether or not the small signal level for interframe C differential detection is to be cored. By this reference data, a small signal is regarded as noise and is nullified.

"111" ..... Maximum coring
"000" ..... Coring OFF

7.3.10 MSC (Motion Data Control)

SA_6	0	X	X	X	X	D_0	0	1

The MSC bit of subaddress SA_6 specifies whether or not the selection of a Y/C separation filter is to be directly controlled with serial bus data.
If this bit is set to "1", the internal motion signal data will be disabled, allowing Y/C separation to be controlled with the MSD bit of the serial bus.

"1" ..... Serial bus data
"0" ..... Internal data (standard)

7.3.11 MSD (Motion Data)

SA_6	0	X	X	X	D_0	X	0	1

The MSD bit of subaddress SA_6 specifies which of the Y/C separation filters is to be selected, interframe or intra-field filter.
By setting the MSC (Motion Data Control) bit of subaddress SA_6 to "1", the selection of a Y/C separation filter can be controlled with this data.
"1" ..... Interframe Y/C separation
"0" ..... Intra-field Y/C separation

7.3.12 BPFS (Band-Pass Filter Select)

SA_6	0	X	X	D_0	X	X	0	1

The BPFS bit of subaddress SA_6 selects the mode of intra-field Y/C separation.
"1" ..... Interline Y/C separation
"0" ..... BPF (Frequency separation type Y/C separation)

7.3.13 CFILS (Chroma Filter Select)

SA_6	0	X	D_0	X	X	X	0	1

The CFILS bit of subaddress SA_6 selects the chroma band characteristic of intra-field Y/C separation.
"1" ..... Narrow band
"0" ..... Standard band

7.3.14 MSTFS (Temporal Filter Select)

SA_6	0	D_0	X	X	X	X	0	1

The MSTFS bit of subaddress SA_6 specifies whether or not the temporal filter is to be used for the motion signal.
"1" ..... Use temporal filter.
"0" ..... Do not use temporal filter.

7.3.15 CGAIN (Chroma Output Gain Select)

SA_9	0	D_0	0	1	0	1	0	1

The CGAIN bit of subaddress SA_9 selects the gain of the chroma signal output.
If this bit is set to "0", the gain of the chroma signal output will be multiplied by 2 in the Composite Input mode or multiplied by 1 (will remain the same) in the S-terminal Input mode.
If this bit is set to "1", the gain of the chroma signal output will be multiplied by 1/2 in each mode.

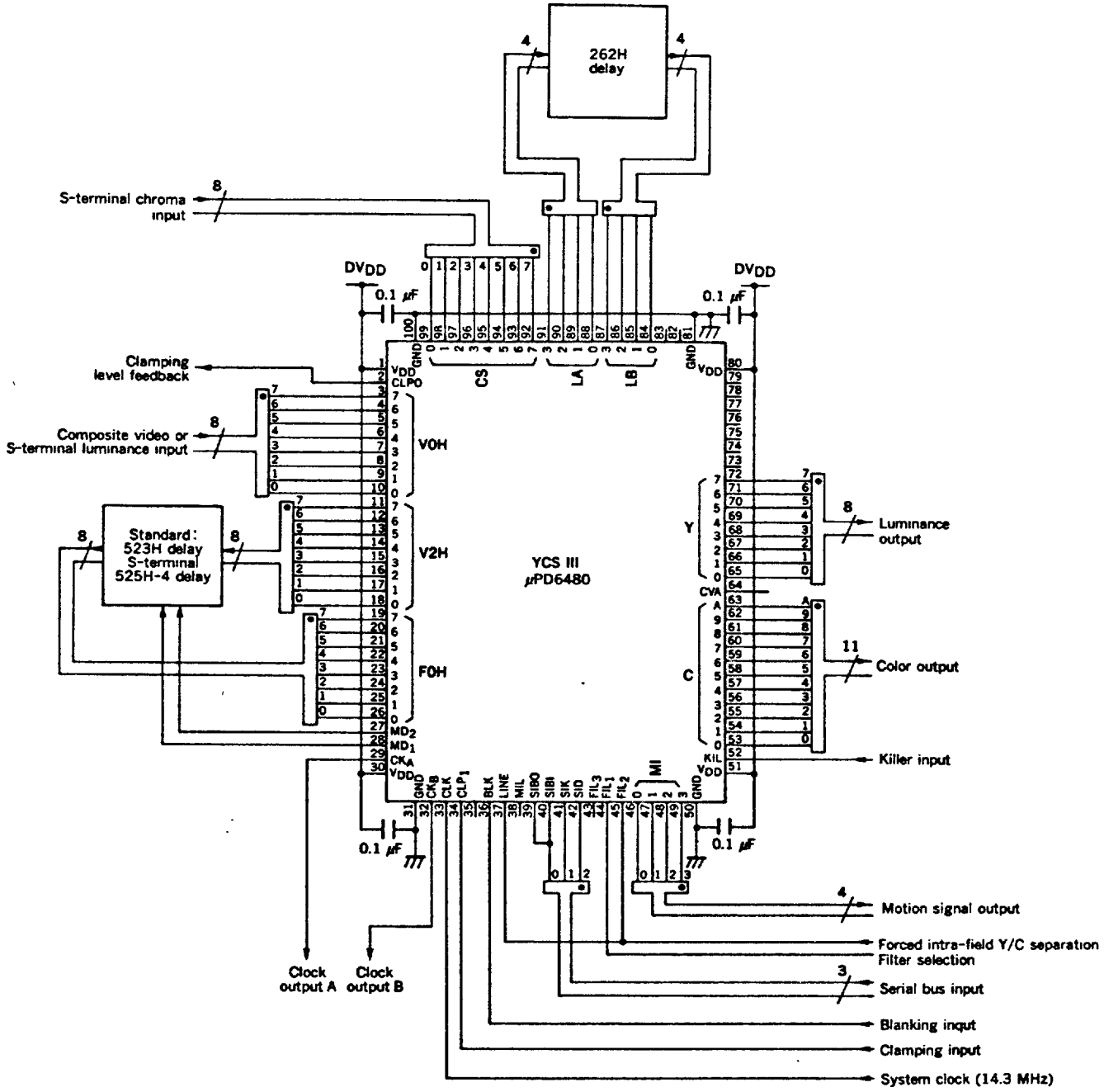
7.3.16 FLOAT (Floating Select)

SA_A	D_0	0	0	1	0	0	0	0

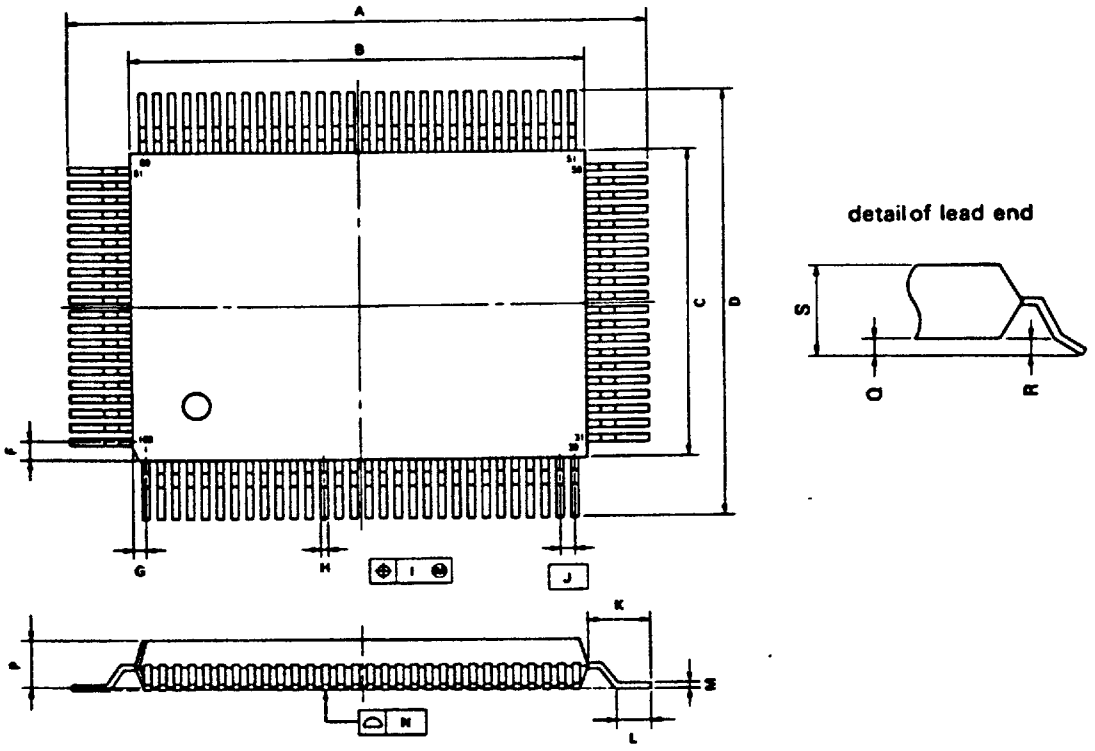
If the FLOAT bit of subaddrnss SA_A is set to "1", the following pins will be put in the High Impedance state and an external memory will be put in the floating state.
This bit allows an external memory to be used for a different purpose when the μPD6480 is not in use.

"1" ..... Puts $V2H_0$ to $V2H_7$, MD_1, MD_2, CK_A, CK_B, and LA_0 to LA_3 pins in High Impedance state.
"0" ..... Normal operation

μPD6480 APPLICATION CIRCUIT



100PIN PLASTIC QFP (14×20)



S100GF-65-3BA

NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	$23.2^{\pm 0.4}$	$0.913^{+0.017}_{-0.016}$
B	$20.0^{\pm 0.2}$	$0.795^{+0.009}_{-0.008}$
C	$14.0^{\pm 0.2}$	$0.551^{+0.009}_{-0.008}$
D	$17.2^{\pm 0.4}$	$0.677^{\pm 0.016}$
F	0.8	0.031
G	0.6	0.024
H	$0.30^{\pm 0.10}$	$0.012^{+0.004}_{-0.005}$
I	0.15	0.006
J	0.65 (T.P.)	0.026 (T.P.)
K	$1.6^{\pm 0.2}$	$0.063^{\pm 0.008}$
L	$0.8^{\pm 0.2}$	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.15	0.006
P	2.7	0.106
Q	$0.1^{\pm 0.1}$	$0.004^{\pm 0.004}$
R	$0.1^{\pm 0.1}$	$0.004^{\pm 0.004}$
S	3.0 MAX	0.119 MAX.