



NEC Electronics Inc.

**PRELIMINARY INFORMATION****Description**

The  $\mu$ PD70616 (V60) is a high-performance, second-generation 32-bit microprocessor designed for a wide range of applications including personal computers, engineering workstations, and industrial controllers. The V60 includes advanced features such as thirty-two 32-bit general-purpose registers and a powerful instruction set optimized for high-level languages and operating systems such as UNIX™ and MS-DOS®. The on-chip demand-paged memory management and floating point units further increase performance and design flexibility.

Performance in the  $\mu$ PD70616 is enhanced by pipelining internal operations such as instruction prefetch, instruction decode, address translation, and instruction execution. Software development and debugging is fully supported by instruction breakpoints, single-step traps, and address traps. Emulation mode allows porting of  $\mu$ PD70108/ $\mu$ PD70116 application software to run without modification and with the full protection of the demand-paged virtual memory system. The ability to execute software from the large established base of  $\mu$ PD70108/ $\mu$ PD70116 applications under a host operating system such as UNIX provides an upgrade path from 16-bit architectures yet preserves existing software investments.

**Features**

- 32-bit high-performance CMOS microprocessor
- Thirty-two 32-bit general-purpose registers
- On-chip demand-paged memory management unit
  - 4-gigabyte virtual address space
  - 2-level translation scheme (area/page)
  - 4 levels of protection
  - 16-megabyte physical address space
  - 16 entry translation lookaside buffer (TLB)
- Supported data types include
  - 8-, 16-, 32-, 64-bit integers
  - 32-, 64-bit floating point
  - 8-, 16-bit characters
  - Bit, bit field and bit string
- 21 powerful addressing modes plus bit addressing
- Context switching and operating system support
- V20™/V30™ emulation mode
- Flexible hardware debugging support
  - Breakpoints
  - Instruction trace
  - Address traps
- Functional redundancy monitor (FRM)

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**$\mu$ PD70616 (V60™)  
32-BIT VIRTUAL MEMORY  
CMOS MICROPROCESSOR**

T-49-17-32

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**Ordering Information**

Part Number	Package	Maximum Frequency
$\mu$ PD70616R	68-pin PGA	16 MHz

**Pin Identification**

Symbol	Function
A <sub>23</sub> -A <sub>0</sub>	24-bit address bus output
D <sub>15</sub> -D <sub>0</sub>	16-bit data bus I/O
ST2-ST0	Bus status output
MRQ	Memory request output
R/W	Read/write output
DS	Data strobe output
BCY	Bus cycle output
DL1-DL0	Data length output
FAS	First data access output
UBE	Upper byte enable output
READY	Ready input
BMODE (FRM)	Bus mode input Functional redundancy monitor
BLOCK (MSMAT)	Bus lock output Mismatch
BERR	Bus error input
BFREZ	Bus freeze input
RT/EP	Retry/exception input
NMI	Non-maskable interrupt input
INT	Interrupt input
HLDREQ	Hold request input
HLDACK	Hold acknowledge output
CPBUSY	Coprocessor busy input
RESET	Reset input
CLK	Clock input
VDD	Power
GND	Ground

UNIX is a trademark of AT&amp;T Bell Labs.

MS-DOS is a registered trademark of Microsoft Inc.

V20, V30, and V60 are trademarks of NEC Corporation.

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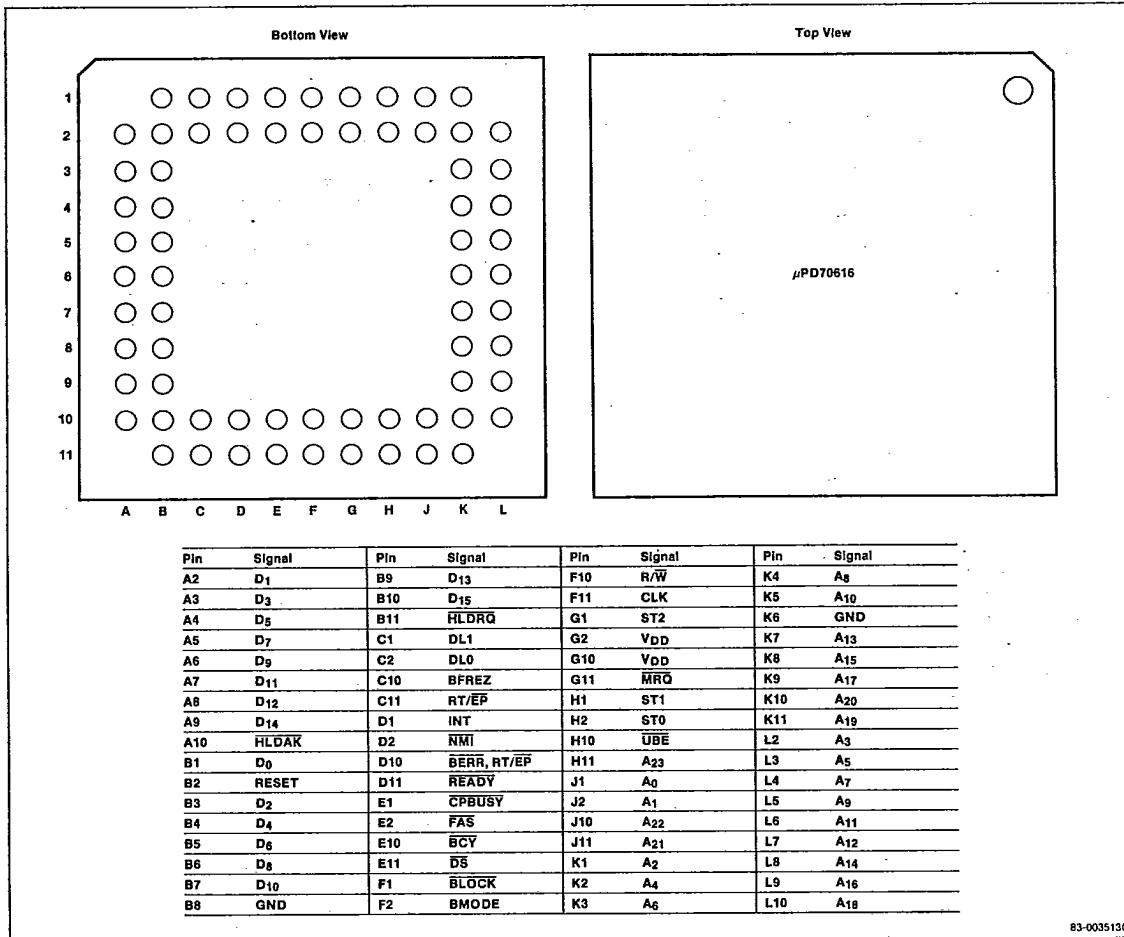
**μPD70616 (V60)**

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## **Pin Configuration**

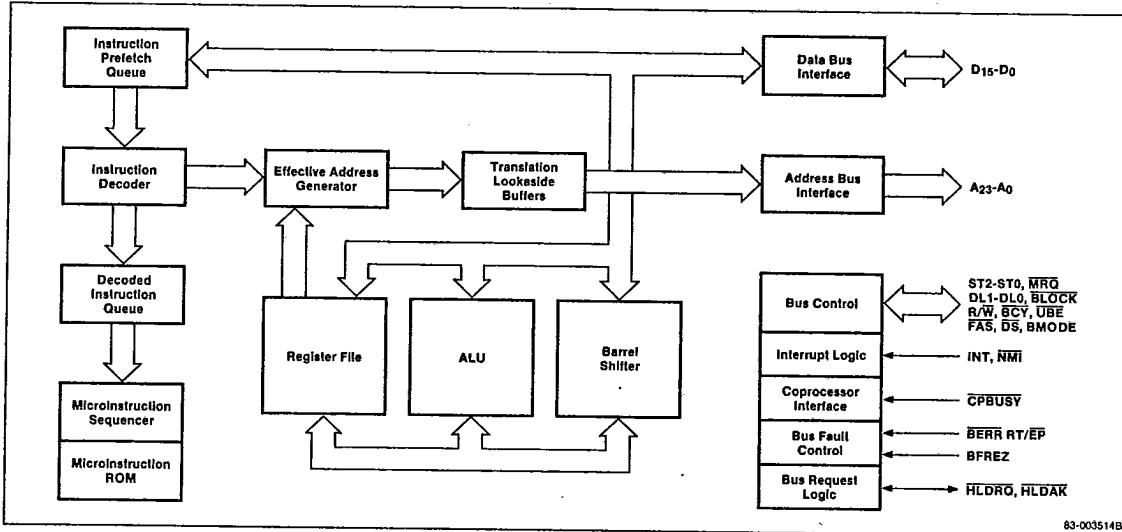


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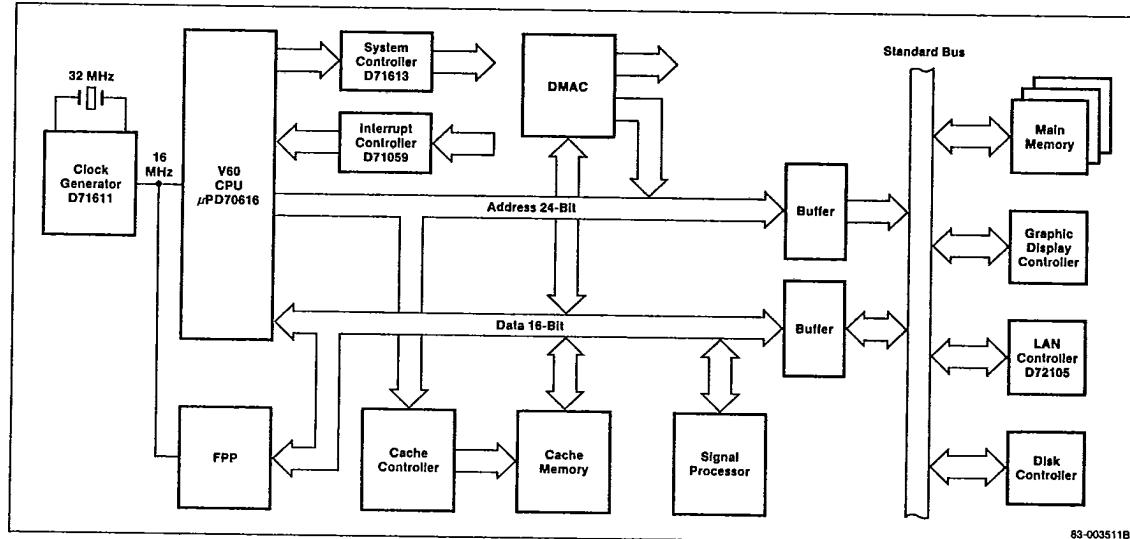
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**Block Diagram**

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**Applications****V60 CPU Design Example 1**

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