Preliminary

Am82520

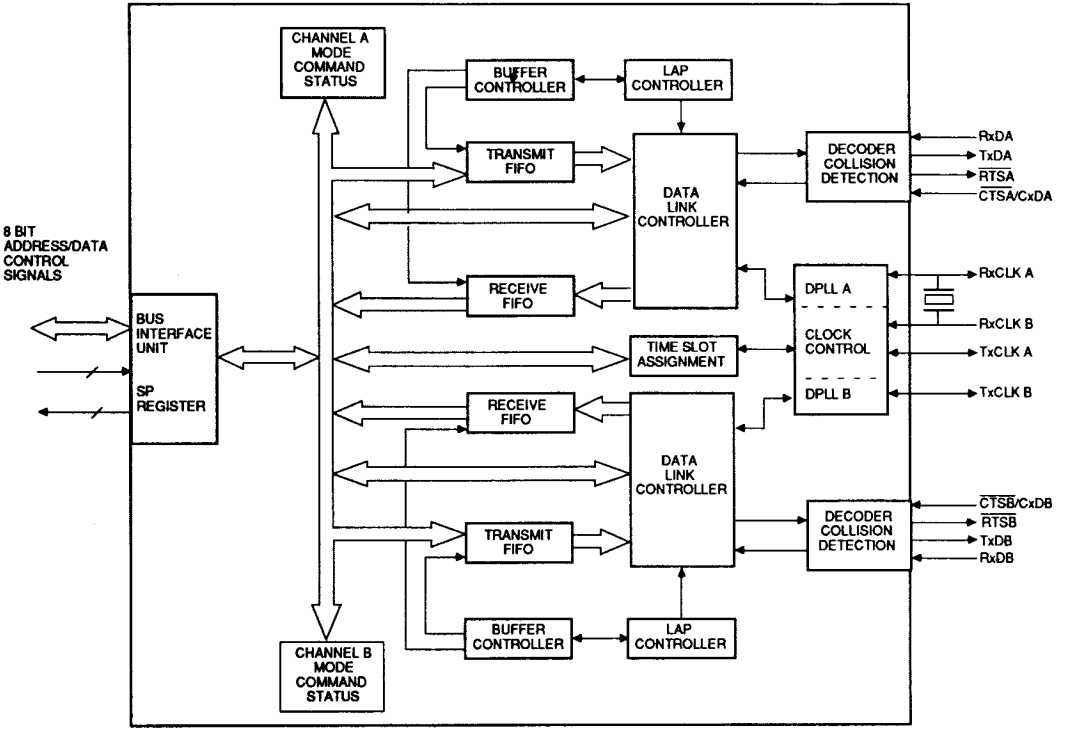
HSCC High-Level Serial Communications Controller

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- Two independent HDLC channels
- Implementation of X.25 LAPB/LAPD protocol
- Programmable timeout and retry conditions
- FIFO buffers for efficient transfer of data packets
- Digital phase locked loop for each channel
- Baud rate generator and oscillator
- Different modes for clock recovery and data encoding
- High-speed data rate (up to 4 MHz)
- Supports bus configuration by collision resolution
- Telecom-specific features programmable
- 8-bit parallel microprocessor interface
- Advanced CMOS technology
- Low power consumption;
  active: 25 mW at 4 MHz
  standby: 3 mW
- Package: 28-Pin Plastic or 28-Pin Plastic Leaded Chip Carrier
- Operating temperature 0 to +70°C
- Industrial: operating temperature –40 to +85°C

BLOCK DIAGRAM



Publication #	Rev.	Amendment
11138	B	& /1

Issue Date: May 1989

DISTINCTIVE CHARACTERISTICS (continued)

Support of Layer 2 Functions by HSCC

"Low-level" HDLC devices usually support various protocols. When applying the HDLC protocol, mainly bit-oriented functions such as bit stuffing, CRC check, flag, and address recognition are performed. The Am82520 has been especially designed to support the ISO HDLC protocol. In addition to the bit-oriented functions, the device provides a high degree of procedural support by evaluating the layer 2 control field. In this way the communications procedures are processed between the communications controllers and not between the processors. As a result, procedure handshaking is minimized. The processor, however, is informed of the status of the procedure. The dynamic load of the processor is thus largely reduced. To maintain cost effectiveness and flexibility, not all layer 2 functions have been implemented in hardware. Instead, functions such as connection setup, cleardown, and error recovery errors are performed by the processor software.

Operating Modes

The distribution of functions between the HSCC and CPU applies to the auto mode. As a prerequisite for this operating mode, the window size has been limited to 1. Alternatively, transparent modes can be applied where the data field as well as the layer 2 headers are forwarded directly to the CPU. In these modes of operation the reception and transmission of messages is fully controlled by the CPU. This operating mode is selected when the component is used as a central station (master) or in the case where the window size is larger than 1. Furthermore, there is a possibility of bypassing the receiver and having direct access to the received data.

FIFO Buffers for Efficient Transfer of Data Packets

Another feature of the Am82520 can be seen in the buffers that are used for temporary storage of data packets which are transferred between the serial communication interface and the parallel system bus. Due to the overlapping input/output operation (dual-port behavior), the maximum length of the data packets is not limited by the buffer size. The dynamic load of the processor is reduced by transferring the data packets block by block.

Each channel on the HSCC incorporates a 64-byte FIFO buffer per direction. Each FIFO is divided into two memory pools of 32 bytes each. When a pool is filled (receive mode) or emptied (transmit mode) via the serial interface, the HSCC switches pools and the processor is prompted via an interrupt to read or write this pool. Subsequently, the second pool is filled or emptied. During this time the CPU can transfer the first block, ensuring availability of the pool. With a serial transfer rate of 1 Mbps, the reaction time between the first prompting and data overflow without loss of data is 256 µs. In addition, the transmit FIFO provides the flexibility for temporarily storing blocks of various lengths, which can then be transmitted in rapid succession. The receive FIFO can also store a data packet when a preceding short data packet (32 bytes) stored in the FIFO has not yet been read by the processor.

The HSCC is especially suitable for cost-critical applications with single-chip processors due to its memory organization and on-chip memory control.

Move string commands can be used in high-performance applications where fast data rates at the communication interface and a high level of processor performance is required. The FIFO contents can then by addressed by automatically incrementing the address.

GENERAL DESCRIPTION

The Am82520, High-Level Serial Communications Controller (HSCC), has been designed to free the user from tasks occurring in communication with networks and trunk lines. It is an X.25 LAPB/LAPD controller which to a large degree performs communication procedures independent of CPU support.

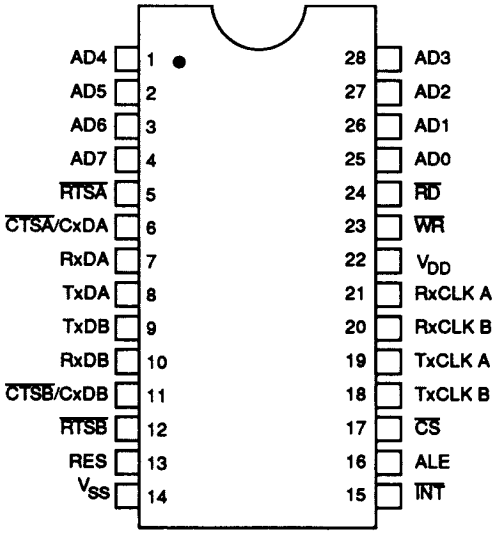
A parallel processor bus constitutes the microprocessor system. The serial communications interface consists of two full-duplex HDLC channels that can be operated independently from one another. The HSCC is connected to the transmission line by additional line drivers or modems. The need for external hardware is reduced because of added functions on-chip. The functions incorporated include an oscillator, DPLL (one per channel), programmable baud rate generator, and time slot assigner.

The chip contains a serial interface for two channels including a DPLL and collision-detection block, a data-link controller, and FIFO buffers. The microprocessor interface, including the status and command registers, is used for both channels. The HSCC is implemented in a 2 micron CMOS technology.

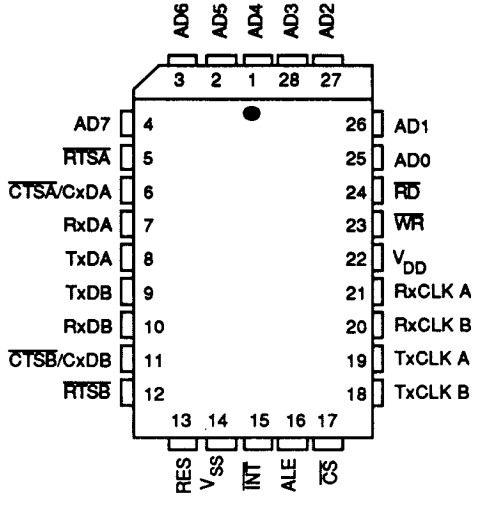
CONNECTION DIAGRAMS

Top View

28-Pin DIP

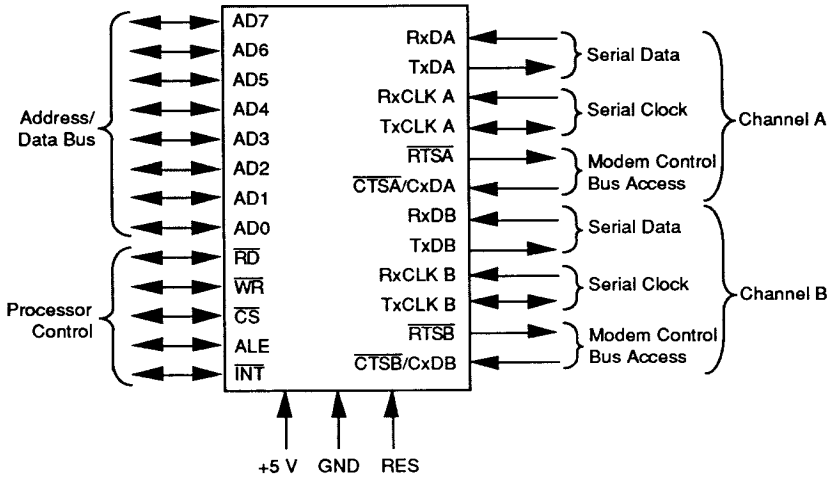


28-Pin PLCC



Note: Pin 1 is marked for orientation

LOGIC SYMBOL

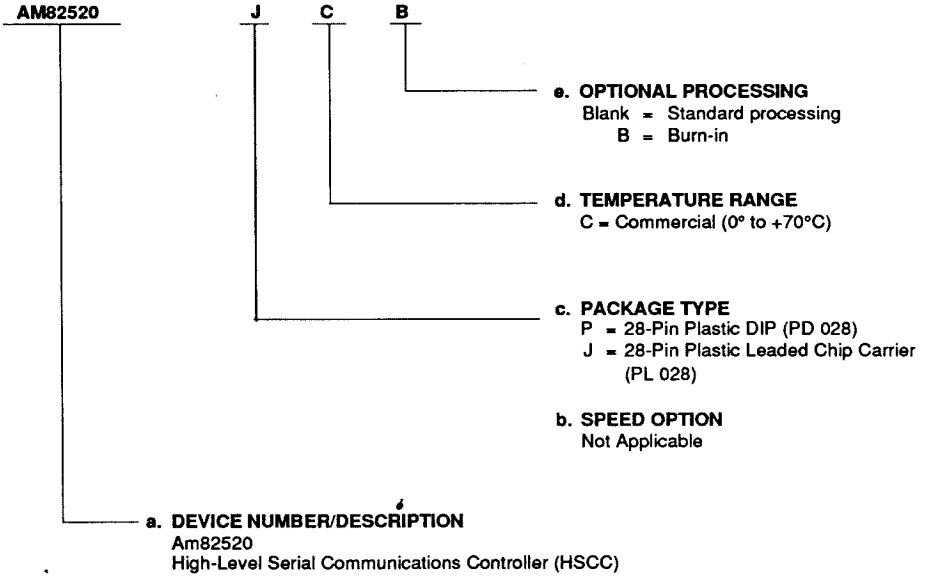


ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM82520	PC, JC PCB, JCB

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

PIN DESCRIPTION

AD0-AD7
Address Data Bus (Input, Output)
The multiplexed address data bus transfers data and commands between the microprocessor and the HSCC.

ALE
Address Latch Enable (Input)
A High on this line indicates an address on the external address data bus, selecting one of the HSCC's internal sources or destinations.

$\overline{CS}$
Chip Select (Input)
A Low on this signal selects the HSCC for a read/write operation.

$\overline{CTSA}$/CxDA, $\overline{CTSB}$/CxDB
Clear to Send/Collision Data (Input)
A Low on these inputs enables the respective transmitter. If the transmitters are always enabled, $\overline{CTS}$ should be connected to V_{SS}. In a bus configuration the external serial bus must be connected to the respective C x D pin.

$\overline{INT}$
Interrupt Request (Output)
This Signal is activated when the HSCC reqeusts an interrupt. It is an open-drain output.

$\overline{RD}$
Read (Input)
This signal indicates a read operation.

RES
Reset (Input)
A High on this input forces the HSCC into the reset state. The HSCC is in power-down mode during reset and in power-up mode after reset. The minimum pulse length is 1.8 µs.

$\overline{RTSA}$, $\overline{RTSB}$
Request to Send (Output)
When the RTS bit in Mode is set, the $\overline{RTS}$ signal goes Low. When the RTS bit is reset, the signal goes HIGH if the transmitter has finished and there is no further request for a transmission. In a bus configuration, $\overline{RTS}$ goes Low during the actual transmission of a frame shifted by a clock period, excluding collison bits.

RxCLKB, RxCLKA
Receive Clock (Input)
These pins can be programmed in several different modes of operation. In each channel RxCLK may supply the receive clock, the receive and transmit clock, the clock for the baud rate generator, or the clock for the DPLL. They also can be programmed for use as a crystal oscillator.

RxDA, RxDB
Receive Data (Input)
These input lines receive serial data at standard TTL or CMOS levels.

TxDA, TxDB
Transmit Data (Output)
These output lines receive serial data at standard TTL or CMOS levels. They can be programmed as push-pull or open-drain outputs.

TxCLKB, TxCLKA
Transmit Clock (Input/Output)
These pins can be programmed in several different modes of operation. TxCLK may supply the transmit clock for the respective channel, a receive strobe signal (TxCLKA) and a transmit strobe signal (TxCLKB) or a frame synchronization signal (TxCLKA, clock mode 5). Programmed as outputs, TxCLK may be used to supply the transmit clock fo the respective channel or as a tristate signal, indicating the programmed transmit time slot (TxCLKB, clock mode 5).

V_{DD}
Power
+5 V power supply.

V_{SS}
Ground (0 V)

$\overline{WR}$
Write (Input)
This signal indicates a write operation.

APPLICATIONS

In a point-to-multipoint or multimaster configuration, the HSCC can be used as a central station (master) or a peripheral station. As a peripheral station the HSCC can initiate the transmission of data. An internal function block provides for collision avoidance, which may occur if several stations start the transmitting simultaneously.

In a special operating mode the HSCC can transmit or receive data packets in programmable time slots. This makes the Am82520 especially suitable for applications in systems designed for packet switching and digital PABX applications. In the digital PABX application in particular, the integrated collision-resolution mechanism provides an optimal utilization of internal PCM paths.

Serial Interface

The serial interface provides two independent, high-performance communication interfaces. As already mentioned, the ISO HDLC layer 2 protocol is supported by the HSCC. In addition, layer 1 functions are provided by means of on-chip circuits. Eight different operating modes can be selected to clock the serial data stream.

In the power-down mode, all internal clocks as well as the oscillator circuitry are disabled.

- During the self-clocked operating mode, the transmit clock is recovered from the received data stream by means of an external crystal only. The on-chip DPLL samples the received bit stream and adjusts the clock edge to the center of the data bit.
- The bit stream is synchronized in the externally clocked operation mode by external clock signals. On the whole, four different clock signals separated by direction and channel, can be forwarded.
- In addition to the data clock, an externally supplied strobe signal can be applied to determine the time period during which data is to be received or transmitted. Using another operating mode, a time slot (up to 64) can be programmed for transmitting data and another time slot for receiving data. One time slot consists of eight clock cycles.
- With the point-to-multipoint configuration, comprising a central station (master) and several peripheral stations (slaves), data transmission can be initiated

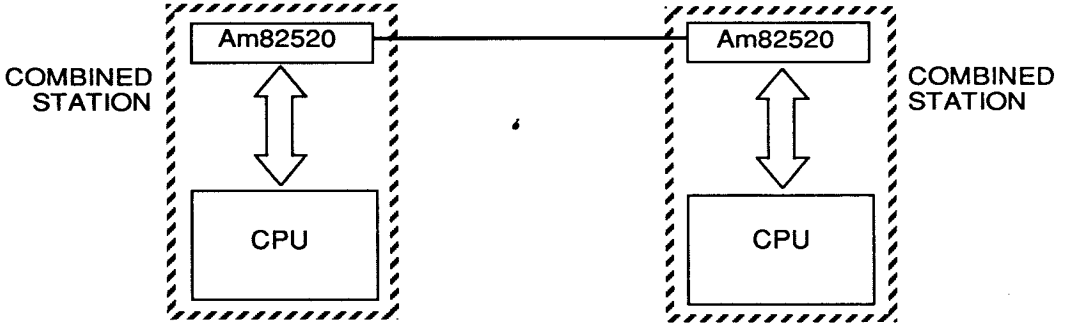


Figure 1. Point-to-Point Configuration

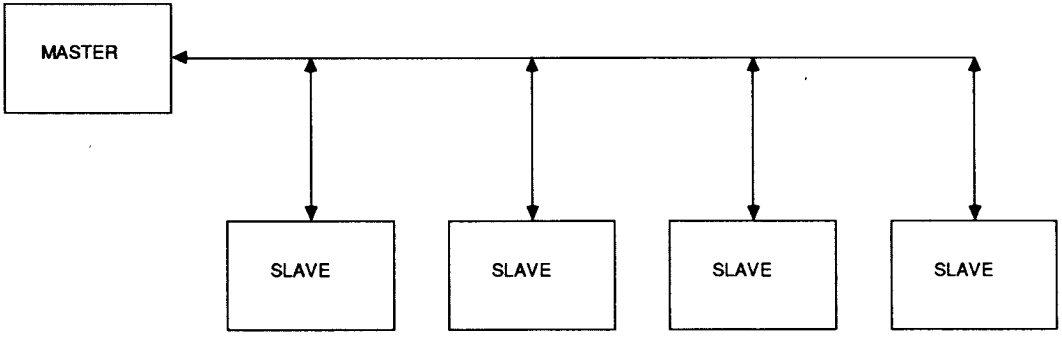


Figure 2. Point-to-Multipoint Configuration

by a slave. If several stations (slaves) transmit data simultaneously, the bus is assigned to one station by a collision-resolution procedure implemented by the HSCC. The bus assignment functions in accordance with the principle applied with the ISDN S interface. Its collision-resolution procedure helps to ensure a sharing of priority among the slave stations.

- The maximum data rate of the externally clocked operating mode is 4 Mbps. In the self-clocked operating mode with an external reference clock or crystal oscillator where the maximum clock rate is 12 MHz, the maximum data rate will be 750 Kbps.

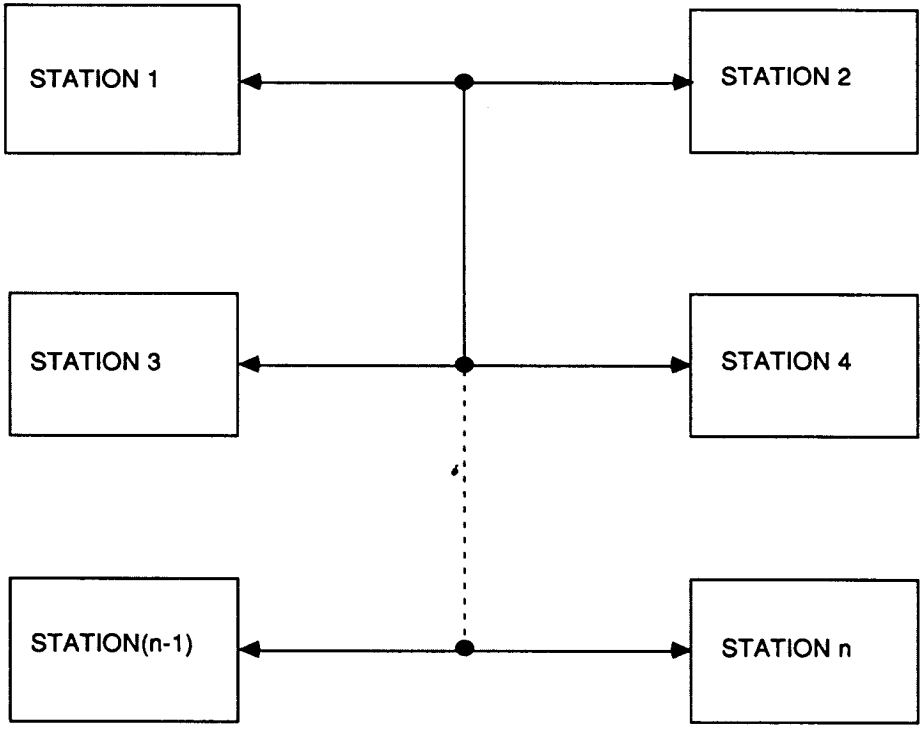


Figure 3. Multimaster Configuration

Absolute Maximum Ratings

Storage temperature (T_{stg})	−65°C to +125°C
Operating temperature: Am82520 (T_A)	0°C to +70°C
Voltage at any pin vs. ground (V)	−0.4 V_{DD} + 0.4 V

DC CHARACTERISTICS

Am82520: T_A = 0 to +70°C; V_{DD} = 5 V ± 10%; V_{SS} = GND = 0 V

Parameter		Test Conditions	Min.	Typical	Max.	Unit
Input Low voltage	V_{IL}		V_{SS}−0.4		0.8	V
Input High voltage	V_{IH}				V_{DD} +0.4	V
Output Low voltage	V_{OL}	I_{OL} = +2 mA			0.45	V
Output High voltage	V_{OH}	I_{OH} = −400 µA	2.4			V
		I_{OH} = −100 µA	V_{DD}−0.5	V_{DD}		V
Input leakage current	I_{IL}	V_{IN} = V_{DD} to 0 V	−10		+10	µA
Output leakage current	I_{OL}	V_{OUT} = V_{DD} to 0 V	−10		+10	µA
V_{DD} supply current						
Inactive	I_{CC}			0.5		mA
Active	I_{CC}	V_{DD} = 5 V t_{CP} = 4 MHz Inputs at V_{SS}/V_{DD} No output loads		5	7	mA

CAPACITANCE

T_A = +25°C; V_{DD} = GND = 0 V

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
Input capacitance	C_{IN}	f_c = 1 MHz		5	10	pF
Input/output capacitance	$C_{I/O}$			10	20	pF
Output capacitance	C_{OUT}	Unmeasured pins returned to GND		8	15	pF

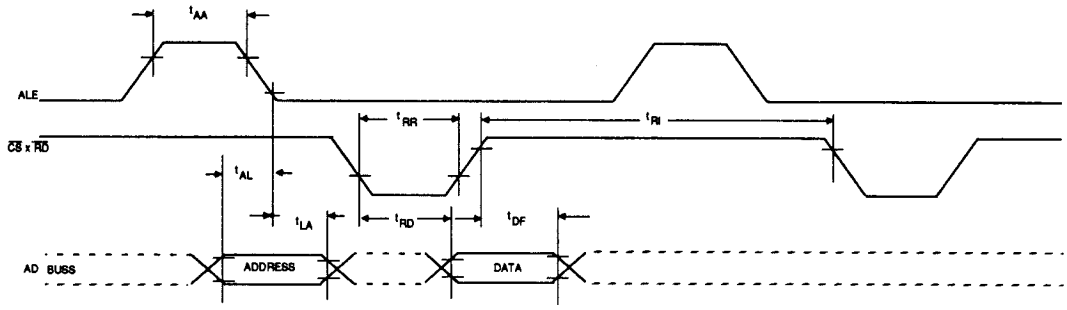


Figure 4. Read Cycle

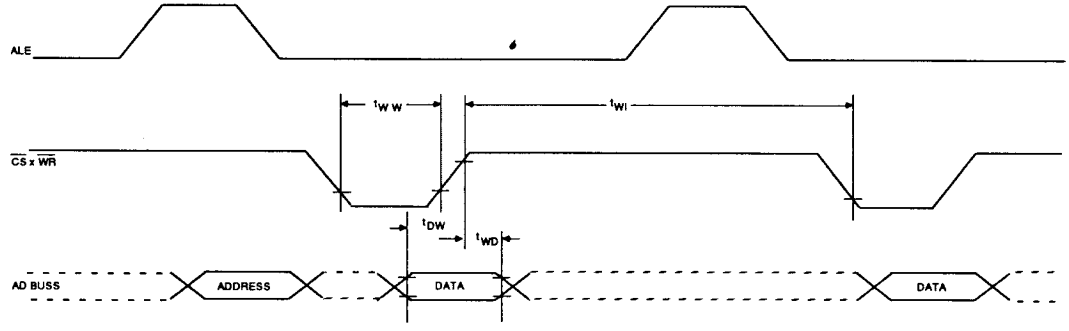


Figure 5. Write Cycle

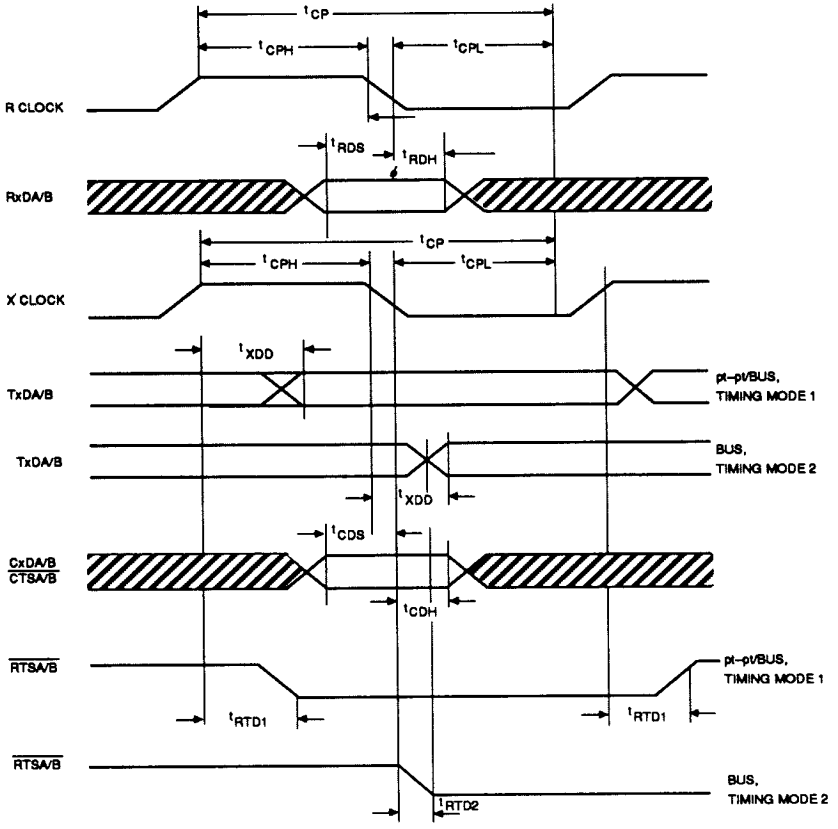
Read Cycle

Parameter		Min.	Max.	Unit
Address hold after $\overline{ALE}$ Low	t_{LA}	25		ns
Address to $\overline{ALE}$ Low setup	t_{AL}	20		ns
Data delay from $\overline{RD}$ Low	t_{RD}		110	ns
$\overline{RD}$ pulse width	t_{RR}	110		ns
Output float delay	t_{DF}		25	ns
$\overline{RD}$ control interval	t_{RI}	60		ns
$\overline{ALE}$ pulse width	t_{AA}	50		ns

Write Cycle

Parameter		Min.	Max.	Unit
$\overline{WR}$ pulse width	t_{WW}	60		ns
Data setup to $\overline{WR}$ High	t_{DW}	30		ns
Data hold after $\overline{WR}$ High	t_{WD}	10		ns
$\overline{WR}$ control interval	t_{WI}	60		ns

SERIAL INTERFACE TIMING



Serial Interface Timing

SWITCHING CHARACTERISTICS

Am82520: T_A = 0 to +70° C; V_{DD} = 5 V ± 10%; V_{SS} = GND = 0 V
T_A = –40 to +85° C; V_{DD} = 5 V ± 5%; V_{SS} = GND = 0 V

Parameter		Min.	Max.	Unit
Receive data setup	t_{RDS}	5		ns
Receive data hold	t_{RDH}	30		ns
Collision data setup	t_{CDS}	0		ns
Collision data hold	t_{CDH}	30		ns
Transmit data delay	t_{XDD}	20	68	ns
Request to send delay 1	t_{RTD1}	30	120	ns
Request to send delay 2	t_{RTD2}	20	85	ns
Clock period	t_{CP}	240		ns
Clock period LOW	t_{CPL}	90		ns
Clock period HIGH	t_{CPH}	100		ns

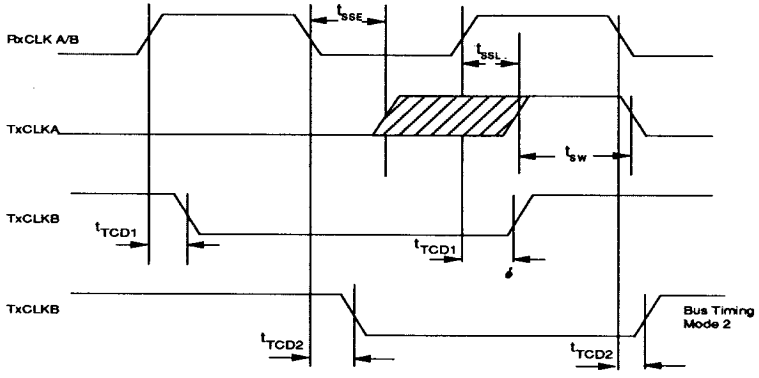


Figure 7. Clock Mode 5

Parameter		Min.	Max.	Unit
Sync pulse start early *	t_{SSE}	30		ns
Sync pulse start late **	t_{SSL}	0	30	ns
Sync pulse width	t_{SW}	40		ns
Time-slot control 2 delay	t_{TCDE}	20	85	ns
Time-slot control 1 delay	t_{TCD1}	30	120	ns

* If sync pulse starts before ↘ edge of RxCLK A/B first bit transmitted occurs on ↘ edge of RxCLK A/B.
** If sync pulse occurs after ↘ edge of RxCLK A/B first bit transmitted occurs on ↘ edge of sync pulse.

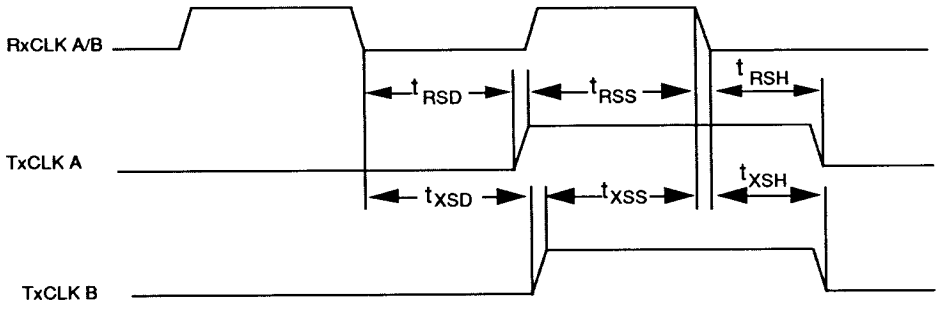


Figure 8. Clock Mode 1

Parameter		Min.	Max.	Unit
Receive strobe delay	t_{RSD}	30		ns
Receive strobe setup	t_{RSS}	70		ns
Receive strobe hold	t_{RSH}	30		ns
Transmit strobe delay	t_{XSD}	30		ns
Transmit strobe setup	t_{XSS}	70		ns
Transmit strobe hold	t_{XSH}	30		ns

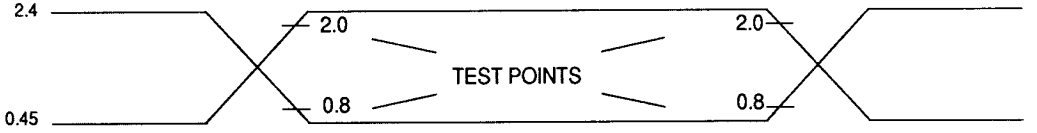


Figure 9. Test Points

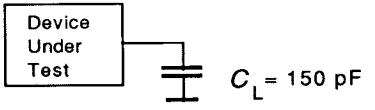
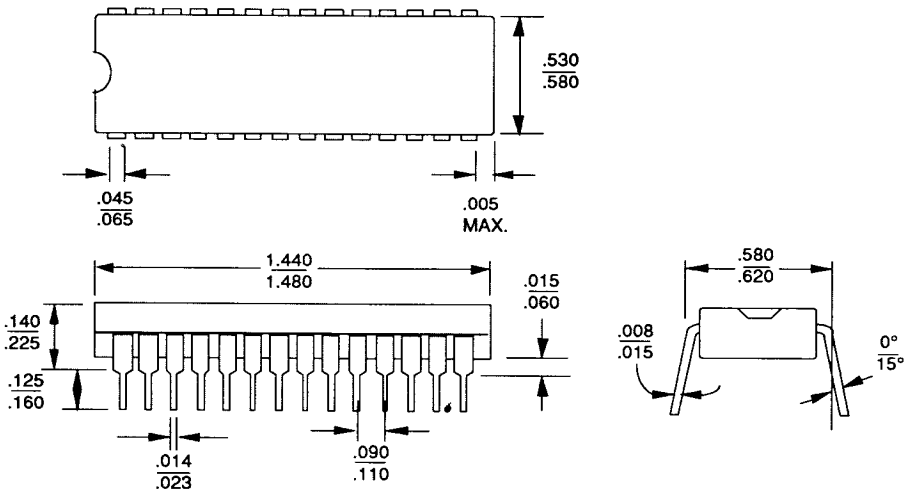


Figure 10. Load Circuit

AC Testing

Inputs are driven at 2.4 V for logical '1' and 0.45 V for logical '0'.
Timing measurements are made at 2.0V for logical '1' and at 0.8 V for logical '0'.

PD 028



06842B

PLCC 028