

Features

- Very high speed: 55 ns
- Wide voltage range: 1.65 V – 2.25 V
- Pin compatible with CY62137CV18
- Ultra low standby power
 - Typical standby current: 1 μ A
 - Maximum standby current: 5 μ A
- Ultra low active power
 - Typical active current: 1.6 mA @ f = 1 MHz
- Ultra low standby power
- Easy memory expansion with CE and OE features
- Automatic power down when deselected
- Complementary metal oxide semiconductor (CMOS) for optimum speed and power
- Byte power-down feature
- Available in a Pb-free 48-Ball Very fine ball grid package (VFBGA) package

Functional Description

The CY62137FV18 is a high performance CMOS static RAM organized as 128K words by 16 bits. This device features advanced circuit design to provide ultra low active current. This

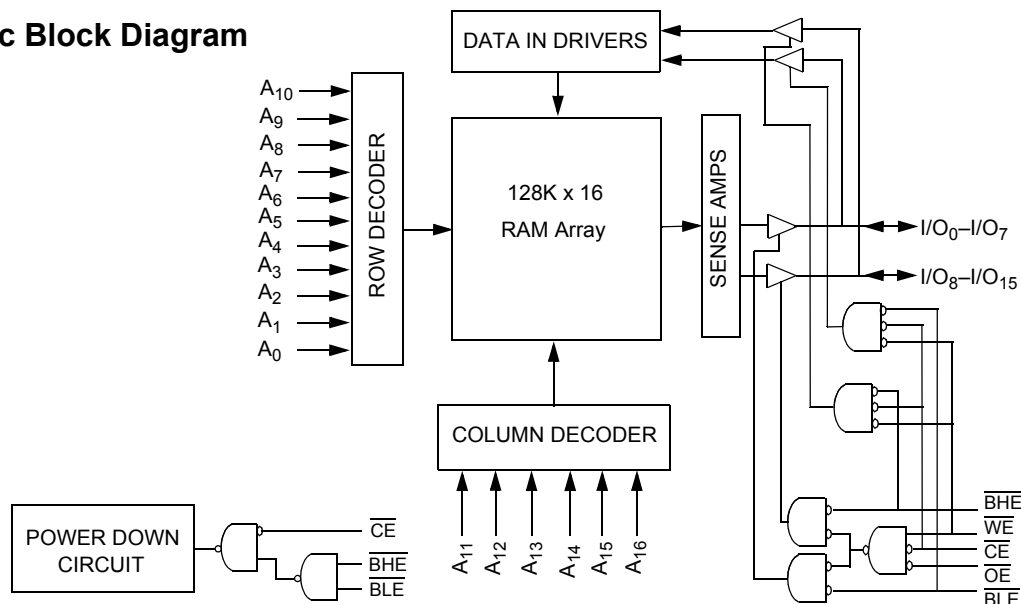
is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power down feature that significantly reduces power consumption when addresses are not toggling. Placing the device into standby mode reduces power consumption by more than 99% when deselected (\overline{CE} HIGH or both \overline{BLE} and \overline{BHE} are HIGH). The input and output pins (I/O_0 through I/O_{15}) are placed in a high impedance state when the device is deselected (\overline{CE} HIGH), the outputs are disabled (\overline{OE} HIGH), both the Byte High Enable and the Byte Low Enable are disabled (\overline{BHE} , \overline{BLE} HIGH), or during an active write operation (\overline{CE} LOW and \overline{WE} LOW).

To write to the device, take Chip Enable (\overline{CE}) and Write Enable (\overline{WE}) inputs LOW. If Byte Low Enable (\overline{BLE}) is LOW, then data from I/O pins (I/O_0 through I/O_7) is written into the location specified on the address pins (A_0 through A_{16}). If Byte High Enable (\overline{BHE}) is LOW, then data from I/O pins (I/O_8 through I/O_{15}) is written into the location specified on the address pins (A_0 through A_{16}).

To read from the device, take Chip Enable (\overline{CE}) and Output Enable (\overline{OE}) LOW while forcing the Write Enable (\overline{WE}) HIGH. If Byte Low Enable (\overline{BLE}) is LOW, then data from the memory location specified by the address pins appear on I/O_0 to I/O_7 . If Byte High Enable (\overline{BHE}) is LOW, then data from the memory appears on I/O_8 to I/O_{15} . See the “Truth Table” on page 11 for a complete description of read and write modes.

For best practice recommendations, refer to the Cypress application note [AN1064, SRAM System Guidelines](#).

Logic Block Diagram



Contents

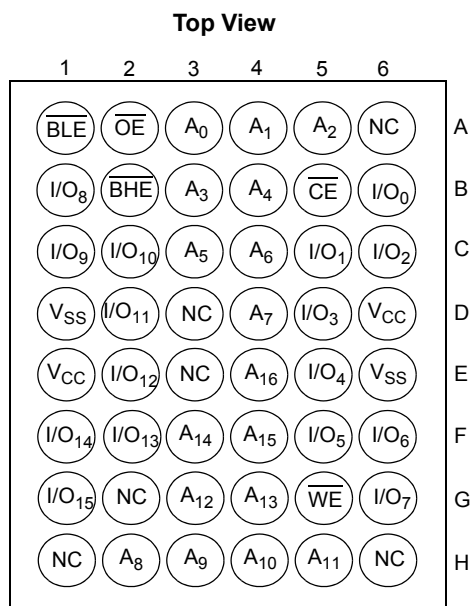
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Product Portfolio

Product	V _{CC} Range (V)			Speed (ns)	Power Dissipation					
					Operating I _{CC} (mA)				Standby I _{SB2} (μA)	
					f = 1 MHz		f = f _{max}			
Min	Typ ^[1]	Max	Typ ^[1]	Max	Typ ^[1]	Max	Typ ^[1]	Max		
CY62137FV18LL	1.65	1.8	2.25	55	1.6	2.5	13	18	1	5

Pin Configuration

Figure 1. 48-Ball VFBGA Pinout [2, 3]



Notes

1. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC(typ)}, T_A = 25 °C.
2. NC pins are not connected on the die.
3. Pins D3, H1, G2, H6 and H3 in the VFBGA package are address expansion pins for 4 Mb, 8 Mb, 16 Mb, and 32 Mb and 64 Mb respectively.

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. User guidelines are not tested.

Storage temperature	-65 °C to + 150 °C
Ambient temperature with power applied	-55 °C to + 125 °C
Supply voltage to ground potential	-0.2 V to + 2.45 V
DC voltage applied to outputs in High Z State ^[4, 5]	-0.2 V to 2.45 V

DC Input Voltage ^[4, 5]	-0.2 V to 2.45 V
Output Current into Outputs (LOW)	20 mA
Static Discharge Voltage	> 2001 V (MIL-STD-883, Method 3015)
Latch up Current	> 200 mA

Operating Range

Device	Range	Ambient Temperature	V _{CC} ^[6]
CY62137FV18	Industrial	-40 °C to +85 °C	1.65 V to 2.25 V

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	55 ns			Unit
			Min	Typ ^[7]	Max	
V _{OH}	Output high voltage	I _{OH} = -0.1 mA	1.4	-	-	V
V _{OL}	Output low voltage	I _{OL} = 0.1 mA		-	0.2	V
V _{IH}	Input high voltage	V _{CC} = 1.65 V to 2.25 V	1.4	-	V _{CC} + 0.2 V	V
V _{IL}	Input low voltage	V _{CC} = 1.65 V to 2.25 V	-0.2	-	0.4	V
I _{IX}	Input leakage current	GND ≤ V _I ≤ V _{CC}	-1	-	+1	μA
I _{OZ}	Output leakage current	GND ≤ V _O ≤ V _{CC} , output disabled	-1	-	+1	μA
I _{CC}	V _{CC} operating supply current	f = f _{max} = 1/t _{RC} V _{CC(max)} = 2.25 V I _{OUT} = 0 mA CMOS levels	-	13	18	mA
		f = 1 MHz V _{CC(max)} = 2.25 V	-	1.6	2.5	mA
I _{SB1} ^[8]	Automatic power down current—CMOS inputs	$\overline{CE} \geq V_{CC} - 0.2 \text{ V}$, or $(\overline{BHE} \text{ and } \overline{BLE}) \geq V_{CC} - 0.2 \text{ V}$, V _{IN} ≥ V _{CC} - 0.2 V, V _{IN} ≤ 0.2 V, f = f _{max} (address and data only), f = 0 (OE, WE)	-	1	5	μA
I _{SB2} ^[8]	Automatic power down current—CMOS inputs	$\overline{CE} \geq V_{CC} - 0.2 \text{ V}$, or $(\overline{BHE} \text{ and } \overline{BLE}) \geq V_{CC} - 0.2 \text{ V}$, V _{IN} ≥ V _{CC} - 0.2 V, or V _{IN} ≤ 0.2 V, f = 0	-	1	5	μA

Capacitance

Parameter ^[9]	Description	Test Conditions	Max	Unit
C _{IN}	Input capacitance	T _A = 25 °C, f = 1 MHz,	10	pF
C _{OUT}	Output capacitance	V _{CC} = V _{CC(typ)}	10	pF

Notes

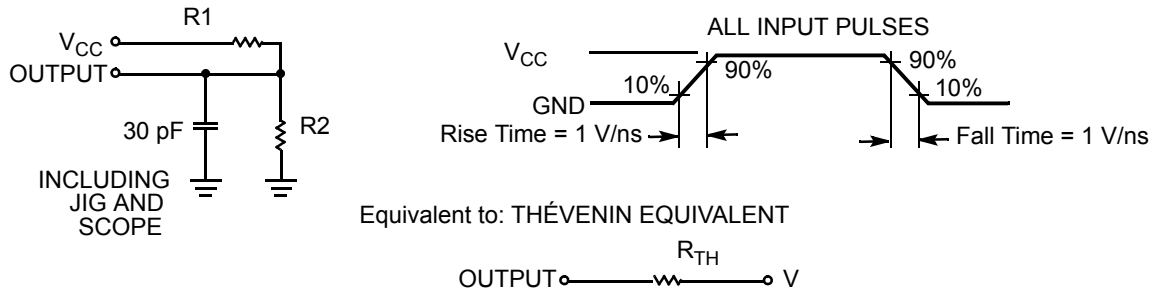
- V_{IL(min)} = -2.0 V for pulse durations less than 20 ns.
- V_{IH(max)} = V_{CC} + 0.5 V for pulse durations less than 20 ns.
- Full device AC operation assumes a minimum of 100 μs ramp time from 0 to V_{CC(min)} and 200 μs wait time after V_{CC} stabilization.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC(typ)}, T_A = 25 °C
- Chip enable (CE) and byte enables (BHE and BLE) must be tied to CMOS levels to meet the I_{SB1} / I_{SB2} / I_{CCDR} spec. Other inputs can be left floating
- Tested initially and after any design or process changes that may affect these parameters

Thermal Resistance

Parameter ^[10]	Description	Test Conditions	VFBGA	Unit
Θ_{JA}	Thermal resistance (Junction to Ambient)	Still air, soldered on a 3 × 4.5 inch, two-layer printed circuit board	75	°C / W
Θ_{JC}	Thermal resistance (Junction to case)		10	°C / W

AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms



Parameters	1.80 V	Unit
R1	13500	Ω
R2	10800	Ω
R_{TH}	6000	Ω
V_{TH}	0.80	V

Note

10. Tested initially and after any design or process changes that may affect these parameters

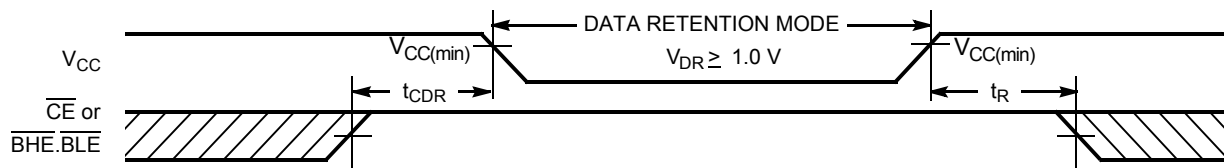
Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Typ ^[11]	Max	Unit
V_{DR}	V_{CC} for data retention		1.0	–	–	V
I_{CCDR} ^[12]	Data retention current	$V_{CC} = 1.0\text{ V}$, $CE \geq V_{CC} - 0.2\text{ V}$, or $(\overline{BHE}$ and $\overline{BLE}) \geq V_{CC} - 0.2\text{ V}$, $V_{IN} \geq V_{CC} - 0.2\text{ V}$ or $V_{IN} \leq 0.2\text{ V}$	–	1	4	μA
t_{CDR} ^[13]	Chip deselect to data retention time		0	–	–	ns
t_R ^[14]	Operation recovery time		55	–	–	ns

Data Retention Waveform

Figure 3. Data Retention Waveform^[15]



Note

11. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(\text{typ})}$, $T_A = 25\text{ }^\circ\text{C}$.
12. Chip enable (\overline{CE}) and byte enables (\overline{BHE} and \overline{BLE}) must be tied to CMOS levels to meet the $I_{SB1} / I_{SB2} / I_{CCDR}$ spec. Other inputs can be left floating.
13. Tested initially and after any design or process changes that may affect these parameters
14. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(\text{min})} \geq 100\text{ }\mu\text{s}$ or stable at $V_{CC(\text{min})} \geq 100\text{ }\mu\text{s}$
15. $\overline{BHE}.\overline{BLE}$ is the AND of both \overline{BHE} and \overline{BLE} . Deselect the chip by either disabling chip enable signals or by disabling both \overline{BHE} and \overline{BLE} .

Switching Characteristics

Over the Operating Range

Parameter ^[16, 17]	Description	55 ns		Unit
		Min	Max	
Read Cycle				
t _{RC}	Read cycle time	55	–	ns
t _{AA}	Address to data valid	–	55	ns
t _{OHA}	Data hold from address change	10	–	ns
t _{ACE}	\overline{CE} LOW to data valid	–	55	ns
t _{DOE}	\overline{OE} LOW to data valid	–	25	ns
t _{LZOE}	\overline{OE} LOW to low Z ^[18]	5	–	ns
t _{HZOE}	\overline{OE} HIGH to high Z ^[18, 19]	–	18	ns
t _{LZCE}	\overline{CE} LOW to low Z ^[18]	10	–	ns
t _{HZCE}	\overline{CE} HIGH to high Z ^[18, 19]	–	18	ns
t _{PU}	\overline{CE} LOW to power up	0	–	ns
t _{PD}	\overline{CE} HIGH to power down	–	55	ns
t _{DBE}	$\overline{BLE}/\overline{BHE}$ LOW to data valid	–	55	ns
t _{LZBE}	$\overline{BLE}/\overline{BHE}$ LOW to Low Z ^[18]	10	–	ns
t _{HZBE}	$\overline{BLE}/\overline{BHE}$ HIGH to High Z ^[18, 19]	–	18	ns
Write Cycle ^[20]				
t _{WC}	Write cycle time	45	–	ns
t _{SCE}	\overline{CE} LOW to write end	35	–	ns
t _{AW}	Address setup to write end	35	–	ns
t _{HA}	Address hold from write end	0	–	ns
t _{SA}	Address setup to write start	0	–	ns
t _{PWE}	\overline{WE} pulse width	35	–	ns
t _{BW}	$\overline{BLE}/\overline{BHE}$ LOW to write end	35	–	ns
t _{SD}	Data setup to write end	25	–	ns
t _{HD}	Data hold from write end	0	–	ns
t _{HZWE}	\overline{WE} LOW to high Z ^[18, 19]	–	18	ns
t _{LZWE}	\overline{WE} HIGH to low Z ^[18]	10	–	ns

Notes

16. Test conditions for all parameters other than tri-state parameters assume signal transition time of 1V/ns or less, timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0 to $V_{CC(typ)}$, and output loading of the specified I_{OL}/I_{OH} as shown in the "AC Test Loads and Waveforms" on page 5.
17. AC timing parameters are subject to byte enable signals (BHE or BLE) not switching when chip is disabled. Please see application note AN13842 for further clarification.
18. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZBE} is less than t_{LZBE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
19. t_{HZOE}, t_{HZCE}, t_{HZBE}, and t_{HZWE} transitions are measured when the outputs enter a high impedance state
20. The internal write time of the memory is defined by the overlap of \overline{WE} , $CE = V_{IL}$, BHE and/or $\overline{BLE} = V_{IL}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.

Switching Waveforms

Figure 4. Read Cycle No.1 (Address Transition Controlled)^[21, 22]

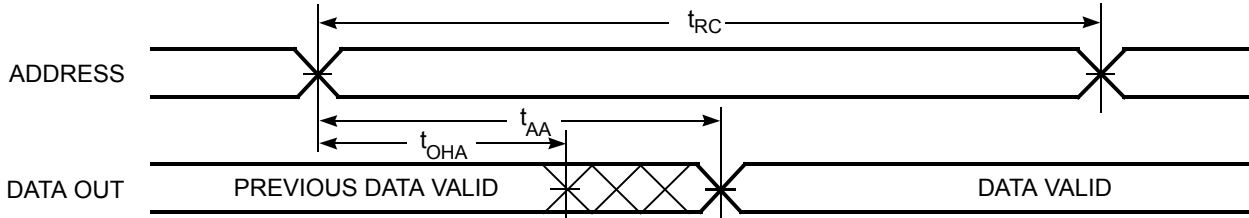
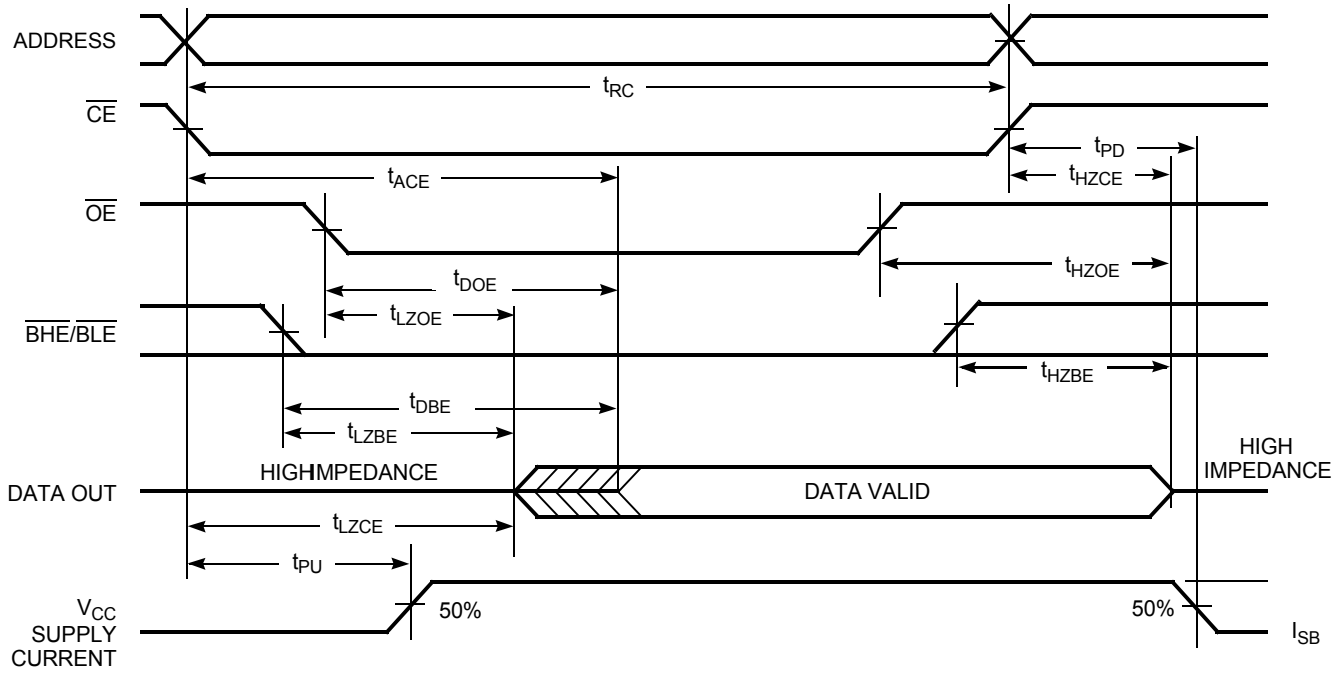


Figure 5. Read Cycle No. 2 ($\overline{\text{OE}}$ Controlled)^[22, 23]



Notes

21. The device is continuously selected. $\overline{\text{OE}}$, $\overline{\text{CE}} = V_{\text{IL}}$, $\overline{\text{BHE}}$ and/or $\overline{\text{BLE}} = V_{\text{IL}}$.
22. $\overline{\text{WE}}$ is HIGH for read cycle.
23. Address valid before or similar to $\overline{\text{CE}}$ and $\overline{\text{BHE}}$, $\overline{\text{BLE}}$ transition LOW.

Switching Waveforms (continued)

Figure 6. Write Cycle No. 1 (\overline{WE} Controlled)^[24, 25]

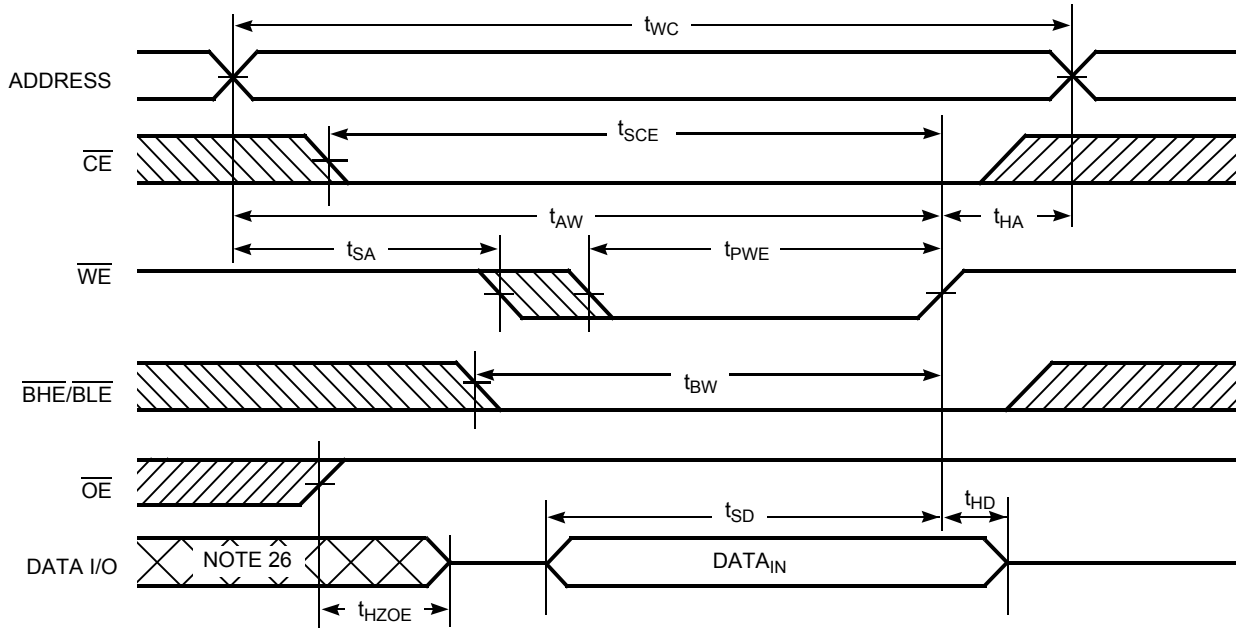
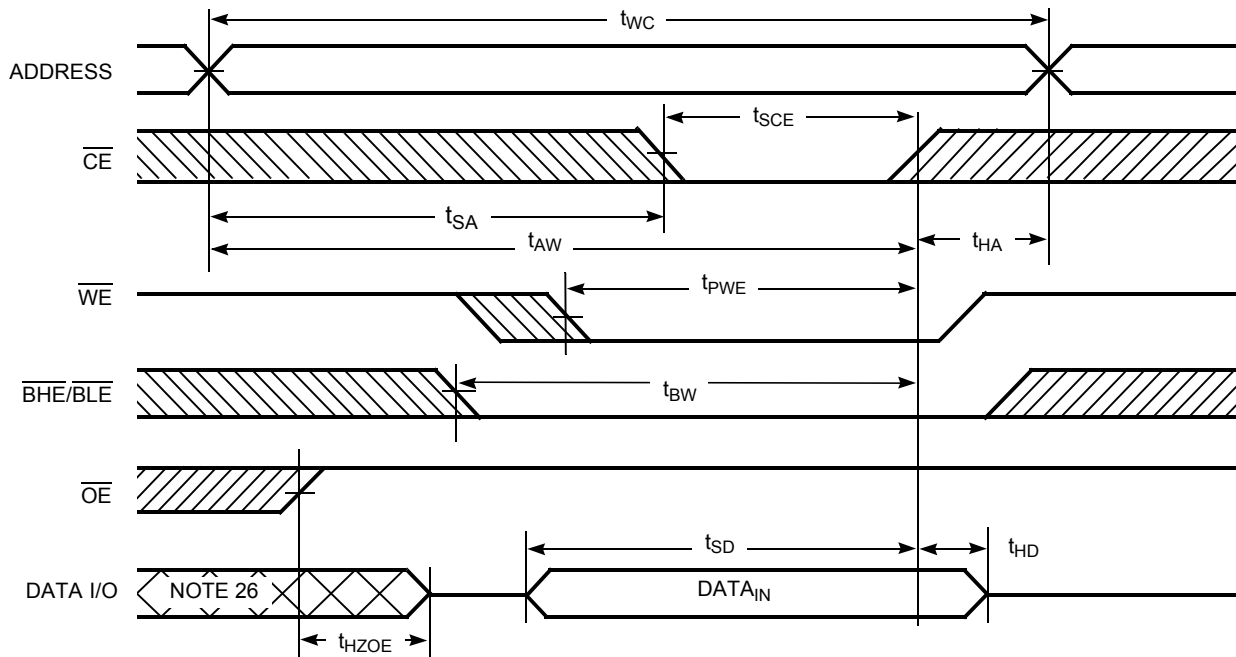


Figure 7. Write Cycle No. 2 (\overline{CE} Controlled)^[24, 25]



Notes

- 24. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
- 25. If \overline{CE} goes HIGH simultaneously with $\overline{WE} = V_{IH}$, the output remains in a high impedance state.
- 26. During this period, the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 8. Write Cycle No. 3 ($\overline{\text{WE}}$ Controlled)^[27]

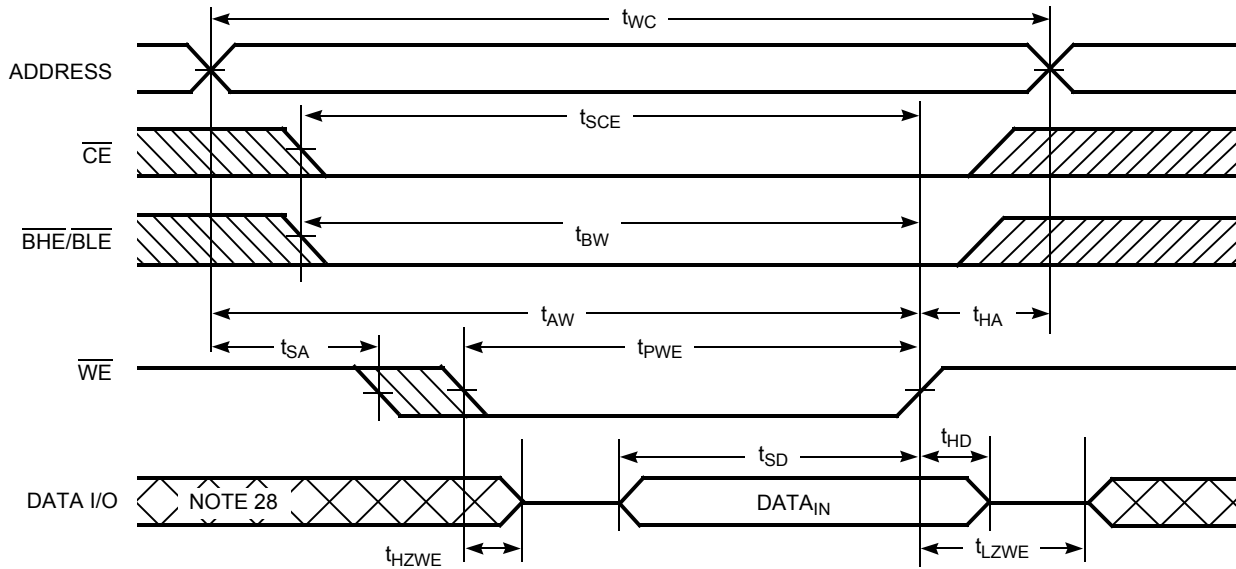
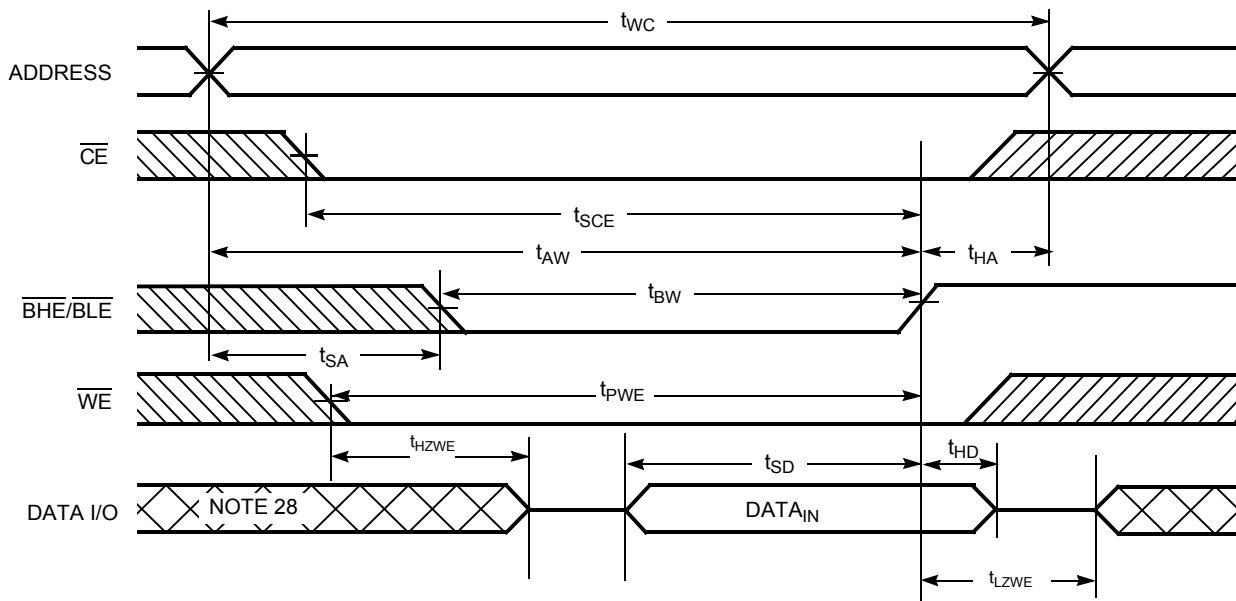


Figure 9. Write Cycle No. 4 ($\overline{\text{BHE/BLE}}$ Controlled, $\overline{\text{OE}}$ LOW)^[27]



Notes

- 27. If $\overline{\text{CE}}$ goes HIGH simultaneously with $\overline{\text{WE}} = V_{IH}$, the output remains in a high impedance state.
- 28. During this period, the I/Os are in output state. Do not apply input signals

Truth Table

\overline{CE}	\overline{WE}	\overline{OE}	\overline{BHE}	\overline{BLE}	Inputs or Outputs	Mode	Power
H	X	X	X ^[29]	X ^[29]	High Z	Deselect or power down	Standby (I _{SB})
X ^[29]	X	X	H	H	High Z	Deselect or power down	Standby (I _{SB})
L	H	L	L	L	Data out (I/O ₀ –I/O ₁₅)	Read	Active (I _{CC})
L	H	L	H	L	Data out (I/O ₀ –I/O ₇); I/O ₈ –I/O ₁₅ in High Z	Read	Active (I _{CC})
L	H	L	L	H	Data out (I/O ₈ –I/O ₁₅); I/O ₀ –I/O ₇ in High Z	Read	Active (I _{CC})
L	H	H	L	L	High Z	Output disabled	Active (I _{CC})
L	H	H	H	L	High Z	Output disabled	Active (I _{CC})
L	H	H	L	H	High Z	Output disabled	Active (I _{CC})
L	L	X	L	L	Data in (I/O ₀ –I/O ₁₅)	Write	Active (I _{CC})
L	L	X	H	L	Data in (I/O ₀ –I/O ₇); I/O ₈ –I/O ₁₅ in High Z	Write	Active (I _{CC})
L	L	X	L	H	Data in (I/O ₈ –I/O ₁₅); I/O ₀ –I/O ₇ in High Z	Write	Active (I _{CC})

Note

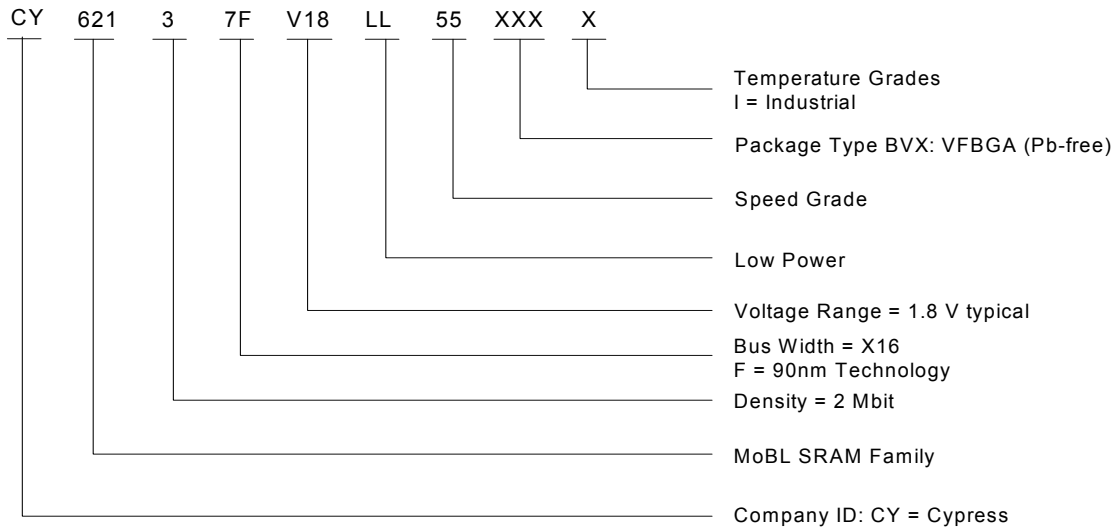
29. The 'X' (Don't care) state for the Chip enable (\overline{CE}) and Byte enables (\overline{BHE} and \overline{BLE}) in the truth table refer to the logic state (either HIGH or LOW). Intermediate voltage levels on these pins is not permitted

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
55	CY62137FV18LL-55BVXI	51-85150	48-Ball VFBGA (Pb-free)	Industrial

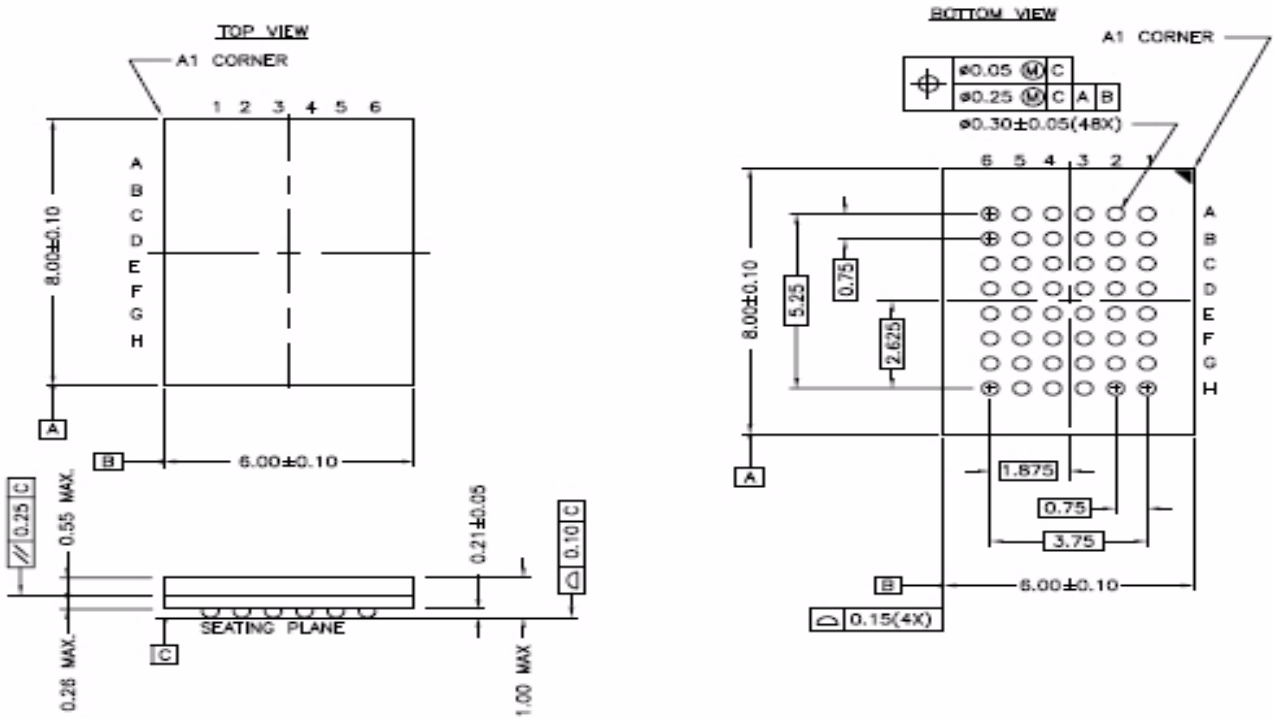
Contact your local Cypress sales representative for availability of other parts.

Ordering Code Definition



Package Diagram

Figure 10. 48-Ball VFBGA (6 x 8 x 1 mm), 51-85150



51-85150 *F

Acronyms

Acronym	Description
CMOS	complementary metal oxide semiconductor
I/O	input/output
SRAM	static random access memory
VFBGA	very fine ball grid array
TSOP	thin small outline package

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
μA	microamperes
mA	milliampere
MHz	megahertz
ns	nanoseconds
pF	picofarads
V	volts
Ω	ohms
W	watts

Document History Page

Document Title: CY62137FV18 MoBL® 2-Mbit (128K x 16) Static RAM Document Number: 001-08030				
REV.	ECN NO.	Submission Date	Orig. of Change	Description of Change
**	463660	See ECN	NXR	New datasheet
*A	469180	See ECN	NSI	Minor change: moved to external web
*B	569125	See ECN	NXR	Converted from preliminary to final Replaced 45 ns speed bin with 55 ns speed bin Changed the $I_{CC(max)}$ value from 2.25 mA to 2.5 mA for test condition $f=1$ MHz Changed the $I_{SB2(typ)}$ value from 0.5 μ A to 1 μ A Changed the $I_{SB2(max)}$ value from 2.5 μ A to 5 μ A Changed the $I_{CCDR(typ)}$ value from 0.5 μ A to 1 μ A and $I_{CCDR(max)}$ value from 2.5 μ A to 4 μ A
*C	869500	See ECN	VKN	Added footnote #12 related to t_{ACE}
*D	908120	See ECN	VKN	Added footnote #8 related to I_{SB2} and I_{CCDR} Made footnote #13 applicable to AC parameters from t_{ACE} Changed t_{WC} specification from 45 ns to 55 ns Changed t_{SCE} , t_{AW} , t_{PWE} , t_{BW} specification from 35 ns to 40 ns Changed t_{HZWE} specification from 18 ns to 20 ns
*E	1274728	See ECN	VKN/AESA	Changed t_{WC} specification from 55 ns to 45 ns Changed t_{SCE} , t_{AW} , t_{PWE} , t_{BW} specification from 40 ns to 35 ns Changed t_{HZWE} specification from 20 ns to 18 ns
*F	2943752	06/03/2010	VKN	Added Contents Added footnote related to Chip enable and Byte enables in Truth Table Updated Package Diagram Added Sales, Solutions, and Legal Information
*G	3055165	10/12/2010	RAME	Added Contents Added Acronyms and Units of Measure Update Package Diagram from *E to *F Added Ordering Code Definition details. Changed $I_{SB1}/I_{SB2}/I_{CCDR}$ test conditions to reflect byte power down feature
*H	3061313	10/15/2010	RAME	Minor Changes: Corrected CE to \overline{CE} and WE to \overline{WE} in Figures 7 and 8

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