New Jersey Semi-Conductor Products, Inc.

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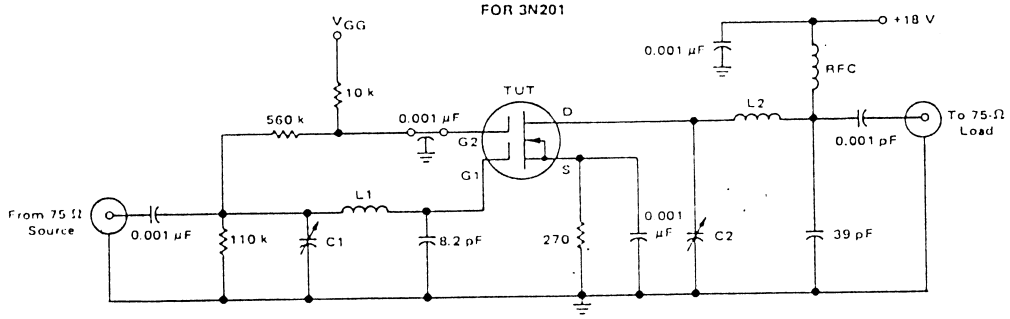
ELECTRICAL CHARACTERISTICS (continued) (T_A = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
Common Source Power Gain		G_{ps}				dB
(V_{DD} = 18 Vdc, V_{GG} = 7.0 Vdc, f = 200 MHz) (Figure 1)	3N201		15	20	25	
(V_{DD} = 18 Vdc, V_{GG} = 6.0 Vdc, f = 45 MHz) (Figure 3)	3N203		20	25	30	
(V_{DD} = 18 Vdc, f_{LO} = 245 MHz, f_{RF} = 200 MHz) (Figure 2)	3N202	G_c(5)	15	19	25	
Bandwidth		BW				MHz
(V_{DD} = 18 Vdc, V_{GG} = 7.0 Vdc, f = 200 MHz) (Figure 1)	3N201		5.0	—	9.0	
(V_{DD} = 18 Vdc, f_{LO} = 245 MHz, f_{RF} = 200 MHz) (Figure 2)	3N202		4.5	—	7.5	
(V_{DD} = 18 Vdc, V_{GG} = 6.0 Vdc, f = 45 MHz) (Figure 3)	3N203		3.0	—	6.0	
Gain Control Gate-Supply Voltage(4)		$V_{GG(GC)}$				Vdc
(V_{DD} = 18 Vdc, ΔG_{ps} = −30 dB, f = 200 MHz) (Figure 1)	3N201		0	−1.0	−3.0	
(V_{DD} = 18 Vdc, ΔG_{ps} = −30 dB, f = 45 MHz) (Figure 3)	3N203		0	−0.6	−3.0	

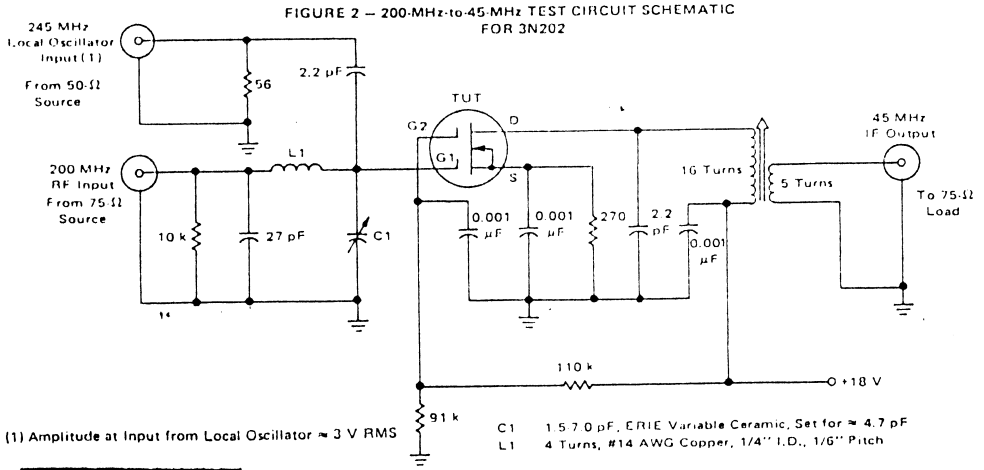
) All gate breakdown voltages are measured while the device is conducting rated gate current. This ensures that the gate-voltage limiting network is functioning properly.
) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2.0%.
) This parameter must be measured with bias voltages applied for less than 5 seconds to avoid overheating.
) ΔG_{ps} is defined as the change in G_{ps} from the value at V_{GG} = 7.0 volts (3N201) and V_{GG} = 6.0 volts (3N203).
) Power Gain Conversion

FIGURE 1 – 200-MHz TEST CIRCUIT SCHEMATIC FOR 3N201



C1 4.0-30 pF, ERIE Variable Ceramic, Set for ≈ 22 pF
C2 4.0-30 pF, ERIE Variable Ceramic, Set for ≈ 10 pF
L1 4 Turns, #14 AWG Cooper, 1/4" I.D., 1/6" Pitch
L2 3 Turns, #14 AWG Cooper, 1/4" I.D., 1/8" Pitch
RFC DELEVAN No. 153712, 1.0 μH

FIGURE 2 – 200-MHz-to-45-MHz TEST CIRCUIT SCHEMATIC FOR 3N202



(1) Amplitude at Input from Local Oscillator ≈ 3 V RMS

C1 1.5-7.0 pF, ERIE Variable Ceramic, Set for ≈ 4.7 pF
L1 4 Turns, #14 AWG Copper, 1/4" I.D., 1/6" Pitch

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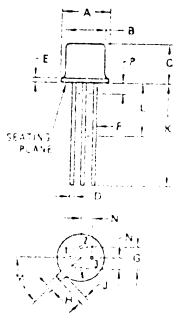
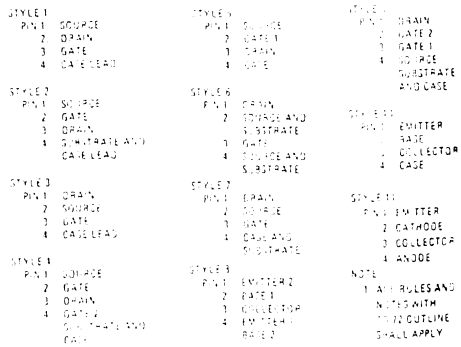


DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	5.31	5.74	0.209	0.226
B	4.52	4.95	0.178	0.195
C	4.32	5.33	0.171	0.210
D	0.41	0.53	0.016	0.021
E		0.25		0.010
F	0.41	0.48	0.016	0.019
G		2.54 BSC		0.100 BSC
H	0.91	1.17	0.036	0.046
J	0.71	1.22	0.028	0.048
K	12.70		0.500	
L	5.35		0.210	
M	45° BSC		45° BSC	
N	1.27 BSC		0.050 BSC	
P		0.51		0.020

ALL JEDEC dimensions and notes apply

CASE 20 STYLES

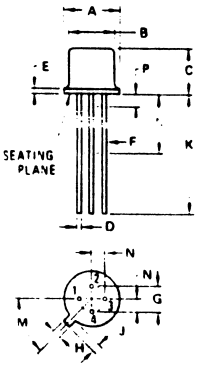


Quality Semi-Conductors

Package Outline Dimensions

Dimensions are in inches unless otherwise noted.

TO-72 (TO-206AF)



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	[illegible]	[illegible]	[illegible]	[illegible]
B	4.52	4.95	0.178	0.195
C	4.32	5.33	0.170	0.210
D	0.41	0.53	0.016	0.021
E		0.76		0.030
F	0.41	0.48	0.016	0.019
G	2.54 BSC		0.100 BSC	
H	0.91	1.17	0.036	0.046
J	0.71	1.22	0.028	0.048
K	12.70	-	0.500	-
L	6.35	-	0.250	-
M	45° BSC		45° BSC	
N	1.27 BSC		0.050 BSC	
P		1.27		0.050

ALL JEDEC dimensions and notes apply