AK5602A

Energy Metering LSI for multi phase, high accurate application

Features

- Suitable for three phase, 3 wired or 4 wired energy metering or energy monitoring application
- Provide less than 0.1 % active & reactive energy error over a dynamic range of 1000 to 1, compatible with IEC 0.5S
- Provide instantaneous active power, reactive power and apparent power
- Provide voltage RMS, current RMS, voltage instantaneous value, current instantaneous value and power factor in each phase.
- Provide less than 0.5 % voltage RMS, current RMS and power factor error
- Provide very accurate 90 degree phase shifter over 45Hz to 65Hz input frequency range, which is used for reactive power calculation
- Provide minute input voltage monitoring function
- Wide phase adjust. range between V & I (11°)
- Provide positive and negative power indication
- Built-in temperature sensor
- Single power supply (3 V or 5V)
- 48LQFP

Operational Summary

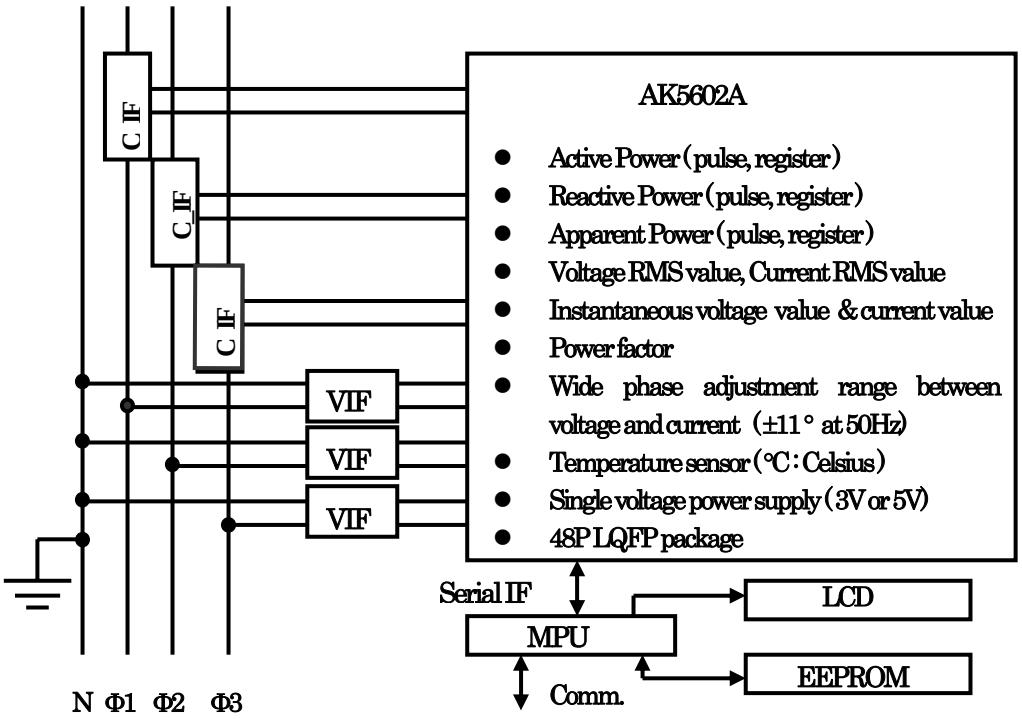
AK5602A is one of the most advanced and functional LSIs for multi phase energy measurement.
Current and voltage signals through CT, Hall sensor, or Shunt Resistors are converted into digital signal with 18bit ADC.

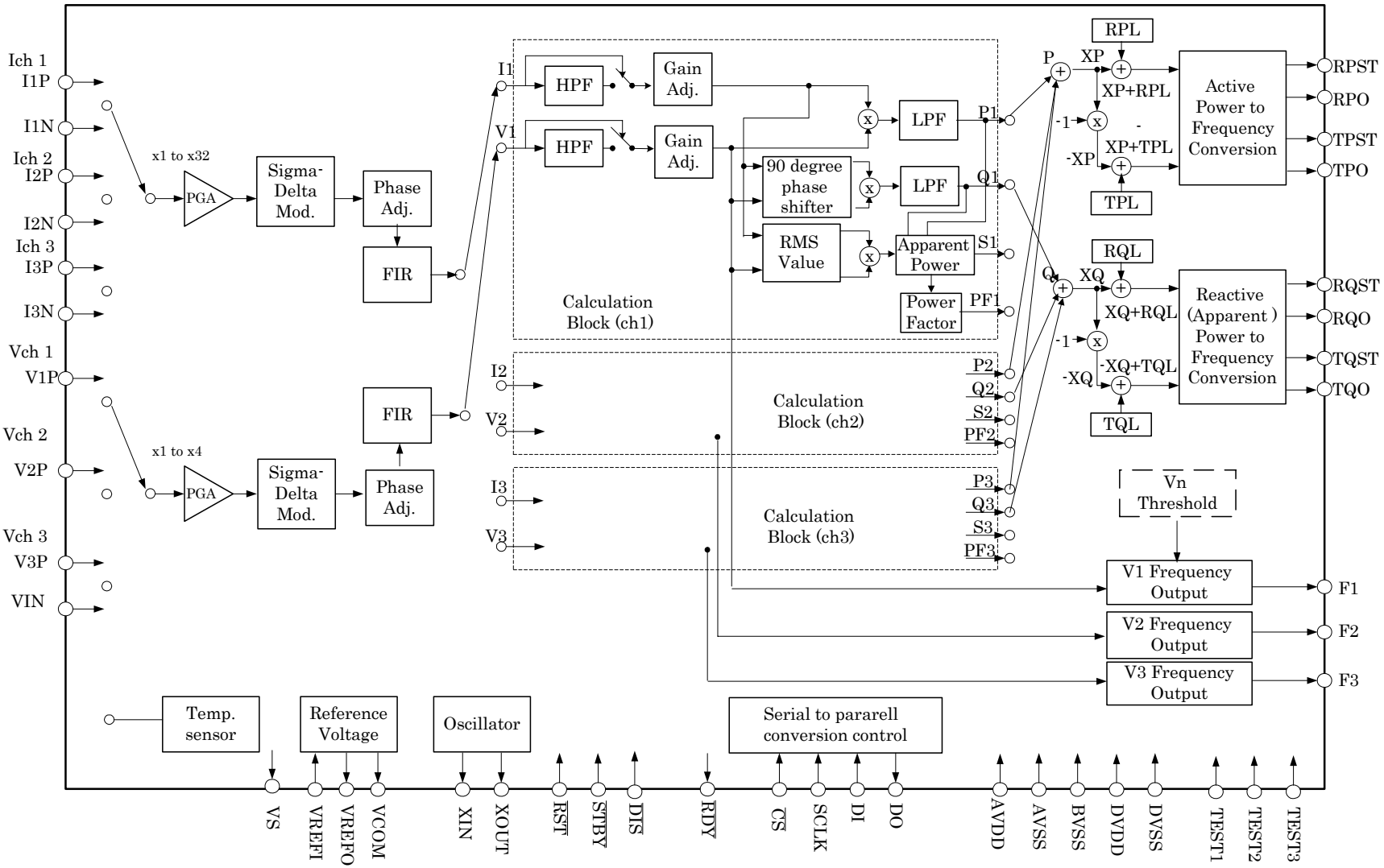
Instantaneous voltage and current in each phase is multiplied and is added in total phases.

The value changes into active power after passing through LPF and added with the value of a light load register. After this value is compared with the value of rated standard value register, it outputs pulses in proportion to the calculation.

Regarding reactive power, input current is precisely shift by 90 degree and multiplied with respective voltage input signal. It outputs pulses in the same manner of active power calculation.
And apparent power can be selectively derived from either active power and reactive power calculation or VRMS x IRMS calculation and it outputs pulses as the result of calculation.

System Block Diagram




Ich 1
I1P
I1N
Ich 2
I2P
I2N
Ich 3
I3P
I3N
Vch 1
V1P
Vch 2
V2P
Vch 3
V3P
VIN
x1 to x32
PGA
Sigma-Delta Mod.
Phase Adj.
FIR
x1 to x4
PGA
Sigma-Delta Mod.
Phase Adj.
FIR
I1
V1
I2
V2
I3
V3
HPF
HPF
Gain Adj.
Gain Adj.
90 degree phase shifter
RMS Value
LPF
LPF
Apparent Power
Power Factor
P1
Q1
S1
PF1
Calculation Block (ch1)
Calculation Block (ch2)
Calculation Block (ch3)
P2
Q2
S2
PF2
P3
Q3
S3
PF3
RPL
XP
XP+RPL
XP+TPL
TPL
-1
-XP
P
Active Power to Frequency Conversion
RPST
RPO
TPST
TPO
RQL
XQ
XQ+RQL
-XQ+TQL
TQL
-1
-XQ
Q
Reactive (Apparent) Power to Frequency Conversion
RQST
RQO
TQST
TQO
Vn Threshold
V1 Frequency Output
V2 Frequency Output
V3 Frequency Output
F1
F2
F3
Temp. sensor
Reference Voltage
Oscillator
Serial to pararell conversion control
VS
VREFI
VREFO
VCOM
XIN
XOUT
RST
STBY
DIS
RDY
CS
SCLK
DI
DO
AVDD
AVSS
BVSS
DVDD
DVSS
TEST1
TEST2
TEST3

2. Block feature

Block	Function
PGA (Programmable Gain Amp)	Current Input Gain selection (from ×1 to ×32) Voltage Input Gain selection (from ×1 to ×4) This PGA becomes operative with $\overline{\text{RST}}$ = $\overline{\text{STBY}}$ = "H"
Sigma Delta Modulator	Sigma Delta Modulator with 3 channel differential inputs. This modulator becomes operative with $\overline{\text{RST}}$ = $\overline{\text{STBY}}$ = "H"
Phase Adjuster	This adjusts the phase difference between current IF and voltage IF. This phase shifter becomes operative with $\overline{\text{RST}}$ = $\overline{\text{STBY}}$ = "H"
FIR Filter	LPF. This produces 18 bit ADC data in current side and 16 bit ADC data in voltage side from the sigma delta modulator. This Filter becomes operative with $\overline{\text{RST}}$ = $\overline{\text{STBY}}$ = "H"
HPF	This HPF is a selectable filter. It removes the DC part arising from DC offset of ADC or input signal. In a case of passing through the DC part of input signal, only DC offset of ADC can be removed by calibration command. This HPF is not selected in the default setting. This HPF becomes operative with $\overline{\text{RST}}$ = $\overline{\text{STBY}}$ = "H"
Gain Adjustment	Values of input current and input voltage can be adjusted against ideal values with a gain adjustment (full-scale) command. This adjustment becomes operative with $\overline{\text{RST}}$ = $\overline{\text{STBY}}$ = "H"
90 degree phase shifter	90-degree phase shifter. This shifter becomes operative with $\overline{\text{RST}}$ = $\overline{\text{STBY}}$ = "H"
RMS value calculator	It calculates RMS value from an instantaneous signal. This calculator becomes operative with $\overline{\text{RST}}$ = $\overline{\text{STBY}}$ = "H"
LPF	LPF. This filter becomes operative with $\overline{\text{RST}}$ = $\overline{\text{STBY}}$ = "H"
Apparent power calculator	Apparent power can be derived from either VRMS × IRMS calculation or active power & reactive power calculation. This calculator becomes operative with $\overline{\text{RST}}$ = $\overline{\text{STBY}}$ = "H"
Power Factor	Power factor can be derived from active power & apparent power calculation. Power factor becomes operative with $\overline{\text{RST}}$ = $\overline{\text{STBY}}$ = "H"
Active energy to frequency conversion	Positive active energy or negative active energy is converted into respective frequency, which is proportional to its active energy. This block becomes operative with $\overline{\text{RST}}$ = $\overline{\text{STBY}}$ = $\overline{\text{DIS}}$ = "H"

Reactive energy to frequency conversion	Positive reactive energy or negative reactive energy is converted into respective frequency, which is proportional to its reactive energy. This block becomes operative with $\overline{RST}$ = $\overline{STBY}$ = $\overline{DIS}$ = "H"

Block	Function
Temperature sensor	This block measures the temperature of AK5602A. This block becomes operative with $\overline{RST}$ = $\overline{STBY}$ = $\overline{DIS}$ = "H"
Frequency pulse outputs	Each voltage input is digitized according to each threshold value, and digitized frequency is output. This block becomes operative with $\overline{RST}$ = $\overline{STBY}$ = "H"
Reference voltage generator	This block generates 1.17V reference voltage. This block becomes operative with $\overline{RST}$ = $\overline{STBY}$ = "H"
Oscillator	The crystal oscillator which oscillates around 12.9024MHz is connected. This block becomes operative with $\overline{RST}$ = $\overline{STBY}$ = "H"
Serial to parallel controller	Serial interface to CPU. This block becomes operative with $\overline{RST}$ = "H"

2-1 Block operation mode

$\overline{RST}$	$\overline{STBY}$	$\overline{DIS}$	Block operation mode
L	L	L	All blocks are off
H	L	L	Only serial to parallel controller block is operative.
H	H	L	All blocks except power to frequency conversion blocks are operative.
H	H	H	All blocks are operative.

3. Pin description

AI : Analog input DI : Digital input PWR : Power
AO : Analog output DO : Digital output GND : Ground

Pin Number	Pin Name	Type	Function
1	$\overline{\text{RST}}$	DI	Reset input (Schmitt trigger input) All circuits become inoperative with "L" level input. All registers including input or output registers, controlling registers, data registers are initialized.
2	$\overline{\text{STBY}}$	DI	Standby input (Schmitt trigger input) All circuits except serial pararell controller block become inoperative with "L" level input after $\overline{\text{RST}}$ = "H" It is possible to write in and read registers through the serial to the parallel conversion controller.
3	$\overline{\text{DIS}}$	DI	Disable input (Schmitt trigger input) Active energy to frequency conversion and reactive energy to frequency conversion blocks are stopped and data registers in those blocks are initialized with "L" level input after $\overline{\text{RST}}$ = $\overline{\text{STBY}}$ = "H".
4	TQO	DO	Negative reactive power pulse output "H" pulse is output when accumulated negative reactive energy value is over the setting standard value. This pin becomes inoperative when $\overline{\text{RST}}$ = "L" or $\overline{\text{STBY}}$ = "L" or $\overline{\text{DIS}}$ = "L".
5	TQST	DO	Negative reactive energy flag output (This pin is not used in IEC mode.) "H" level is output when an interval of output pulses at TQO is under the setting starting value. This pin becomes inoperative when $\overline{\text{RST}}$ = "L" or $\overline{\text{STBY}}$ = "L" or $\overline{\text{DIS}}$ = "L".
6	RQO	DO	Positive reactive energy pulse output "H" pulse is output when accumulated positive reactive power value is over the setting standard value. This pin becomes inoperative when $\overline{\text{RST}}$ = "L" or $\overline{\text{STBY}}$ = "L" or $\overline{\text{DIS}}$ = "L".
7	RQST	DO	Positive reactive energy flag output (This pin is not used in IEC mode.) "H" level is output when an interval output pulses at RQO is under the setting starting value. This pin becomes inoperative when $\overline{\text{RST}}$ = "L" or $\overline{\text{STBY}}$ = "L" or $\overline{\text{DIS}}$ = "L".

Pin Number	Pin Name	Type	Function
8	DVSS	GND	Digital ground.
9	DVDD	PWR	Digital power.
10	TPO	DO	Negative active energy pulse output. "H" pulse is output when accumulated negative active power value is over the setting standard value. This pin becomes inoperative when $\overline{\text{RST}}$ = "L" or $\overline{\text{STBY}}$ = "L" or $\overline{\text{DIS}}$ = "L".
11	TPST	DO	Negative active power flag output. "H' level is output when an interval of output pulses at TPO is under the setting starting value. This pin becomes inoperative when $\overline{\text{RST}}$ = "L" or $\overline{\text{STBY}}$ = "L" or $\overline{\text{DIS}}$ = "L".
12	TEST1	DI	Internal use only. Connects to DVSS.
13	RPO	DO	Positive active energy pulse output "H" pulse is output when accumulated positive active power value is over the setting standard value. This pin becomes inoperative when $\overline{\text{RST}}$ = "L" or $\overline{\text{STBY}}$ = "L" or $\overline{\text{DIS}}$ = "L".
14	RPST	DO	Positive active power flag output. "H" level is output when an interval output pulses at RPO is under the setting starting value. This pin becomes inoperative when $\overline{\text{RST}}$ = "L" or $\overline{\text{STBY}}$ = "L" or $\overline{\text{DIS}}$ = "L".
15	TEST2	DI	Internal use only. Connects to DVSS.
16	TEST3	DI	Internal use only. Connects to DVSS.
17	BVSS	GND	Silicon base reference GND. Connects AVSS.
18	XOUT	AO	Crystal oscillator connection. Connects 12.8 MHz oscillator.
19	XIN	AI	
20	AVDD	PWR	Analog power.
21	AVSS	GND	Analog ground.
22	VREFO	AO	Reference voltage output, 1.17V It outputs with the reference to AVSS. This output usually connects to VREFI pin. Connects 4.7uF (under 10uF) electrolytic capacitor and 0.1uF ceramic capacitor between this pin and AGND. This output is an internal use only and should not be connected to circuits outside the IC.

Pin number	Pin name	Type	Function
23	VREFI	AI	Reference voltage input. It usually connects to VREFO. An outside VREF is connected between this pin and AVSS in a case that an inside VREF of the IC is not used.
24	VCOM	AO	Common voltage output, 1.17V. It feeds a common voltage to an internal block of the IC. It should not be connected to the outside circuits of the LSI. Connect 0.1uF ceramic capacitor between this pin and AVSS.
25	VS	AO	Controlling voltage output for input switches. It generates the voltage which controls input switches referenced to AVSS in ON and OFF state. This is an internal use only. It should not be connected to the outside circuits of the IC. Connects 0.1uF ceramic capacitor between this pin and AVSS.
26	VIN	AI	Voltage side common analog negative input.
27	V3P	AI	Voltage side ch3 analog positive input.
28	V2P	AI	Voltage side ch2 analog positive input.
29	V1P	AI	Voltage side ch1 analog positive input.
30	NC	NC	No connection. Connects to AVSS.
31	I1P	AI	Current side ch1 analog positive input.
32	I1N	AI	Current side ch1 analog negative input.
33	I2P	AI	Current side ch2 analog positive input.
34	I2N	AI	Current side ch2 analog negative input.
35	I3P	AI	Current side ch3 analog positive input.
36	I3N	AI	Current side ch2 analog negative input.
37	NC	NC	No connection. Connects to AVSS.
38	$\overline{\text{RDY}}$	DO	Reading approval pin of registers The content of registers can be read when this pin becomes "low". This pin becomes "high" when $\overline{\text{RST}}$ = "L" or $\overline{\text{STBY}}$ = "L" or $\overline{\text{DIS}}$ = "L".

Pin number	Pin name	Type	Function
39	$\overline{CS}$	DI	Serial interface selection input (Schmitt trigger input) Serial interface become operative with "L" level input at this pin while $\overline{RST}$ = "H".
40	SCLK	DI	Serial data clock input
41	BVSS	GND	Silicon base reference GND. Connects to AVSS.
42	DVSS	GND	Digital ground.
43	DVDD	PWR	Digital power.
44	DI	DI	Serial data input This DI pin becomes valid with $\overline{CS}$ = "L" while $\overline{RST}$ = "H" and it inputs data in synchronization with the rising edge of the clock at SCLK pin. Stored data is transferred into the respective register in the synchronization with the rising edge of $\overline{CS}$.
45	DO	DO	Serial data output This DO pin becomes valid with $\overline{CS}$ = "L" while $\overline{RST}$ = "H" and it outputs data in synchronization with the falling edge of the clock at SCLK pin. This DO pin becomes a high impedance state except $\overline{CS}$ = "L" while $\overline{RST}$ = "H".
46	F3	DO	V3 frequency output A rectangular wave produced by a waveform shaping circuit is output. This pin becomes low level when $\overline{RST}$ = "L" or $\overline{STBY}$ = "L".
47	F2	DO	V2 frequency output A rectangular wave produced by a waveform shaping circuit is output. This pin becomes low level when $\overline{RST}$ = "L" or $\overline{STBY}$ = "L".
48	F1	DO	V1 frequency output A rectangular wave produced by a waveform shaping circuit is output. This pin becomes low level when $\overline{RST}$ = "L" or $\overline{STBY}$ = "L".

4. Electrical characteristics

4.1 Absolute maximum rating

Item	Symbol	MIN	MAX	Unit	Reference
Power supply voltage	DVDD	-0.3	+6.5	V	
	AVDD	-0.3	+6.5		
Ground level	AVSS DVSS BVSS	0		V	Voltage reference level
Input current	IIN		±10	mA	Except power pin
Analog input voltage1	V_{INA1}	-0.3	(AVDD)+0.3	V	
Analog input voltage2	V_{INA2}	-3.0	+3.0	V	I1P, I1N, I2P, I2N, I3P, I3N, V1P, V2P, V3P, VIN
Digital input voltage	I_{IND}	-0.3	DVDD+0.3	V	
Storage temperature	T_{stg}	-50	125	°C	

Note) It may cause a permanent damage to the device if used beyond listed conditions.

4.2 Recommended operating conditions

Item	Symbol	MIN	TYP	MAX	Unit	Reference
Power supply voltage	AVDD	2.7		5.25	V	Note 1
	DVDD	2.7		5.25		
Analog reference input voltage	V_{REF}	1.11	1.17	1.23	V	Note 2
Analog input maximum voltage	V_{AIN} MAX	-1.0		1.0	V	Note 3
Analog input voltage	V_{AIN}	-FS		+FS	V	Note 4
Operating temperature	Ta	-40		85	°C	

Note 1: -0.1V ≤ DVDD - AVDD ≤ +0.1V

Note 2: This is a case when outside reference voltage is connected to VREFI.
1.17V±5%

Note 3: This range of analog input signal is to be calculated.

Note 4:

V_{AIN} = (AINP) - (AINN)

AINP: V1P, V2P, V3P; AINN: VIN

Gain × 1 : -FS = -1.0V, +FS = 1.0V
× 2 : -FS = -0.5V, +FS = 0.5V
× 4 : -FS = -0.25V, +FS = 0.25V

AINP: I1P, I2P, I3P; AINN: I1N, I2N, I3N

Gain × 1 : -FS = -1.0V, +FS = 1.0V
× 2 : -FS = -0.5V, +FS = 0.5V
-
× 8 : -FS = -0.125V, +FS = 0.125V
-
× 16 : -FS = -0.0625V, +FS = 0.0625V
-
× 24 : -FS = -0.0417V, +FS = 0.0417V
-
× 32 : -FS = -0.03125V, +FS = 0.03125V

- **Regarding the analog voltage input, ADC outputs a plus full scale code (7FFFh) against the input over a +FS input and outputs a minus full scale code (8000h) against the input under -FS.**
- **Regarding the analog current input, ADC outputs a plus full scale code (1FFFFh) against the input over a +FS input and outputs a minus full scale code (20000h) against the input under -FS.**

4.3 Analog characteristics

Conditions: Ta=25°C, AVDD=DVDD=5.0V,
V_{REF} = 1.17V, XCLK = 12.9024MHz,
Signal frequency = 50Hz, Measured bandwidth = 10 to 1.5kHz;
Unless otherwise specified.

4.3.1 PGA

Voltage side

Item	MIN	TYP	MAX	Unit	Reference
Input range Gain setting : ×4 (12 dB) ×2 (6 dB) ×1 (0 dB)	 ±0.95	 ±0.25 ±0.5 ±1.0	 ±1.05	V_{p-p}	Note 5
Input impedance	350			kΩ	Note 6

Note 5: Only applicable for V (voltage) input. This is a full-scale value of analog input voltage (V_{AIN}= (AINP) - (AINN)). VIN is usually connected to AGND and each analog input voltage is added with reference to VIN.

Note 6: Input impedance between AINP (V1P, V2P, V3P) and AINN (VIN).
Minimum value is when gain is set at ×4 (12dB). Input impedance is reversed proportional to the gain setting.

Current side

Item	MIN	TYP	MAX	Unit	Reference
Input range Gain setting: ×32 (30dB) ×24 (27.6dB) ×16 (24 dB) ×8 (18 dB) ×4 (12 dB) ×2 (6 dB) ×1 (0 dB)	 ±0.95	 ±0.0313 ±0.0417 ±0.0625 ±0.125 ±0.25 ±0.5 ±1.0	 ±1.05	V_{p-p}	Note 7
Input impedance	200			kΩ	Note 8

Note 7: Only applicable for I(current) input (differential input). This is a full-scale value of analog input voltage (V_{AIN} = (AINP) - (AINN)).

Note 8: Input impedance between AINP (I1P, I2P, I3P) and AINN (I1N, I2N, I3N).
Minimum value is when gain is set at ×8 (18dB). Input impedance is reversed proportional to gain setting.

4.3.2 ADC

Voltage side

Item	MIN	TYP	MAX	Unit	Reference
Resolution			16	bit	
S/N+D		65		dB	Note 9
Isolation between current and voltage		100		dB	Note 10
Crosstalk between voltage channels		100		dB	
Power factor adjustment range between current and voltage	-613.84		613.84	us	Note 11
Power factor adjustment accuracy between current and voltage		1.24		us	Note 12
ADC period		3.15		kHz	Note 13

Note 9: This is the value when analog input signal is applied at -6dB of full scale value with PGA = 0 dB. This is the ratio between RMS value of input signal and summation of RMS values of all frequencies from 10Hz to 1.5kHz excluding the input signal.

Note 10: This is the isolation value between voltage side ADC and current side ADC.

Note 11: This is the delay adjustment range of voltage side against current side.
+ side setting delays starting point of A/D conversion at voltage side against starting point of A/D conversion at current side in the range of 0us to +613.84us, while - side setting delays starting point of A/D conversion at current side against starting point of A/D conversion at voltage side in the range of 0us to +613.84us. This enables the delay adjustment range at voltage side against current side from -613.84us to +613.84us. Please note that when the delay adjustment is changed from + to - or - to + during the operation of the IC, A/D conversion data becomes uncontinuous.

Note 12: Delay adjustment step is 1.24us.

Note 13: ADC period is 3.15kHz at every channel.

Current side

Item	MIN	TYP	MAX	Unit	Reference
Resolution			18	bit	
S/N+D		65		dB	Note 14
Isolation between current and voltage		100		dB	Note 15
Crosstalk between current channels		100		dB	
ADC period		3.15		kHz	Note 16

Note 14: This is the value when analog input signal is applied at -6dB of full scale value with PGA = 0 dB. This is the ratio between RMS value of input signal and summation of RMS values of all frequencies from 10Hz to 1.5kHz excluding the input signal.
Note 15: This is the isolation value between voltage side ADC and current side ADC.
Note 16: ADC period is 3.15kHz at every channel.

4.3.3 Reference voltage

Item	MIN	TYP	MAX	Unit	Reference
VREF output level	1.11	1.17	1.23	V	Note 17
VREF temperature drift		30		ppm/°C	Note 18

Note 17: Output level of VREFO. It outputs 1.17V±5% with reference to AVSS.
Note 18: The temperature drift of VREFO output level.

4.3.4 Temperature sensor

Item	MIN	TYP	MAX	Unit	Reference
Temperature range	-40		85	°C	
Resolution		1		°C	Note 19
Accuracy		±5		°C	Note 20

Note 19: Resolution value when the value of temperature register is read from the register.
Note 20: This is the difference between the value of temperature register and real value at 25°C.

4.3.5 Power supply

Item	MIN	TYP1	TYP2	MAX	Unit	Reference
Power consumption		18	40	70	mW	Note 21
Standby Current		1	1	20	uA	Note 21

Note 21: TYP1 is the value at AVDD = DVDD = 3.0V and TYP2 is the value at AVDD = DVDD = 5.0V. Consumption current is measured on condition of which all digital inputs are connected to DVDD or DVSS and all analog inputs are connected to analog input bias level. It does not contain output current. AVDD = DVDD = 2.7V to 5.25V.

4.3.6 Filter characteristics

Ta = -40 to 85°C, AVDD=DVDD=2.7V to 5.25V,
XCLK=12.9024 MHz (Filter characteristics is proportional to the frequency of XCLK.)

4.3.6.1 FIR filter (LPF)

Item		MIN	TYP	MAX	Unit	Reference
Pass band	±0.008dB	45		66	Hz	
	+0.008dB -0.910dB	0		1500		
Attenuation level at stop band	at 10.0kHz	74.0			dB	

4.3.6.2 HPF

Item		MIN	TYP	MAX	Unit	Reference
Frequency response	-3 dB		1.3		Hz	
	-0.5 dB		3.6			
	-0.1dB		8.7			
	-0.004 dB		45			
	-0.002 dB		66			
Phase shift value	45 to 66Hz	1.13		1.66	degree	

4.3.6.3 90 degree phase shifter

Item		MIN	TYP	MAX	Unit	Reference
Phase shift value	45 to 66Hz	89.98	90	90.02	degree	Note 22
Gain error	0 to 1500Hz			± 0.001	dB	Note 23

Note 22: Phase difference between two inputs.
Note 23: Gain error between input and output of 90 degree phase shifter.

4.3.6.4 IIR filter (LPF)

Item		MIN	TYP	MAX	Unit	Reference
Pass band	±0.1dB	0		0.4	Hz	
Attenuation level at stop band	at 100Hz	60			dB	

4.3.7 DC characteristics

Ta = -40 to 85°C, AVDD=DVDD=2.7 to 5.25V

Item	Symbol	MIN	TYP	MAX	Unit	Reference
High level input voltage	V_{IH}	0.7(DVDD)			V	Note 24
Low level input voltage	V_{IL}			0.3(DVDD)	V	Note 24
High level output voltage Iout=0.5mA For RPO/TPO/RQO/TQO Iout=2mA	V_{OH}	(DVDD)-0.4				
Low level output voltage Iout=-0.5mA For RPO/TPO/RQO/TQO Iout=-2mA	V_{OL}			0.4	V	
Input leak current	I_{IN}			±10	uA	

Note 24: Except TEST1, TEST2, and TEST3 pins.

4.3.8 Switching characteristics

Ta=-40 to 85°C, AVDD=DVDD=2.7~5.25V,
CL=20pF, XCLK=12.9024MHz

Item	Symbol	Pin	MIN	TYP	MAX	Unit	Reference
Serial Clock Frequency	f_{SCLK}	SCLK			4	MHz	
"H" pulse width	t_{SCKH}	SCLK	100			ns	Fig.1
	t_{OUTH}	RPO,TPO RQO,TQO			59.5 ±0.2	us	Fig.3 Note 25
"L" pulse width	t_{SCKL}	SCLK	100			ns	Fig.1
	t_{RSTL}	$\overline{\text{RST}}$	1			us	Fig.4
	t_{STBL}	$\overline{\text{STBY}}$	1				
	t_{DISL}	$\overline{\text{DIS}}$	1				
Hold time	t_{CCKH}	CS↑SCLK	100			ns	Fig.1
	t_{CKDH}	SCLK →DI	50				
Setup time	t_{CKDS}	SCLK →DI	50			ns	Fig.1
	t_{CCKS}	CS ↑SCLK	100				
Data output	t_{CKDV}	SCLK →DO			80	ns	Fig.2
	t_{CKDZ}	SCLK →DO			200		

Note 25: In case of PULSW11-0=000H (default).

In writing

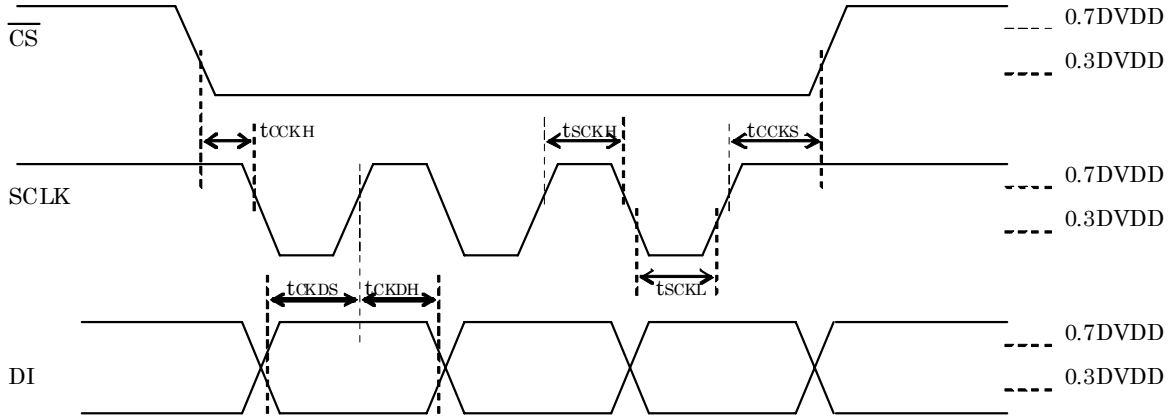


Fig.1

In reading

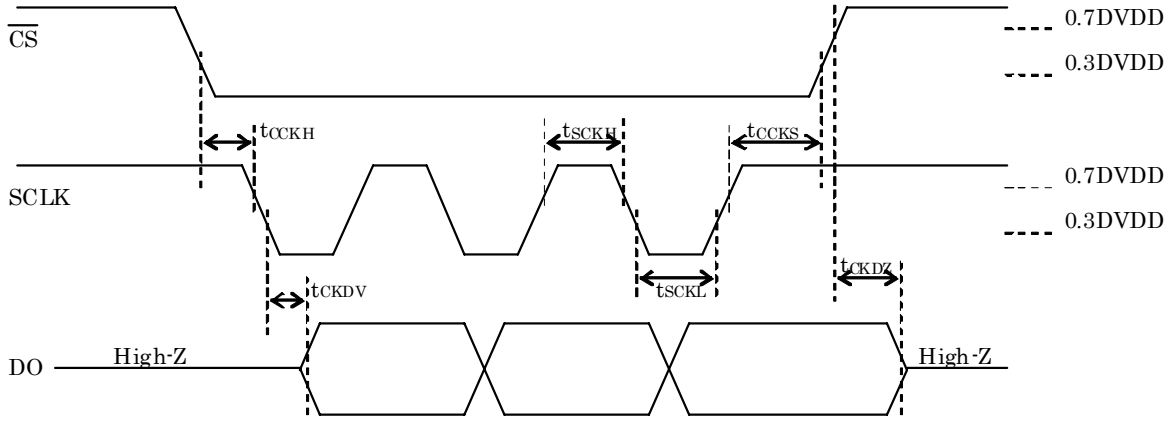


Fig.2

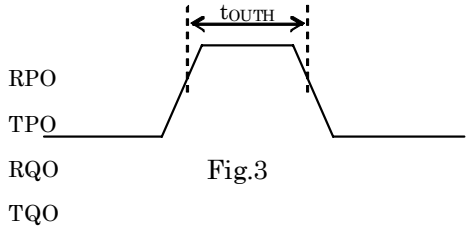


Fig.3

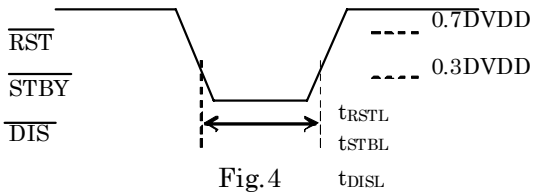


Fig.4

(Note) Reading and writing control is executed by commands of Control setting register, ADD.'21h'.

5. Function

5.1 Power on sequence

Operation phase	Comment
Ph1 $\overline{\text{RST}}$: L	Operation of all circuits including serial interface and oscillator circuits is halted and digital circuits including input / output register, control register and data register are initialized. At the same time F1, F2, F3, RPO, TPO, RQO,TQO, TPST, RQST and TQST becomes "L" level and DO becomes high impedance state.
Ph2 $\overline{\text{STBY}}$: L $\overline{\text{RST}}$: H	A serial interface circuit (input / output register) becomes active and it is possible to write in and read registers.
Ph3 $\overline{\text{DIS}}$: L $\overline{\text{STBY}}$: H $\overline{\text{RST}}$: H	All circuits except active power to frequency conversion circuit and reactive power to frequency conversion circuit become active. At this moment, RPO, TPO, RQO, TQO, RPST, TPST, RQST and TQST keeps "L" level. Oscillator circuit starts oscillation with $\overline{\text{RST}}$ = $\overline{\text{STBY}}$ = "H" and ADC sequence is started. It normally needs **300mS** before oscillation frequency and HPF are stabilized. The accuracy of ADC and calibration is not guaranteed during this period.
Ph4 $\overline{\text{DIS}}$: H $\overline{\text{STBY}}$: H $\overline{\text{RST}}$: H	All circuits become active, but the changing of the state from Ph3 to Ph4 must be done after 300mS are being elapsed in Ph3 state.

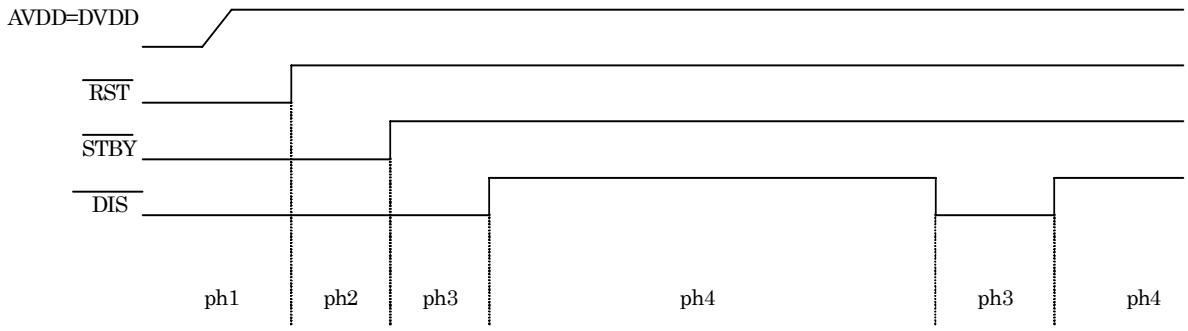


Fig.5 Power on sequence

5.2 Registers

5.2.1 Writing data into registers

It is possible to access a serial interface circuit with $\overline{RST}$ = "H", $\overline{CS}$ = "L".

By applying a serial clock at SCLK pin, input data is written into an input shift register. Input data consists of 7 bits of address, one bit "L" level writing command and 16 bits data strings.

The state of DI is sampled at rising edge of SCLK for 24 times after $\overline{CS}$ = "L" and transferred into the shift register. 16 bits data, which have been written into input shift data register will be transferred to the corresponding control register at the rising edge of $\overline{CS}$.

In a case that the number of clocks of SCLK is either less than 24 times or more than 25 times, input data will not be transferred into the corresponding control register.
The number of clocks of SCLK should be applied for 24 times even if the writing data consist of less than 16 bits format. And SCLK must be started at "H" state and ended at "H" state.

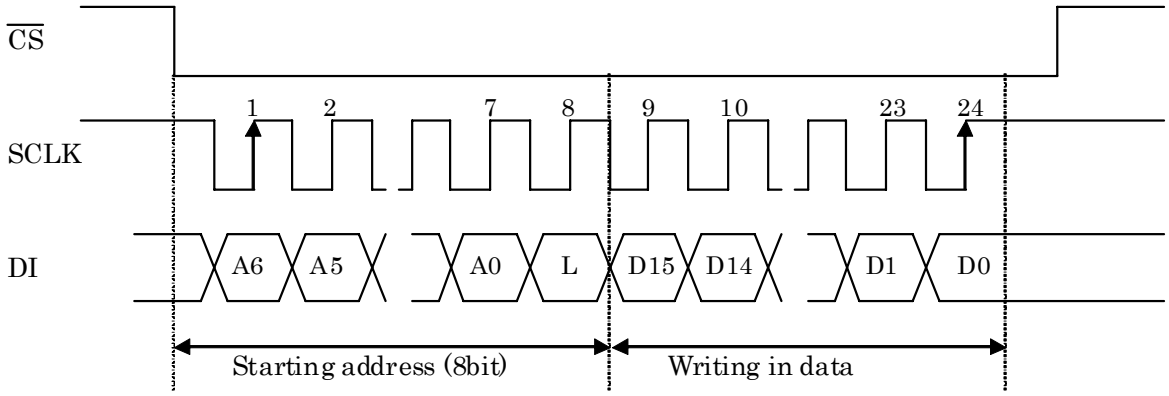


Fig.6 writing timing to registers

5.2.2 Reading data from registers

It is possible to access a serial interface circuit with $\overline{RST}$ = "H", $\overline{CS}$ = "L".

By applying a serial clock at SCLK pin, input data is written into an input shift register. Input data consists of 7 bits of address, one-bit "H" level reading command is followed.

The state of DI is sampled at rising edge of SCLK for 8 times after $\overline{CS}$ = "L", transferred into the shift register and specified the starting address.

In the starting address, the first 7 bits show the address of the control register which data should be stored and the next 1 bit shows either reading or writing. If the bit is "H", it means reading. If the bit is "L", it means writing.

In case that data specified with only one address is read (when ADD. '21h', bit1='1'), 16 bit data which is specified by reading indication register is loaded into the shift register from the controlling register at the first falling edge of SCLK following after the starting address and data is output at DO pin. After that, data is continuously output at every SCLK's falling edge and 16-bit data, which have been loaded into the output shift register are output.

Furthermore, the next 16-bit data at the next address are output if SCLK is input continuously. This makes it possible to read data from registers continuously without readdressing.

If SCLK is applied even after, data at the last address ADD. '59h' being output, the LSI outputs "L" as far as $\overline{CS}$ pin remains "L". DO pin becomes high impedance state when $\overline{CS}$ pin is controlled at "H" state. In a case that $\overline{CS}$ pin becomes "H" state before all data being output, DO pin becomes high impedance state and reading procedure is halted.
In addition, SCLK must be started at "H" state and ended at "H" state.

When the data loading period into the output register and data renewal period coincide each other, the bit15 (INVALID) of data at ADD. '21h' becomes "H" level. The INVALID bit at ADD. '21h' keeps "H" level until the content of ADD. '21h' will have been read, and it will be cleared after the reading.

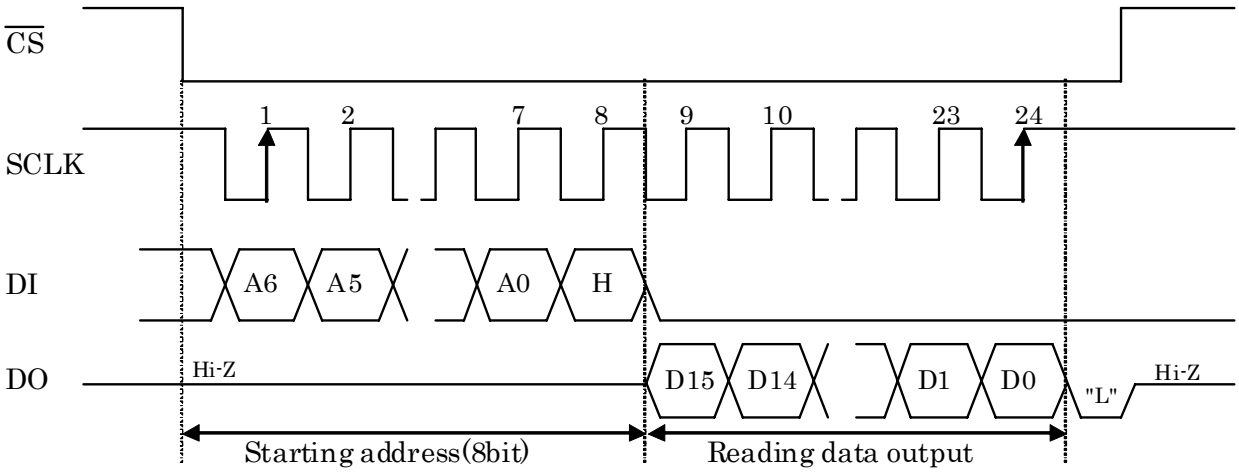


Fig.7 Reading timing from controlling registers

Initialization of registers

All registers are initialized and the initial values are loaded with "L" level at $\overline{RST}$ pin.

5.2.3 Mapping of controlling registers

[Readable and writable registers]

Initial value of controlling registers below is set to comply with Japanese standard. In a case that the LSI is used to comply with IEC standard, initial value of some registers should be modified. Please refer to the chapter 5.5, which describes the way of the system calibration in IEC mode.

Address A6-0	R/W	Symbol	Name	Initial value
00h	R/W	RPR	RP rated active power threshold value	9999h
01h				00C9h
02h	R/W	TPR	TP rated active power threshold value	9999h
03h				00C9h
04h	R/W	RQR	RQ rated reactive power threshold value	9999h
05h				00C9h
06h	R/W	TQR	TQ rated reactive power threshold value	9999h
07h				00C9h
08h	R/W	RPST/TPST/ RQST/TQST	RP/TP/RQ/TQ starting power threshold value for Japanese specification	1111h
09h	R/W	B2B	B2 balance value	0000h
0Ah	R/W	B3B	B3 balance value	0000h
0Bh	R/W	RPL/RQL	RP/RQ light load value	0000h
0Ch	R/W	TPL/TQL	TP/TQ light load value	0000h
0Dh	R/W	PFCN1	N1 power factor adjustment value	0000h
0Eh	R/W	PFCN2	N2 power factor adjustment value	0000h
0Fh	R/W	PFCN3	N3 power factor adjustment value	0000h
10h	R/W	PGAV1/PGAI1	PGA1 gain	0401h
11h	R/W	PGAV2/PGAI2	PGA2 gain	0401h
12h	R/W	PGAV3/PGAI3	PGA3 gain	0401h
13h	R/W	VTHR1/VTHF1	F1 threshold value	2B2Dh
14h	R/W	VTHR2/VTHF2	F2 threshold value	2B2Dh
15h	R/W	VTHR3/VTHF3	F3 threshold value	2B2Dh
16h	R/W	FULV1/FULI1	Full scale adjustment 1	0000h
17h	R/W	FULV2/FULI2	Full scale adjustment 2	0000h
18h	R/W	FULV3/FULI3	Full scale adjustment 3	0000h
19h	R/W	VOFF	Voltage offset	0000h
1Ah	R/W			0000h
1Bh	R/W	IOFF	Current offset	0000h
1Ch	R/W			0000h
1Dh	R/W	PWADD	Power addition able or disable control	0000h
1Eh	R/W	SENDOU	Creeping current threshold value for IEC specification	003Ah
1Fh	R/W	PULSW	Pulse width of output powers for IEC specification	0000h
20h	R/W	FUNC_SET	Function setting	0000h
21h	R/W	CONTL_SET	Control setting	0000h

[Read only registers]

Address A6-0	R/W	Symbol	Name	Initial value
22h	R	V1AD	V(voltage)1 instantaneous value	0000h
23h	R	V2AD	V(voltage)2 instantaneous value	0000h
24h	R	V3AD	V(voltage)3 instantaneous value	0000h
25h	R	I1HAD	I(current)1 instantaneous value (upper bits)	0000h
26h	R	I2HAD	I(current)2 instantaneous value (upper bits)	0000h
27h	R	I3HAD	I(current)3 instantaneous value (upper bits)	0000h
28h	R	ILAD	I1/I2/I3 instantaneous value (lower bits)	0000h
29h	R	V1RMS	V(voltage)1 RMS value	0000h
2Ah	R	V2RMS	V(voltage)2 RMS value	0000h
2Bh	R	V3RMS	V(voltage)3 RMS value	0000h
2Ch	R	I1RMS	I(current)1 RMS value	0000h
2Dh	R	I2RMS	I(current)2 RMS value	0000h
2Eh	R	I3RMS	I(current)3 RMS value	0000h
2F			Reserved	
30h	R	P1	P1 instantaneous active power	0000h
31h				0000h
32h	R	P2	P2 instantaneous active power	0000h
33h				0000h
34h	R	P3	P3 instantaneous active power	0000h
35h				0000h
36h	R	PSUM	Total instantaneous active power	0000h
37h				0000h
38h	R	Q1	Q1 instantaneous reactive power	0000h
39h				0000h
3Ah	R	Q2	Q2 instantaneous reactive power	0000h
3Bh				0000h
3Ch	R	Q3	Q3 instantaneous reactive power	0000h
3Dh				0000h
3Eh	R	QSUM	Total instantaneous reactive power	0000h
3Fh				0000h
40h	R	PTOTR	All total instantaneous active power (Receiving)	0000h
41h				0000h
42h	R	PTOTT	All total instantaneous active power (Transmitting)	0000h
43h				0000h
44h	R	QTOTR	All total instantaneous reactive power (Receiving)	0000h
45h				0000h
46h	R	QTOTT	All total instantaneous reactive power (Transmitting)	0000h
47h				0000h
48h	R	PPULSE	Active energy pulse	0000h
49h	R	QPULSE	Reactive energy pulse	0000h

Address A6-0	R/W	Symbol	Name	Initial value
4Ah	R	S1	S1 apparent power	0000h
4Bh	R	S2	S2 apparent power	0000h
4Ch	R	S3	S3 apparent power	0000h
4Dh	R	SSUM	Total apparent power	0000h
4Eh	R			0000h
4Fh	-	-	Reserved	0000h
50h	R	RXPO	RPO active power accumulated value	0000h
51h	R	TXPO	TPO active power accumulated value	0000h
52h	R	RXQO	RQO reactive power accumulated value	0000h
53h	R	TXQO	TQO reactive power accumulated value	0000h
54h	R	PF1	ϕ1 Power factor	0000h
55h	R	PF2	ϕ2 Power factor	0000h
56h	R	PF3	ϕ3 Power factor	0000h
57h	R	TEMP	Temperature	0080h
58h	R/W	TEMP_COEF	Temp. adjustment coefficient (Gain)	1C2Ah
59h	R/W	TOFFSET	Temp. adjustment coefficient (Offset)	0000h

Minute register mapping

Address A6-0	Data								Initial value
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	
00h (R/W)	RPR15-8								9999h
	RPR7-0								
01h (R/W)	-	-	-	-	-	-	RPR25-24		00C9h
	RPR23-16								
02h (R/W)	TPR15-8								9999h
	TPR7-0								
03h (R/W)	-	-	-	-	-	-	TPR25-24		00C9h
	TPR23-16								
04h (R/W)	RQR15-8								9999h
	RQR7-0								
05h (R/W)	-	-	-	-	-	-	RQR25-24		00C9h
	RQR23-16								
06h (R/W)	TQR15-8								9999h
	TQR7-0								
07h (R/W)	-	-	-	-	-	-	TQR25-24		00C9h
	TQR23-16								
08h (R/W)	TQST3-0				RQST3-0				1111h
	TPST3-0				RPST3-0				
09h (R/W)	-	-	-	-	B2B11-8				0000h
	B2B7-0								
0Ah (R/W)	-	-	-	-	B3B11-8				0000h
	B3B7-0								
0Bh (R/W)	RQL7-0								0000h
	RPL7-0								
0Ch (R/W)	TQL7-0								0000h
	TPL7-0								
0Dh (R/W)	-	-	-	-	-	-	PFCN1_9-8		0000h
	PFCN1_7-0								
0Eh (R/W)	-	-	-	-	-	-	PFCN2_9-8		0000h
	PFCN2_7-0								
0Fh (R/W)	-	-	-	-	-	-	PFCN3_9-8		0000h
	PFCN3_7-0								

Address A6-0	Data								Initial value
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	
10h (R/W)	-	-	PGAI1_5-0						0401h
	-	-	-	-	-	PGAV1_2-0			
11h (R/W)	-	-	PGAI2_5-0						0401h
	-	-	-	-	-	PGAV2_2-0			
12h (R/W)	-	-	PGAI3_5-0						0401h
	-	-	-	-	-	PGAV3_2-0			
13h (R/W)	VTHF1_7-0								2B2Dh
	VTHR1_7-0								
14h (R/W)	VTHF2_7-0								2B2Dh
	VTHR2_7-0								
15h (R/W)	VTHF3_7-0								2B2Dh
	VTHR3_7-0								
16h (R/W)	FULI1_7-0								0000h
	FULV1_7-0								
17h (R/W)	FULI2_7-0								0000h
	FULV2_7-0								
18h (R/W)	FULI3_7-0								0000h
	FULV3_7-0								
19h (R/W)	VOFF15-8								0000h
	VOFF7-0								
1A (R/W)	-	-	-	-	-	-	-	-	0000h
	VOFF23-16								
1Bh (R/W)	IOFF15-8								0000h
	IOFF7-0								
1Ch (R/W)	-	-	-	-	-	-	-	-	0000h
	IOFF23-16								
1Dh (R/W)	-	QSSEL	S3DIS	S2DIS	S1DIS	Q3DIS	Q2DIS	Q1DIS	0000h
	-	-	-	-	-	P3DIS	P2DIS	P1DIS	
1Eh (R/W)	-	-	-	-	-	-	-	SENDOU8	003Ah
	SENDOU7-0								
1Fh (R/W)	RDIV1-0		QODIS	PODIS	PULSW11-8				0000h
	PULSW7-0								

Address A6-0	Data								Initial value
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	
20h (R/W)	-	-	ZSI3	ZSI2	ZSI1	ZSV3	ZSV2	ZSV1	0000h
	CAL	PFSEL	SSEL	IEC	HPF	TEMP	FULLI	FULLV	
21h (R/W)	INVALID	-	-	-	-	-	-	-	0000h
	-	-	RMSRD1-0		ADRD1-0		RDY1-0		
22h (R)	V1AD15-8								0000h
	V1AD7-0								
23h (R)	V2AD15-8								0000h
	V2AD7-0								
24h (R)	V3AD15-8								0000h
	V3AD7-0								
25h (R)	I1AD17-10								0000h
	I1AD9-2								
26h (R)	I2AD17-10								0000h
	I2AD9-2								
27h (R)	I3AD17-10								0000h
	I3AD9-2								
28h (R)	-	-	-	-	-	-	-	-	0000h
	-	-	I3AD1-0		I2AD1-0		I1AD1-0		
29h (R)	V1RMS15-8								0000h
	V1RMS7-2						-	-	
2Ah (R)	V2RMS15-8								0000h
	V2RMS7-2						-	-	
2Bh (R)	V3RMS15-8								0000h
	V3RMS7-2						-	-	
2Ch (R)	I1RMS15-8								0000h
	I1RMS7-0								
2Dh (R)	I2RMS15-8								0000h
	I2RMS7-0								
2Eh (R)	I3RMS15-8								0000h
	I3RMS7-0								
2Fh (R)	Reserved								0000h
	Reserved								

Address A6-0	Data								Initial value
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	
30h (R)	P1_15-8								0000h
	P1_7-0								
31h (R)	-	-	-	-	-	-	-	-	0000h
	-	-	-	-	P1_19-16				
32h (R)	P2_15-8								0000h
	P2_7-0								
33h (R)	-	-	-	-	-	-	-	-	0000h
	-	-	-	-	P2_19-16				
34h (R)	P3_15-8								0000h
	P3_7-0								
35h (R)	-	-	-	-	-	-	-	-	0000h
	-	-	-	-	P3_19-16				
36h (R)	PSUM15-8								0000h
	PSUM7-0								
37h (R)	-	-	-	-	-	-	-	-	0000h
	-	-	PSUM21-16						
38h (R)	Q1_15-8								0000h
	Q1_7-0								
39h (R)	-	-	-	-	-	-	-	-	0000h
	-	-	-	-	Q1_19-16				
3Ah (R)	Q2_15-8								0000h
	Q2_7-0								
3Bh (R)	-	-	-	-	-	-	-	-	0000h
	-	-	-	-	Q2_19-16				
3Ch (R)	Q3_15-8								0000h
	Q3_7-0								
3Dh (R)	-	-	-	-	-	-	-	-	0000h
	-	-	-	-	Q3_19-16				
3Eh (R)	QSUM15-8								0000h
	QSUM7-0								
3Fh (R)	-	-	-	-	-	-	-	-	0000h
	-	-	QSUM21-16						

Address A6-0	Data								Initial value
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	
40h (R)	PTOTR15-8								0000h
	PTOTR7-0								
41h (R)	-	-	-	-	-	-	-	-	0000h
	PTOTR23-16								
42h (R)	PTOTT15-8								0000h
	PTOTT7-0								
43h (R)	-	-	-	-	-	-	-	-	0000h
	PTOTT23-16								
44h (R)	QTOTR15-8								0000h
	QTOTR7-0								
45h (R)	-	-	-	-	-	-	-	-	0000h
	QTOTR23-16								
46h (R)	QTOTT15-8								0000h
	QTOTT7-0								
47h (R)	-	-	-	-	-	-	-	-	0000h
	QTOTT23-16								
48h (R)	PD	-	PPULSE13-8						0000h
	PPULSE7-0								
49h (R)	QD	-	QPULSE13-8						0000h
	QPULSE7-0								
4Ah (R)	S1_15-8								0000h
	S1_7-0								
4Bh (R)	S2_15-8								0000h
	S2_7-0								
4Ch (R)	S3_15-8								0000h
	S3_7-0								
4Dh (R)	SSUM15-8								0000h
	SSUM7-0								
4Eh (R)	-	-	-	-	-	-	-	-	0000h
	-	-	-	-	-	-	SSUM17-16		
4Fh (R)	Reserved								0000h
	Reserved								

Address A6-0	Data								Initial value
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	
50h (R)	RXPO15-8								0000h
	RXPO7-0								
51h (R)	TXPO15-8								0000h
	TXPO7-0								
52h (R)	RXQO15-8								0000h
	RXQO7-0								
53h (R)	TXQO15-8								0000h
	TXQO7-0								
54h (R)	-	PF1_14-8							0000h
	PF1_7-0								
55h (R)	-	PF2_14-8							0000h
	PF2_7-0								
56h (R)	-	PF3_14-8							0000h
	PF3_7-0								
57h (R)	-	-	-	-	-	-	-	-	0080h
	TEMP7-0								
58h (R/W)	-	-	-	TCOEF12-8					1C2Ah
	TCOEF7-0								
59h (R/W)	-	-	-	-	-	-	-	-	0000h
	-	-	-	TOFFSET4-0					

5.2.4 Controlling registers

Rated power threshold value setting (ADD. 00h, 01h, 02h, 03h, 04h, 05h, 06h, 07h)

Address A6-0	Data								Initial value
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	
00h (R/W)	RPR15-8 (Same as below)								9999h
	RPR7-0 (Rated active power threshold value at receiving mode)								
01h (R/W)	-	-	-	-	-	-	RPR25-24 (Same as below)		00C9h
	RPR23-16 (Rated active power threshold value at receiving mode)								
02h (R/W)	TPR15-8 (Same as below)								9999h
	TPR7-0 (Rated active power threshold value at transmitting mode)								
03h (R/W)	-	-	-	-	-	-	TPR25-24 (Same as below)		00C9h
	TPR23-16 (Rated active power threshold value at transmitting mode)								
04h (R/W)	RQR15-8 (Same as below)								9999h
	RQR7-0 (Rated reactive power threshold value at receiving mode)								
05h (R/W)	-	-	-	-	-	-	RQR25-24 (Same as below)		00C9h
	RQR23-16 (Rated reactive power threshold value at receiving mode)								
06h (R/W)	TQR15-8 (Same as below)								9999h
	TQR7-0 (Rated reactive power threshold value at transmitting mode)								
07h (R/W)	-	-	-	-	-	-	TQR25-24 (Same as below)		00C9h
	TQR23-16 (Rated reactive power threshold value at transmitting mode)								

[RP Rated active power threshold value] This is the threshold value for producing the pulse of active power at receiving mode.

The value should be 0000000h ≤ W_{RPR} ≤ 3FFFFFFh

[TP Rated active power threshold value] This is the threshold value for producing the pulse of active power at transmitting mode.

0000000h ≤ W_{TPR} ≤ 3FFFFFFh

[RQ Rated reactive power threshold value] This is the threshold value for producing the pulse of reactive power at receiving mode.

0000000h ≤ W_{RQR} ≤ 3FFFFFFh

[TQ Rated reactive power threshold value] This is the threshold value for producing the pulse of reactive power at transmitting mode.

0000000h ≤ W_{TQR} ≤ 3FFFFFFh

The initial value of RP, TP, RQ and TQ is set to meet the Japanese specification. 1000 pulses are output for one second when the half of full-scale signal is applied at each voltage and current input of three phases. It is needed to change these values into 3225h to meet IEC specification.

Starting power threshold value setting (ADD. 08h)

This value should be modified to 0FFFh to meet IEC standard.

Address A6 -0	Data								Initial value
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	
08h (R/W)	TQST3-0 (TQ starting power threshold value)				RQST3-0 (RQ starting power threshold value)				1111h
	TPST3-0 (TP starting power threshold value)				RPST3-0 (RP starting power threshold value)				

RP starting power threshold value setting

Setting value				Starting power threshold value (Sec)	Function
bit3	bit2	bit1	bit0		
0	0	0	0	0.70	When "L" level pulse width at RPO pin is narrower than the starting power threshold value, the level at RPST pin becomes "H" level at the next rising edge of RPO pulse. When "L" level pulse width at RPO pin is wider than the starting power threshold value, the level at RPST pin becomes "L" level after the starting power threshold value.
0	0	0	1	0.75	
0	0	1	0	0.80	
0	0	1	1	0.85	
0	1	0	0	0.90	
0	1	0	1	0.95	
0	1	1	0	1.00	
0	1	1	1	1.05	
1	X	X	X	0	Regardless of the value at bit2 to bit0, '0' second is selected as the starting power threshold value. The level of RPST becomes "H" when the value of XP + RPL is positive. The level of RPST becomes "L" when the value of XP + RPL is negative.

TP starting power threshold value setting

Setting value				Starting power threshold value (Sec)	Function
bit7	bit6	bit5	bit4		
0	0	0	0	0.70	When "L" level pulse width at TPO pin is narrower than the starting power threshold value, the level at TPST pin becomes "H" level at the next rising edge of TPO pulse. When "L" level pulse width at TPO pin is wider than the starting power threshold value, the level at TPST pin becomes "L" level after the starting power threshold value.
0	0	0	1	0.75	
0	0	1	0	0.80	
0	0	1	1	0.85	
0	1	0	0	0.90	
0	1	0	1	0.95	
0	1	1	0	1.00	
0	1	1	1	1.05	
1	X	X	X	0	Regardless of the value at bit6 to bit4, '0' second is selected as the starting power threshold value. The level of TPST becomes "H" when the value of -XP + TPL is positive. The level of TPST becomes "L" when the value of -XP + TPL is negative.

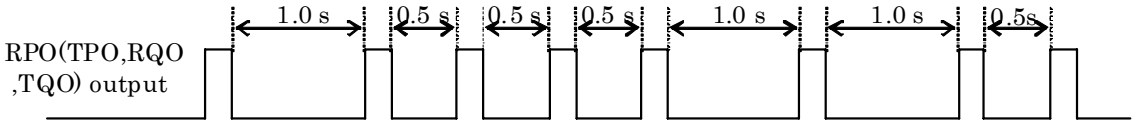
RQ starting power threshold value setting

Setting value				Starting power threshold value (Sec)	Function
bit11	bit10	bit9	bit8		
0	0	0	0	0.70	When "L" level pulse width at RQO pin is narrower than the starting power threshold value, the level at RQST pin becomes "H" level at the next rising edge of RQO pulse. When "L" level pulse width at RQO pin is wider than the starting power threshold value, the level at RQST pin becomes "L" level after the starting power threshold value.
0	0	0	1	0.75	
0	0	1	0	0.80	
0	0	1	1	0.85	
0	1	0	0	0.90	
0	1	0	1	0.95	
0	1	1	0	1.00	
0	1	1	1	1.05	
1	X	X	X	0	Regardless of the value at bit10 to bit8, '0' second is selected as the starting power threshold value. The level of RQST becomes "H" when the value of XQ + RQL is positive. The level of RQST becomes "L" when the value of XQ + RQL is negative.

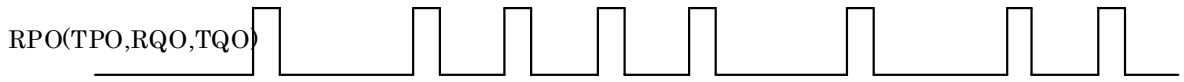
TQ starting power threshold value setting

Setting value				Starting power threshold value (Sec)	Function
bit15	bit14	bit13	bit12		
0	0	0	0	0.70	When "L" level pulse width at TQO pin is narrower than the starting power threshold value, the level at TQST pin becomes "H" level at the next rising edge of TQO pulse. When "L" level pulse width at TQO pin is wider than the starting power threshold value, the level at TQST pin becomes "L" level after the starting power threshold value.
0	0	0	1	0.75	
0	0	1	0	0.80	
0	0	1	1	0.85	
0	1	0	0	0.90	
0	1	0	1	0.95	
0	1	1	0	1.00	
0	1	1	1	1.05	
1	X	X	X	0	Regardless of the value at bit14 to bit12, '0' second is selected as the starting power threshold value. The level of TQST becomes "H" when the value of -XQ + TQL is positive. The level of TQST becomes "L" when the value of -XQ + TQL is negative.

Initial value of starting power threshold value of TP, RP, TQ and RQ is set at 0.75 second.



When starting power threshold value is set to "0" second,



RPST,TPST,RQST,TQST The polarity of XP+RPL (-XP+TPL,XQ+RQL,-XQ+TQL)

When starting power threshold value is set "0.75" second in this case,

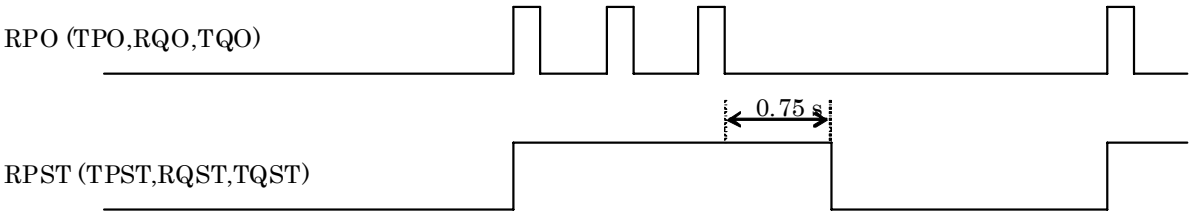


Fig.6 Output waveform of RPST(TPST,RQST,TQST)

Balance value setting (ADD. 09h, 0Ah)

Address A6-0	Data																Initial value
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	
09h (R/W)	-	-	-	-	B2 balance value												X000h
0Ah (R/W)	-	-	-	-	B3 balance value												X000h

B2 balance value: the value to adjust the gain of V2 against V1

B3 balance value: the value to adjust the gain of V3 against V1

The gain can be adjusted from 0 times to (2-1/2048) times.

When the value is '000h', the gain is '1'.

The value should be 000h ≤ B2 balance value, B3 balance value ≤ FFFh

Setting value	Gain
7FFh	1+ 1/2 + 1/4 + 1/8 + … + 1/2048
~	
400h	1+ 1/2 (1.5)
~	
200h	1+ 1/4 (1.25)
1FFh	1+ 1/8 + 1/16 + … + 1/2048
~	
100h	1+ 1/8 (1.125)
0FFh	1+ 1/16 + 1/32 + … + 1/2048
~	
001h	1+ 1/2048
000h	1
FFFh	1- 1/2048
FFEh	1 – 1/1024
~	
F01h	1 - 1/16 - 1/32 - … - 1/2048
F00h	1 - 1/8 (0.875)
~	
E00h	1 - 1/4 (0.75)
~	
C00h	1 - 1/2 (0.5)
~	
800h	1 - 1 (0)

Do not set the value to 800h. This value makes the scale '0', which is invalid.
Initial value of B2 balance and B3 balance is set at ×1.

Light load value setting (ADD. 0Bh, 0Ch)

Address A6-0	Data																Initial value
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	
0Bh(R/W)	RQ light load value								RP light load value								0000h
0Ch(R/W)	TQ light load value								TP light load value								0000h

RP light load value, RQ light load value: the value is used to adjust the offset at RP side or RQ side in light load mode.

Value	Offset
7Fh	+31.75
7Eh	+31.5
~	:
01h	+0.25
00h	0
FFh	-0.25
~	:
81h	-31.75
80h	-32

TP light load value, TQ light load value: the value is used to adjust the offset at TP side or TQ side in light load mode.

Value	Offset
7Fh	+31.75
7Eh	+31.5
~	:
01h	+0.25
00h	0
FFh	-0.25
~	:
81h	-31.75
80h	-32

The initial value of each light load is set at '0'.

Power factor adjustment value setting (ADD. 0Dh, 0Eh, 0Fh)

Address A6-0	Data								Initial value
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	
0Dh (R/W)	-	-	-	-	-	-	PFCN1_9-8 (N1_Adj.)		0000h
	PFCN1_7-0 (N1_Adj.)								
0Eh (R/W)	-	-	-	-	-	-	PFCN2_9-8 (N2_Adj)		0000h
	PFCN2_7-0 (N2_Adj)								
0Fh (R/W)	-	-	-	-	-	-	PFCN3_9-8 (N3_Adj)		0000h
	PFCN3_7-0 (N3_Adj)								

N1_Adjust: This value is used to delay the starting point of AD conversion at voltage side against current side in the AD conversion of [(I1P) – (I1N), (V1P) – (VIN)].

Value	Delay (XCLK=12.9024MHz)
1EFh	7920 XCLK (613.84us)
1EEh	7904XCLK (612.60us)
~	
01h	16 XCLK (1.24us)
00h	0 XCLK (0us)
3FFh	-16XCLK (-1.24us)
~	
212h	-7904XCLK (-612.60us)
211h	-7920XCLK (-613.84us)

N2_Adjust: This value is used to delay the starting point of AD conversion at voltage side against current side in the AD conversion of [(I2P) – (I2N), (V2P) – (VIN)].

Value	Delay (XCLK=12.9024MHz)
1EFh	7920 XCLK (613.84us)
1EEh	7904 XCLK (612.60us)
~	
01h	16 XCLK (1.24us)
00h	0 XCLK (0us)
3FFh	-16XCLK (-1.24us)
~	
212h	-7904XCLK (-612.60us)
211h	-7920XCLK (-613.84us)

N3_Adjust: This value is used to delay the starting point of AD conversion at voltage side against current side in the AD conversion of [(I3P) – (I3N), (V3P) – (VIN)].

Value	Delay (XCLK=12.9024MHz)
1EFh	7920 XCLK (613.84us)
1EEh	7904XCLK (612.60us)
~	
01h	16 XCLK (1.24us)
00h	0 XCLK (0us)
3FFh	-16XCLK (-1.24us)
~	
212h	-7904XCLK (-612.60us)
211h	-7920XCLk (-613.84us)

In a case that the value which is more than '1EFh' is set at the above register, the delay will be 7920XCLK . And if the value is less than '211h', the delay will be -7920XCLK.

Initial value of each power factor adjustment value is set '0', which means no adjustment.

PGA setting(ADD. 10h, 11h, 12h)

Address A6-0	Data								Initial value
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	
10h (R/W)	-	-	PGAI1_5-0 (CH1 current side PGA)						0401h
	-	-	-	-	-	PGAV1_2-0 (CH1 voltage side PGA)			
11h (R/W)	-	-	PGAI2_5-0 (CH2 current side PGA)						0401h
	-	-	-	-	-	PGAV2_2-0 (CH2 voltage side PGA)			
12h (R/W)	-	-	PGAI3_5-0 (CH3 current side PGA)						0401h
	-	-	-	-	-	PGAV3_2-0 (CH3 voltage side PGA)			

PGAV1 (bit2 – 0): to select CH1voltage side PGA

Value			Gain	Analog input Full scale voltage
bit2	bit1	bit0		
0	0	0	x1	±1.0V
0	0	1	x1	±1.0V
0	1	0	x2	±0.5V
0	1	1	x3	±0.333V
1	0	0	x4	±0.25V

PGAI1 (bit13 – 8): to select CH1 current side PGA

Value						Gain	Analog input Full scale voltage
bit13	bit12	bit11	bit10	bit9	bit8		
0	0	0	0	0	0	x1	±1.0V
0	0	0	0	0	1	x1	±1.0V
0	0	0	0	1	0	x2	±0.5V
0	0	0	0	1	1	x3	±0.333V
0	0	0	1	0	0	x4	±0.25V
0	0	0	1	0	1	x5	±0.20V
-	-	-	-	-	-	-	-
0	0	1	0	0	0	x8	±0.125V
-	-	-	-	-	-	-	-
0	0	1	1	0	0	x12	±0.0833V
-	-	-	-	-	-	-	-
0	1	0	0	1	0	x18	±0.0556V
-	-	-	-	-	-	-	-
0	1	1	0	0	0	x24	±0.0417V
-	-	-	-	-	-	-	-
0	1	1	1	1	1	x31	±0.0323V
1	0	0	0	0	0	x32	±0.03125V

PGAV2 (bit2-0): to select CH2 voltage side PGA

Value			Gain	Analog input Full scale voltage
bit2	bit1	bit0		
0	0	0	x1	±1.0V
0	0	1	x1	±1.0V
0	1	0	x2	±0.5V
0	1	1	x3	±0.333V
1	0	0	x4	±0.25V

PGAI2 (bit13-8): to select CH2 current side PGA

Value						Gain	Analog input Full scale input
bit13	bit12	bit11	bit10	bit9	bit8		
0	0	0	0	0	0	x1	±1.0V
0	0	0	0	0	1	x1	±1.0V
0	0	0	0	1	0	x2	±0.5V
0	0	0	0	1	1	x3	±0.333V
0	0	0	1	0	0	x4	±0.25V
0	0	0	1	0	1	x5	±0.20V
-	-	-	-	-	-	-	:
0	0	1	0	0	0	x8	±0.125V
-	-	-	-	-	-	-	:
0	0	1	1	0	0	x12	±0.0833V
-	-	-	-	-	-	-	:
0	1	0	0	1	0	x18	±0.0556V
-	-	-	-	-	-	-	:
0	1	1	0	0	0	x24	±0.0417V
-	-	-	-	-	-	-	:
0	1	1	1	1	1	x31	±0.0323V
1	0	0	0	0	0	x32	±0.03125V

PGAV3 (bit2-0): to select CH3 voltage side PGA

Value			Gain	Analog input Full scale input
bit2	bit1	bit0		
0	0	0	x1	±1.0V
0	0	1	x1	±1.0V
0	1	0	x2	±0.5V
0	1	1	x3	±0.333V
1	0	0	x4	±0.25V

PGAI3 (bit13-8): to select CH3 current side PGA

Value						Gain	Analog input Full scale voltage
bit13	bit12	bit11	bit10	bit9	bit8		
0	0	0	0	0	0	x1	±1.0V
0	0	0	0	0	1	x1	±1.0V
0	0	0	0	1	0	x2	±0.5V
0	0	0	0	1	1	x3	±0.333V
0	0	0	1	0	0	x4	±0.25V
0	0	0	1	0	1	x5	±0.20V
-	-	-	-	-	-	-	-
0	0	1	0	0	0	x8	±0.125V
-	-	-	-	-	-	-	-
0	0	1	1	0	0	x12	±0.0833V
-	-	-	-	-	-	-	-
0	1	0	0	1	0	x18	±0.0556V
-	-	-	-	-	-	-	-
0	1	1	0	0	0	x24	±0.0417V
-	-	-	-	-	-	-	-
0	1	1	1	1	1	x31	±0.0323V
1	0	0	0	0	0	x32	±0.03125V

Initial value of voltage side PGA on each phase is set x1 and initial value of current side PGA on each phase is set x4.

Threshold value of frequency pulse output setting (ADD. 13h, 14h, 15h)

Address A6-0	Data								Initial Value
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	
13h (R/W)	VTHF1_7-0 (F1 falling threshold)								2B2Dh
	VTHR1_7-0 (F1 rising threshold)								
14h (R/W)	VTHF2_7-0 (F2 falling threshold)								2B2Dh
	VTHR2_7-0 (F2 rising threshold)								
15h (R/W)	VTHF3_7-0 (F3 falling threshold)								2B2Dh
	VTHR3_7-0 (F3 rising threshold)								

F1 rising threshold value: This is the rising threshold value of F1 output to determine the frequency based on AD conversion value of V1(voltage input1). F1pin outputs "H" level over the threshold value.

The value should be 00h ≤ VTH1R ≤ 7Fh.

Initial value is set about 70% of voltage input1 at initial value of rated active power register.

Value	Threshold
7Fh	7F00h
7Eh	7E00h
-	-
02h	0200h
01h	0100h
00h	0000h

F1 falling threshold value: This is the falling threshold value of F1 output to determine the frequency based on AD conversion value of V1 (voltage input1). F1pin outputs 'L' level under the threshold value.
The value should be 00h ≤ VTH1F ≤ 7Fh.
Initial value is set about 68% of voltage input at initial value of rated active power register in Japanese specification.

Value	Threshold
7Fh	7F00h
7Eh	7E00h
-	-
02h	0200h
01h	0100h
00h	0000h

The rising threshold value and falling threshold value of F2 and F3 are set in the same manner of F1 and have the same initial values of F1. In addition, it is ignored that even if '1' is written into the 'bit7' of the threshold register.

Full scale adjustment value setting (ADD. 16h, 17h, 18h)

Address A6-0	Data								Initial Value
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	
16h (R/W)	FULI1_7-0 (Current side CH1 full scale adjustment)								0000h
	FULV1_7-0 (Voltage side CH1 full scale adjustment)								
17h (R/W)	FULI2_7-0 (Current side CH2 full scale adjustment)								0000h
	FULV2_7-0 (Voltage side CH2 full scale adjustment)								
18h (R/W)	FULI3_7-0 (Current side CH3 full scale adjustment)								0000h
	FULV3_7-0 (Voltage side CH3 full scale adjustment)								

This register is to adjust the variations produced by PGA and / or VREF from ideal value so that the result of ADC has an ideal ADC code when a half of full-scale **DC** voltage, 0.5 V is applied to each voltage and current channel. When using this function, the gain of all voltage channels should be the same value as well as the gain of all current channels. The gain between current and voltage can be changed. It should be very careful for using this function because after the adjustment, every calculation including an instantaneous value, RMS value and active & reactive power is affected.
The adjustment of gain on voltage side is performed by setting '1' to bit0, FULLV of Function setting register,ADD.'20h'.
And the adjustment of gain on current side is performed by setting '1' to 'bit1', FULLI of Function setting register,ADD.'20h'.
After the execution of this command, the adjustment value can be read from ADD. '16h', '17h', '18h' respectively. It is also possible to set the values as well by writing the values into these registers directly.
Refer to the table below to confirm the relationship between setting value and adjustment value.

Value	Gain
7Fh	(1024+127)/1024 = 1.124023
7Eh	(1024+126)/1024 = 1.123047
~	~
01h	(1024+1)/1024 = 1.0009766
00h	(256+0)/ 256= 1.00
FFh	(1024-1)/1024 = 0.999023
FEh	(1024-2)/1024 = 0.998047
~	~
81h	(1024-127)/1024 = 0.875976
80h	(1024-128)/1024 = 0.875

V(voltage) offset adjustment setting (ADD. 19h, 1Ah)

Address A6-0	Data								Initial Value
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	
19h (R/W)	VOFF15-8 (V offset middle)								0000h
	VOFF7-0 (V offset lower)								
1A (R/W)	-	-	-	-	-	-	-	-	0000h
	VOFF23-16 (V offset higher)								

This register is for setting offset value of ADC at voltage side. The calibration is executed by setting '1' to bit7, CAL bit of Function setting register,ADD.'20h'. It is possible to read the V offset value after the calibration.

I(current) offset adjustment setting (ADD. 1Bh, 1Ch)

Address A6-0	Data								Initial Value
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	
1Bh (R/W)	IOFF15-8 (I offset middle)								0000h
	IOFF7-0 (I offset lower)								
1Ch (R/W)	-	-	-	-	-	-	-	-	0000h
	IOFF23-16 (I offset higher)								

This register is for setting offset value of ADC at current side. The calibration is executed by setting '1' to bit7, CAL bit of Function setting register, ADD. '20h'. It is possible to read the I offset value after the calibration.

Power addition "disable" setting (ADD. 1Dh)

Address A6-0	Data								Initial Value
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	
1Dh (R/W)	-	QSSEL	S3DIS	S2DIS	S1DIS	Q3DIS	Q2DIS	Q1DIS	0000h
	-	-	-	-	-	P3DIS	P2DIS	P1DIS	

This register enables the addition control of active power (P1/P2/P3), reactive power (Q1/Q2/Q3) and apparent power (S1/S2/S3) when power summation is executed. When '1' is set to the corresponding bit, the addition of the corresponding channel is canceled.
Initial setting is that power at each channel is summed in active power, reactive power and apparent power. And QSSEL, bit14 is to select either reactive power pulse, '0' or apparent power pulse,'1'. The initial setting of QSSEL is reactive power pulse.

IEC creeping value setting (ADD. 1Eh)

Address A6-0	Data								Initial Value
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	
1Eh (R/W)	-	-	-	-	-	-	-	SENDOU8	003Ah
	SENDOU7-0								

This register enables to set '0' at power input to pulse conversion block when the value of XP =P1+P2+P3, XQ=Q1+Q2+Q3 or XS=S1+S2+S3 is less than the setting value.
Initial value is '3Ah'. This means that power input to pulse conversion block is set '0' when the summation of power each channel is less than 0.0075% of full-scale value.
Since this value is writable, it is possible to modify the value.

IEC power pulse width setting (ADD. 1Fh)

Address A6-0	Data								Initial Value
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	
1Fh (R/W)	RDIV1-0		QODIS	PODIS	PULSW11-8 (IEC power pulse width higher)				0000h
	PULSW7-0 (IEC power pulse width lower)								

PULSW11-0 (bit11-0): This determines the IEC compliant power pulse width. The pulse width will be 59.5us x (setting value +1). It is possible to set the pulse width between 59.5us and 243.7ms. The initial value of pulse width is 59.5us, which comply with the Japanese standard.

PODIS (bit12): Active power pulse output disable. This stops the output of active power pulse when '1' is set. This does not stop the procedure of the conversion from power to pulse.

QODIS (bit13): Reactive power / apparent power pulse output disable. This stops the output of reactive power / apparent power when '1' is set. This does not stop the procedure of the conversion from power to pulse. Initial value of PODIS and QODIS is set to '0' respectively.

RDIV1-0 (bit15, bit14): This determines the frequency of accumulated addition. The frequency becomes 16.8kHz if the value is set '00',(initial value), becomes 8.4kHz if the value is set '01' and becomes 4.2kHz if the value is set '10'.

Function setting (ADD. 20h)

Address A6-0	Data								Initial Value
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	
20h (R/W)	-	-	ZSI3	ZSI2	ZSI1	ZSV3	ZSV2	ZSV1	0000h
	CAL	PFSEL	SSEL	IEC	HPF	TEMP	FULLI	FULLV	

FULLV (bit0): To set '1' in this bit when the full-scale adjustment for voltage side is to be executed. When the adjustment is completed successfully, this bit becomes '0' automatically. The initial value of this bit is set '0'.

FULLI (bit1): To set '1' in this bit when the full-scale adjustment for current side is to be executed. When the adjustment is completed, this bit becomes '0' automatically. The initial value of this bit is set '0'.

TEMP (bit2): To set '1' in this bit when the measurement of the temperature of the LSI is to be executed. When the measurement is completed, this bit becomes '0' automatically. The initial value of this bit is set '0'.

HPF (bit3): To set '1' in this bit when HPF is inserted into each voltage input and current input. This setting is enabled for all channels simultaneously. The initial value of this bit is set '0'.

IEC (bit4): To set '1' in this bit when IEC value ,ADD.'1Eh' is used as the creeping judgment value. The initial value of this bit is set '0', which means that the creeping judgment value complies with the Japanese standard.

SSEL (bit5): This bit is to select which type of apparent power is used. One is that the apparent power is derived from the calculation of active power and reactive power. The other is derived from the calculation of RMS voltage value and RMS current value. The initial value is set '0', which means that the apparent power is derived from the calculation of active power and reactive power.

PFSEL (bit6): In the calculation of power factor, this bit is to select which type of apparent power is used. The first one is to use the apparent power, which is derived from the calculation of active power and reactive power. The other is to select the apparent power, which is derived from RMS voltage and RMS current. The initial value is set '0', which means that the apparent power is derived from the calculation of active power and reactive power.

CAL (bit7): To set '1' in this bit when the calibration of the ADC at voltage side and current side is to be executed. When the calibration is completed successfully, this bit becomes '0' automatically. The initial value of this bit is set '0'.

ZSV1-ZSV3 (bit8-bit10): When setting each voltage input from CH1 through CH3 in a short mode, the corresponding bit should be set '1'. Initial value is set '0', which means that the corresponding bit is set NOT in a short mode.

ZSI1-ZSI3 (bit11-bit13): When setting each current input from CH1 through CH3 in a short mode, the corresponding bit should be set '1'. Initial value is set '0', which means that the corresponding bit is set NOT in a short mode.

Control setting (ADD. 21h)

Address A6-0	Data								Initial Value
	bit15	bit14	bit13	bit12	bit11	bit10	Bit9	bit8	
	bit7	bit6	bit5	bit4	bit3	bit2	Bit1	bit0	
21h (R/W)	INVALID	-	-	-	-	-	-	-	0000h
	-	-	RMSRD1-0		ADRD1-0		RDY1	RDY0	

RDY1-0 (bit1, bit0): These bits assign RDY pin of the LSI to the one of the instantaneous value registers, RMS value registers or other read-only registers. '00' (initial value) is for RMS registers,'01' is for instantaneous registers, '10' or '11' is for other read-only registers ,ADD.'22h' to '57h'. There is no need RDY_control for readable and writable registers, ADD. '00h' to '21h', '58h' and '59h'. When the collision is occurred between reading and writing without RDY control, INVALID (bit15) bit is set. This means that wrong data had been read. Initial value of INVALID bit is '00', which is RDY control for RMS.

ADRD1-0 (bit3, bit2) assign the renewal frequency of instantaneous values. '00' means that the renewal frequency is 3.15kHz, '01' is 1.575kHz frequency, '10' is 0.7875kHz. Initial value is 3.15kHz.

RMSRD1-0 (bit5, bit4) assign the renewal frequency of RMS values. '00' means that the renewal frequency is 3.15kHz, '01' is 1.575kHz frequency, '10' is 0.7875kHz. Initial value is 3.15kHz.

INVALID (bit15) is set when the collision is occurred between reading and writing controlling registers. When INVALID bit is set, it is needed to read the corresponding data again. This INVALID bit is cleared when this bit is read.

Instantaneous value (ADD. 22h, 23h, 24h, 25h, 26h, 27h, 28h)

Address A6-0	Data								Initial value
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	
22h (R)	V1AD15-8 (Higher bits of CH1 instantaneous voltage)								0000h
	V1AD7-0 (Lower bits of CH1 instantaneous voltage)								
23h (R)	V2AD15-8(Higher bits of CH2 instantaneous voltage)								0000h
	V2AD7-0 (Lower bits of CH2 instantaneous voltage)								
24h (R)	V3AD15-8(Higher bits of CH3 instantaneous voltage)								0000h
	V3AD7-0 (Lower bits of CH3 instantaneous voltage)								
25h (R)	I1AD17-10(Higher bits of CH1 instantaneous current)								0000h
	I1AD9-2 (Lower bits of CH1 instantaneous current)								
26h (R)	I2AD17-10(Higher bits of CH2 instantaneous current)								0000h
	I2AD9-2 (Lower bits of CH2 instantaneous current)								
27h (R)	I3AD17-10(Higher bits of CH3 instantaneous current)								0000h
	I3AD9-2 (Lower bits of CH3 instantaneous current)								
28h (R)	-	-	-	-	-	-	-	-	0000h
	-	-	I3AD1-0(Lowest bits of CH3 instant. current)		I2AD1-0(Lowest bits of CH2 instant. current)		I1AD1-0(Lowest bits of CH1 instant. current)		

These registers store the instantaneous value of each input voltage and current. Voltage is expressed in 16bit format and current is expressed in 18bit format.

RMS value (ADD. 29h, 2Ah, 2Bh, 2Ch, 2Dh, 2Eh)

Address A6-0	data								Initial value
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	
29h (R)	V1RMS15-8 (Higher bits of CH1 voltage RMS value)								0000h
	V1RMS7-2 (Lower bits of CH1 voltage RMS value)						-	-	
2Ah (R)	V2RMS15-8 (Higher bits of CH2 voltage RMS value)								0000h
	V2RMS7-2 (Lower bits of CH2 voltage RMS value)						-	-	
2Bh (R)	V3RMS15-8 (Higher bits of CH3 voltage RMS value)								0000h
	V3RMS7-2 (Lower bits of voltage RMS value)						-	-	
2Ch (R)	I1RMS17-10 (Higher bits of CH1 current RMS value)								0000h
	I1RMS9-2(Lower bits of CH1 current RMS value)								
2Dh (R)	I2RMS17-10(Higher bits of CH2 current RMS value)								0000h
	I2RMS9-2(Lower bits of CH2 current RMS value)								
2Eh (R)	I3RMS17-10(Higher bits of CH3 current RMS value)								0000h
	I3RMS9-2(Lower bits of CH3 current RMS value)								

These registers store the RMS value of each input voltage and each input current. Voltage is expressed in 14 bit format and Current is expressed in 16 bit format.

Active power value (ADD. 30h, 31h, 32h, 33h, 34h, 35h, 36h, 37h)

Address A6-0	data								Initial value
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	
30h (R)	P1_15-8 (Higher bits of CH1 active power)								0000h
	P1_7-0 (Lower bits of CH1 active power)								
31h (R)	-	-	-	-	-	-	-	-	0000h
	-	-	-	-	P1_19-16 (Highest bits of CH1 active power)				
32h (R)	P2_15-8 (Higher bits of CH2 active power)								0000h
	P2_7-0 (Lower bits of CH2 active power)								
33h (R)	-	-	-	-	-	-	-	-	0000h
	-	-	-	-	P2_19-16 (Highest bits of CH2 active power)				
34h (R)	P3_15-8 (Higher bits of CH3 active power)								0000h
	P3_7-0 (Lower bits of CH3 active power)								
35h (R)	-	-	-	-	-	-	-	-	0000h
	-	-	-	-	P3_19-16(Highest bits of CH3 active power)				
36h (R)	PSUM15-8(Higher bits of total active power (P1+P2+P3))								0000h
	PSUM7-0(Lower bits of total active power (P1+P2+P3))								
37h (R)	-	-	-	-	-	-	-	-	0000h
	-	-	PSUM21-16(Highest bits of total active power(P1+P2+P3))						

These registers store the active power value of each input channel. Each active power value is expressed in 20 bit format and total active power value is expressed in 22 bit format.

Reactive power value (ADD. 38h, 39h, 3Ah, 3Bh, 3Ch, 3Dh, 3Eh, 3Fh)

Address A6-0	data								Initial value
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	
38h (R)	Q1_15-8 (Higher bits of CH1 reactive power)								0000h
	Q1_7-0 (Lower bits of CH1 reactive power)								
39h (R)	-	-	-	-	-	-	-	-	0000h
	-	-	-	-	Q1_19-16 (Highest bits of CH1 reactive power)				
3Ah (R)	Q2_15-8 (Higher bits of CH2 reactive power)								0000h
	Q2_7-0 (Lower bits of CH2 reactive power)								
3Bh (R)	-	-	-	-	-	-	-	-	0000h
	-	-	-	-	Q2_19-16 (Highest bits of CH2 reactive power)				
3Ch (R)	Q3_15-8 (Higher bits of CH3 reactive power)								0000h
	Q3_7-0 (Lower bits of CH3 reactive power)								
3Dh (R)	-	-	-	-	-	-	-	-	0000h
	-	-	-	-	Q3_19-16 (Highest bits of CH3 reactive power)				
3Eh (R)	QSUM15-8 (Higher bits of total reactive power (Q1+Q2+Q3))								0000h
	QSUM7-0 (Lower bits of total reactive power (Q1+Q2+Q3))								
3Fh (R)	-	-	-	-	-	-	-	-	0000h
	-	-	QSUM21-16(Highest bits of total reactive power (Q1+Q2+Q3))						

These registers store the reactive power value of each input channel. Each reactive power value is expressed in 20 bit format and total reactive power value is expressed in 22 bit format.

All total active power value(ADD. 40h, 41h, 42h, 43h)

Address A6-0	data								Initial value
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	
40h (R)	PTOTR15-8 (Higher bits of all total receiving active power)								0000h
	PTOTR7-0 (Lower bits of all total receiving active power)								
41h (R)	-	-	-	-	-	-	-	-	0000h
	PTOTR23-16 (Highest bits of all total receiving active power)								
42h (R)	PTOTT15-8 (Higher bits of all total transmitting active power)								0000h
	PTOTT7-0 (Lower bits of all total transmitting active power)								
43h (R)	-	-	-	-	-	-	-	-	0000h
	PTOTT23-16 (Highest bits of all total transmitting active power)								

These registers store all total receiving active power value (P1+P2+P3+RPL) and all total transmitting active power value (P1+P2+P3+TPL). The value is expressed in 24 bit format

All total reactive power value (ADD. 44h, 45h, 46h, 47h)

Address A6-0	data								Initial value
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	
44h (R)	QTOTR15-8 (Higher bits of all total receiving reactive power)								0000h
	QTOTR7-0 (Lower bits of all total receiving reactive power)								
45h (R)	-	-	-	-	-	-	-	-	0000h
	QTOTR23-16 (Highest bits of all total receiving reactive power)								
46h (R)	QTOTT15-8 (Higher bits of all total transmitting reactive power)								0000h
	QTOTT7-0 (Lower bits of all total transmitting reactive power)								
47h (R)	-	-	-	-	-	-	-	-	0000h
	QTOTT23-16 (Highest bits of all total transmitting reactive power)								

These registers store all total receiving reactive power value (Q1+Q2+Q3+RQL) and all total transmitting reactive power value (Q1+Q2+Q3+TQL). The value is expressed in 24 bit format

Pulse count value of energy(ADD. 48h, 49h)

Address A6-0	Data								Initial value
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	
48h (R)	PD	-	PPULSE13 - 8						0000h
	PPULSE7-0								
49h (R)	QD	-	QPULSE13-8						0000h
	QPULSE7-0								

These registers store active energy pulse values and reactive energy pulse values for one second period. Both active energy pulse values (PPULSE13-PPULSE0) and reactive energy pulse values (QPULSE13-QPULSE0) are expressed in 14 bit format. If the pulse count value is overflowed, the count value is stopped with a maximum value. PD(ADD.'48h' :bit15) shows whether the active energy pulse is receiving pulse (PD='0') or transmitting pulse(PD='1') as same as QD(ADD.'49h':bit15) shows whether the reactive energy pulse is receiving pulse (QD='0') or transmitting pulse(QD='1').

'1' second timer is assumed that the frequency of using crystal is 12.9024MHz. If the frequency of using crystal is not 12.9024MHz but ,for example 12.8MHz, the number of pulse count will be '1008', which is equal to 12.9024MHz / 12.8MHz at the rated voltage and the rated current.

Apparent power value (ADD. 4Ah, 4Bh, 4Ch, 4Dh, 4Eh)

Address A6-0	Data								Initial value
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	
4Ah (R)	S1_15-8 (Higher bits of CH1 apparent power)								0000h
	S1_7-0 (Lower bits of CH1 apparent power)								
4Bh (R)	S2_15-8 (Higher bits of CH2 apparent power)								0000h
	S2_7-0 (Lower bits of CH2 apparent power)								
4Ch (R)	S3_15-8 (Higher bits of CH3 apparent power)								0000h
	S3_7-0 (Lower bits of CH3 apparent power)								
4Dh (R)	SSUM15-8 (Higher bits of total apparent power)								0000h
	SSUM7-0 (Lower bits of total apparent power)								
4Eh (R)	-	-	-	-	-	-	-	-	0000h
	-	-	-	-	-	-	SSUM17-16 (Highest bits of total apparent power)		

These registers store an apparent value (S1, S2, S3) on each phase and a total apparent power value. The value of apparent value on each phase is expressed in 16 bit format and the value of total apparent value is expressed in 18 bit format.

Accumulated power pulse value (ADD. 50h, 51h, 52h, 53h)

Address A6-0	Data								Initial value
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	
50h (R)	RXPO15-8 (Upper bits of RPO accumulated power pulse)								0000h
	RXPO7-0 (Lower bits of RPO accumulated power pulse)								
51h (R)	TXPO15-8 (Upper bits of TPO accumulated power pulse)								0000h
	TXPO7-0 (Lower bits of TPO accumulated power pulse)								
52h (R)	RXQO15-8 (Upper bits of RQO accumulated power pulse)								0000h
	RXQO7-0 (Lower bits of RQO accumulated power pulse)								
53h (R)	TXQO15-8(Upper bits of TQO accumulated power pulse)								0000h
	TXQO7-0 (Lower bits of TQO accumulated power pulse)								

These registers store upper 16 bits of accumulated power pulse. Each register is expressed in 16 bit format.

Power factor (54h, 55h, 56h)

Address A6-0	Data								Initial value
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	
54h (R)	-	PF1_14-8(CH1 power factor)							0000h
	PF1_7-0(CH1 power factor)								
55h (R)	-	PF2_14-8(CH2 power factor)							0000h
	PF2_7-0(CH2 power factor)								
56h (R)	-	PF3_14-8(CH3 power factor)							0000h
	PF3_7-0(CH3 power factor)								

These registers store power factors of CH1, CH2, CH3.Power factor is expressed by the value between -1 and +1. There are two different ways of calculating power factor.
The one is to use the apparent power, which is derived from active power and reactive power calculation. This selection of the calculation is the default setting. The other is to use the apparent power, which is derived from RMS voltage and RMS current calculation. The selection is made by the PFSEL (bit 6) bit of Function setting register,ADD.'20h'.
Power factor is expressed in two's complementary expression.
The polarity of the reactive power in each input express whether the θ being derived from power factor in each input is positve or nagative.
If bit3 of ADD. '39h' or '3Bh' or '3Dh' is '0', the θ in the input represents positive. If not, the θ represents negative.

Power factor (-1.0 ~ 1.0)

Value	Power factor	θ [degree]
2000h	1.0	0.0
1FFFh	0.999878(8191/8192)	0.8952
~		
1000h	0.5	60.0
~		
0001h	0.00012207	89.993
0000h	0.0	90.0
7FFFh	-0.00012207	90.00699
~		
7000h	-0.5	120.0
~		
6001h	-0.999878	179.1047
6000h	-1.0	180.0

Temperature data (57h, 58h, 59h)

Address A6-0	Data								Initial value
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	
57h (R)	-	-	-	-	-	-	-	-	0080h
	TEMP7-0 (Temperature data)								
58h (R/W)	-	-	-	TEMP_COEF12-8 (Temperature gain coefficient)					1C2Ah
	TEMP_COEF7-0 (Temperature gain coefficient)								
59h (R/W)	-	-	-	-	-	-	-	-	0000h
	-	-	-	TOFFSET4-0 (Temperature offset coefficient)					

Temperature related data are stored in these registers.

It is possible to set TEMP bit (bit2) with '1' of Function setting segister, ADD. '20h' to measure the temperature of the LSI and the measured temperature data is written into Temperature register, ADD. '57h'.

Temperature data can be adjusted with the value of Temperature gain coefficient register, ADD.'58h' and Temperature offset coefficient register,ADD.'59h'. When modifying the values of the Temperature gain coefficient register and Temperature offset coefficient register, it is needed to measure VREFI voltage at room temperature first and modify the value of the Temperature gain coefficient register,ADD.'58h' according to the following formula.

Relationship between VREFI voltage and setting value of the register is expressed as follows.

$$TEMP\_COEF = 1C2Ah \times (VREFI\ voltage / 1.17V)$$

After modifying the value of TEM_COEF, it is needed to measure the temperature by setting TEMP bit (bit2) with '1' of Function setting register,ADD.'20h' to set the temperature offset coefficient.

It is needed to adjust the difference after comparing this value with the value of present room temperature according to the table of Temperature offset coefficient register,ADD.59h' below.

It is needed to measure the temperature again by setting TEMP bit (bit2) with '1' of Function setting register,ADD.'20h' to confirm that an appropriate adjustment is done.

As the initial value of temperature register is an invalid value, which is '80h', please do not use it as the temperature data.

Temperature register (-40 °C to 85 °C) : ADD. 57h

Value	Temperature (Celsius)
7Fh	-
-	
55h	85 °C
-	~
01h	1°C
00h	0°C
FFh	-1°C
-	~
D8h	-40°C
-	
80h	-

Temperature offset coefficient register (ADD. 59h)

Value	Adjustment temperature (degree)
0Fh	+15°C
~	
01h	+1°C
00h	0°C
1Fh	-1°C
~	
10h	-16°C

Measured temperature data is written into the Temperature data register,ADD.'57h' after the temperature adjustment above is done against the value of temperature sensor.

5.3 PGA (Programmable Gain Controller)

Gain can be set from '1' to '4' at voltage input side and '1' to '32' at current input side. Maximum input range is specified according to analogue input full-scale voltage. This makes it possible to use ADC with the maximum resolution.

5.4 ADC block

5.4.1 ADC

ADC is started with $\overline{\text{RST}}$ = $\overline{\text{STBY}}$ = "H"

CH1's, CH2's and CH3's ADC is timesharingly processed every 16XCLKs. 3 channel's ADC is processed by using 4096XCLKs. This means that ADCs for 3 channels are performed at the rate of 3.15kHz when XCLK is 12.9024MHz.

It usually requires about 300mS to stabilize the VREF, XCLK and HPF after ADC is started with $\overline{\text{RST}}$ = $\overline{\text{STBY}}$ = "H". And it is not guaranteed the accuracy of ADC during this 300ms period.

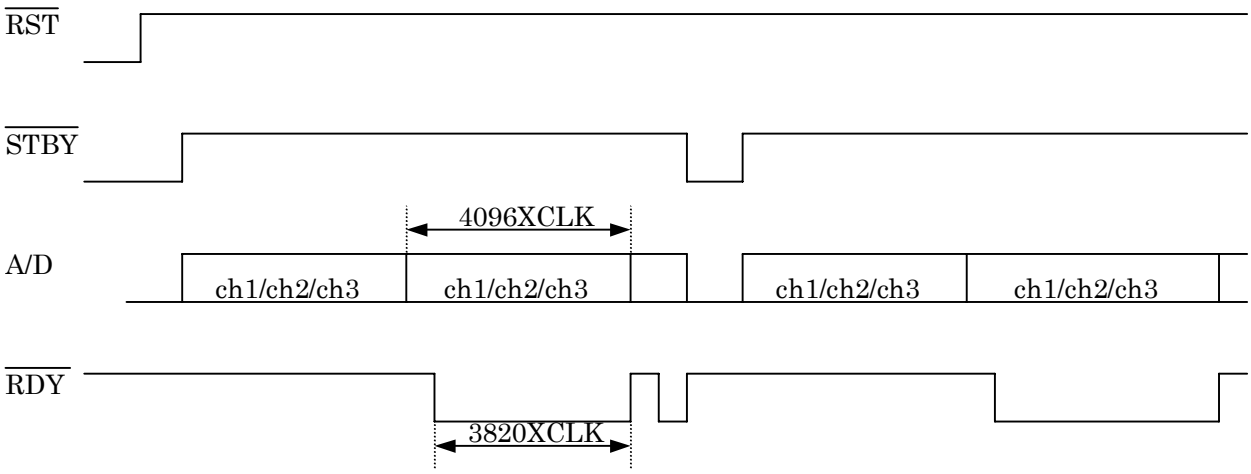


Fig.8 ADC timing

5.4.2 Calibration of ADCs

Calibration, offset adjustment of ADC will be started when CAL bit(bit7) of Function setting register,ADD.'20h' is set '1' under the condition of $\overline{\text{RST}}$ = $\overline{\text{STBY}}$ = "H".

It requires 4096 XCLKs to complete the calibration and ADC will be restarted after the calibration.

$\overline{\text{RDY}}$ signal becomes "High" state as soon as the calibration starts. The RMS calculation and the active power to frequency conversion block are suspended during the calibration. The calibration operation is not executed when only the power is applied to the LSI ($\overline{\text{RST}}$ ="L"). HPF is not set in the default setting. In a case that HPF is not used in the system, it is recommended to execute the calibration command once or write the calibration data, which has been measured before into the offset register in order to get an accurate ADC data. And in the case that HPF is used in the system, it is recommended to set a HPF after the calibration command being executed.

It is needed to execute the calibration operation after the setting of PGA. The setting of PGA should be executed after more than 300ms has passed under the state of $\overline{\text{RST}}$ = $\overline{\text{STBY}}$ = "H" .

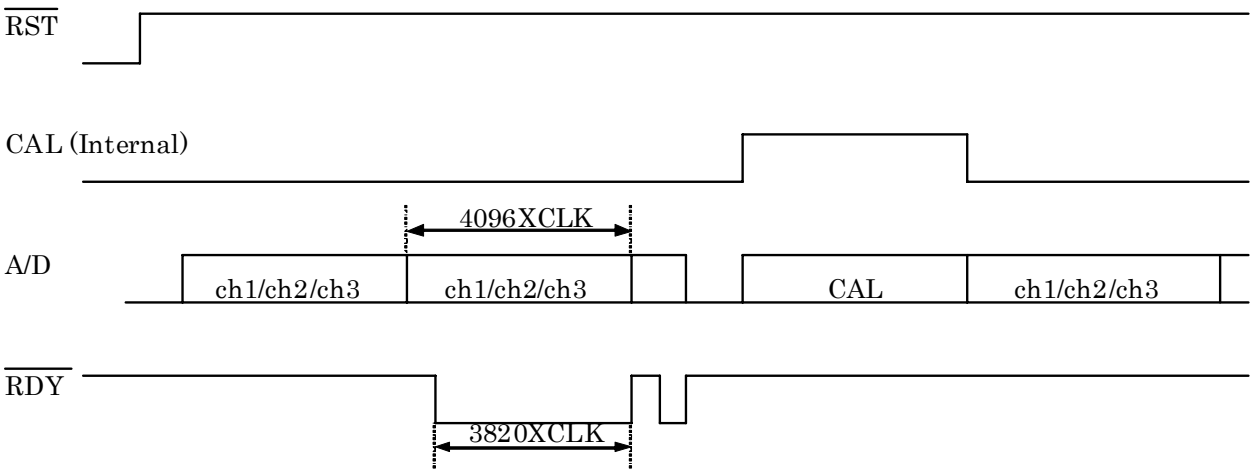


Fig.9 Calibration timing

5.4.3 $\overline{\text{RDY}}$ (ADC's instantaneous value) control

$\overline{\text{RDY}}$ signal for reading instantaneous values of ADC is set and output by setting RDY1-0 (bit1-0)='01' of the Control setting register, ADD. '21h'.

When $\overline{\text{RDY}}$ becomes "L", it means that accurate values of registers storing ADC's value can be read out.

The low level of $\overline{\text{RDY}}$ is output while CH1's ADC is executed after the ADC block has started under the condition of $\overline{\text{RST}}$ = $\overline{\text{STBY}}$ = "H".

$\overline{\text{RDY}}$ signal becomes "L" in 280XCLKs after CH1's ADC has started and returns "H" in 3816XCLKs(about 295.7us).

$\overline{\text{RDY}}$ remains "H" while $\overline{\text{RST}}$ or $\overline{\text{STBY}}$ is "L".

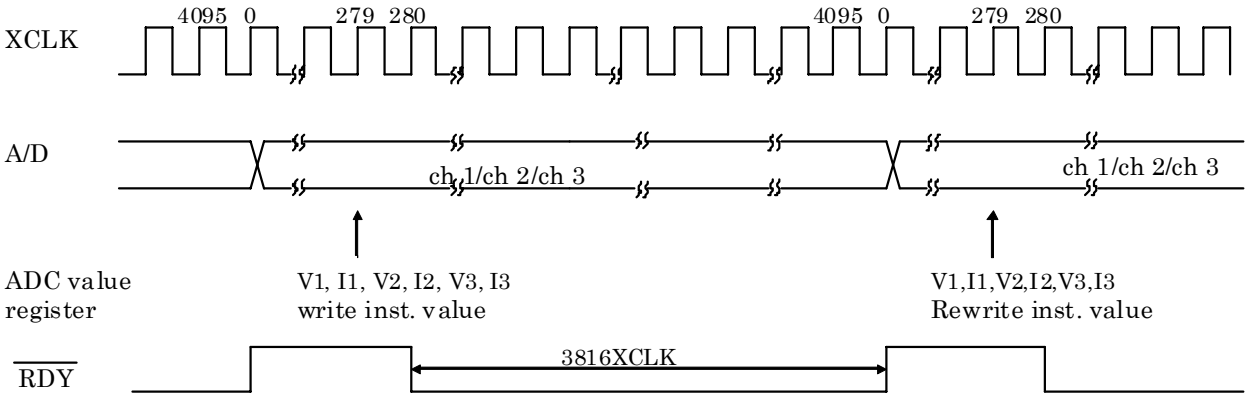


Fig10 ADC inst. value readout timing

When the reading out data timing of instantaneous values of ADCs collide with the timing of writing into instantaneous values by the LSI, INVALID status (bit15) of the controlling register, ADD.'21h' is set. When the collision occurs, it is necessary to read the register again.

5.4.4 $\overline{\text{RDY}}$ (ADC's RMS value) control

$\overline{\text{RDY}}$ signal for reading RMS values of ADC is set and output by setting RDY1-0(bit1-0)='00' of Control setting register, ADD. '21h'.

When $\overline{\text{RDY}}$ becomes "L", it means that accurate values of registers storing ADC's value can be read out.

The low level of $\overline{\text{RDY}}$ is output while CH1's ADC is executed after the ADC block has started under the condition of $\overline{\text{RST}}$ = $\overline{\text{STBY}}$ = "H".

$\overline{\text{RDY}}$ signal becomes "L" in 1872XCLK after CH1's ADC has started and returns "H" in 3384XCLK(about 262.3us) .

$\overline{\text{RDY}}$ remains "H" while $\overline{\text{RST}}$ or $\overline{\text{STBY}}$ is "L".

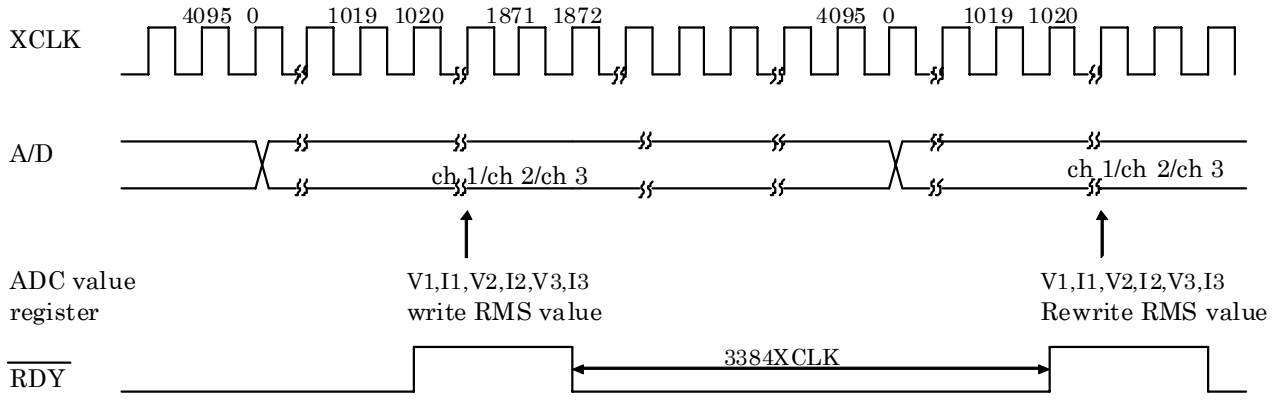


Fig.11 ADC RMS readout timing

When the reading out data timing of RMS values of ADCs collide with the timing of writing RMS values into registers by the LSI , INVALID status (bit15) of Control setting register, ADD. '21h' is set. When the collision occurs, it is necessary to read the register again.

5.4.5 $\overline{\text{RDY}}$ (Other registers: Add.22h - 57h) control

$\overline{\text{RDY}}$ signal for reading registers addressing '22h' to '57h' is set and output by setting RDY1-0 (bit1-0)='10' or '11' of Control setting register, ADD. '21h'.

When $\overline{\text{RDY}}$ becomes "L", it means that accurate values of various registers can be read out.

The low level of $\overline{\text{RDY}}$ is output while CH1's ADC is executed after the ADC block has started under the condition of $\overline{\text{RST}}$ = $\overline{\text{STBY}}$ = "H".

$\overline{\text{RDY}}$ signal becomes "L" in 3164XCLK after CH1's ADC has started and returns "H" in 932XCLK(about 72.2us).

$\overline{\text{RDY}}$ remains "H" while $\overline{\text{RST}}$ or $\overline{\text{STBY}}$ is "L".

When the reading out data timing of a register collide with the timing of writing data into the register by the LSI, INVALID status (bit15) of Control setting register, ADD.'21h' is set. When the collision occurs, it is necessary to read the register again.

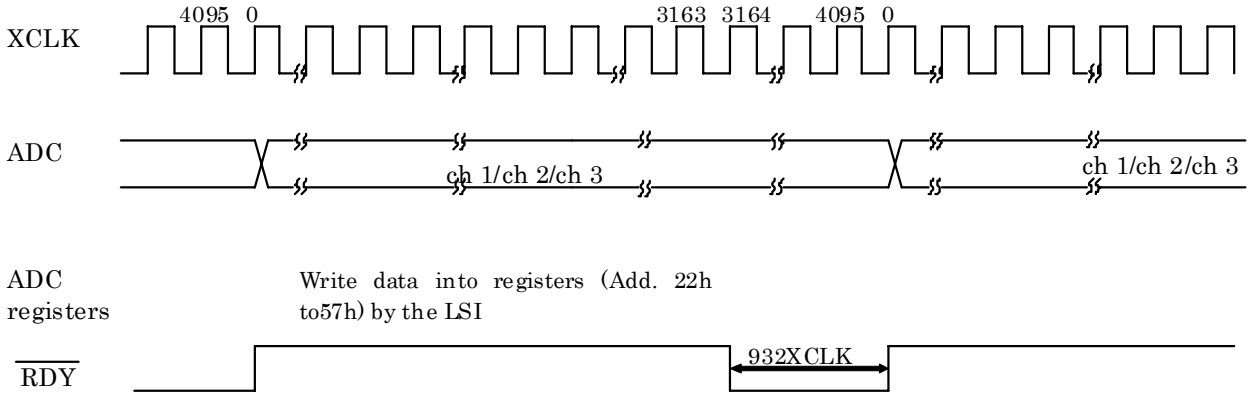


Fig.12 Data registers readout timing

5.5 HPF

It is possible to insert a HPF into voltage sides and current sides in order to remove DC components on input channels. This HPF is placed on a path after each ADC block. This means that DC components super imposed on as one part of an input signal and produced by an ADC block can be removed.

HPFs are inserted into all channels of voltages and currents simultaneously. It is possible to use HPF by setting bit3='1' of Function setting register, ADD.'20h'.

HPFs are not set in the default setting with $\overline{\text{RST}}$ = "L".

In case of using HPFs, it is recommended to set HPFs after executing the calibration command.

Gain and phase characteristics of the HPFs are shown from Fig.13 to Fig15.

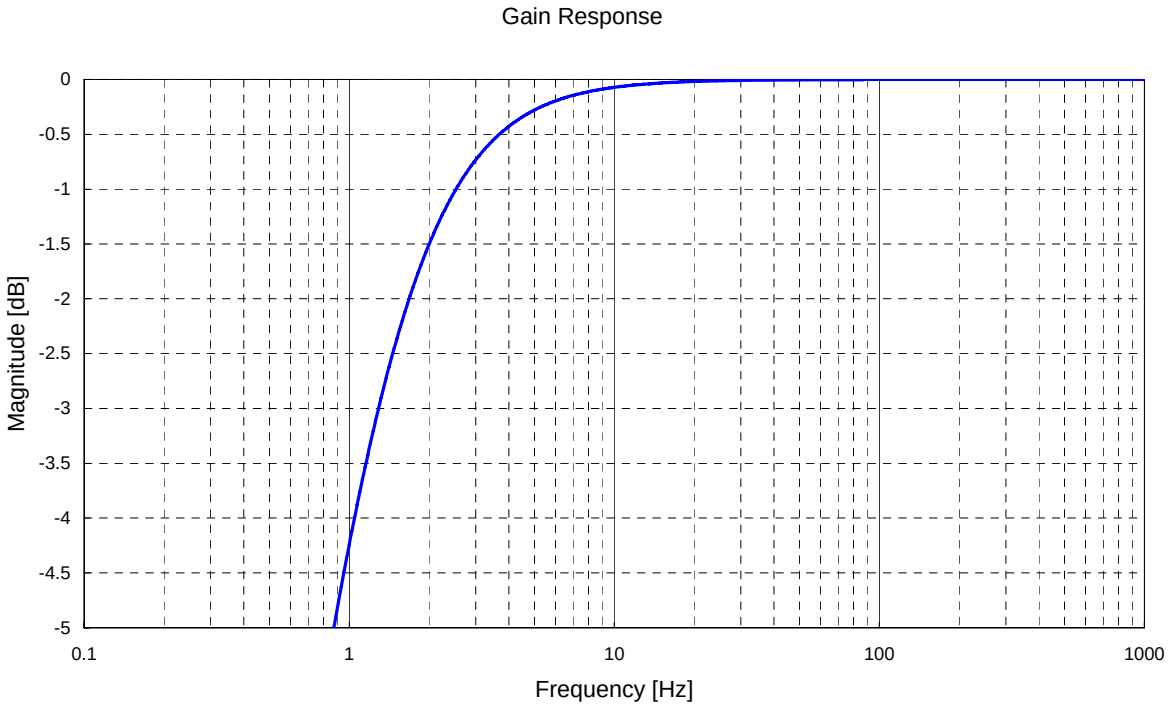


Fig.13 Gain – Frequency characteristics

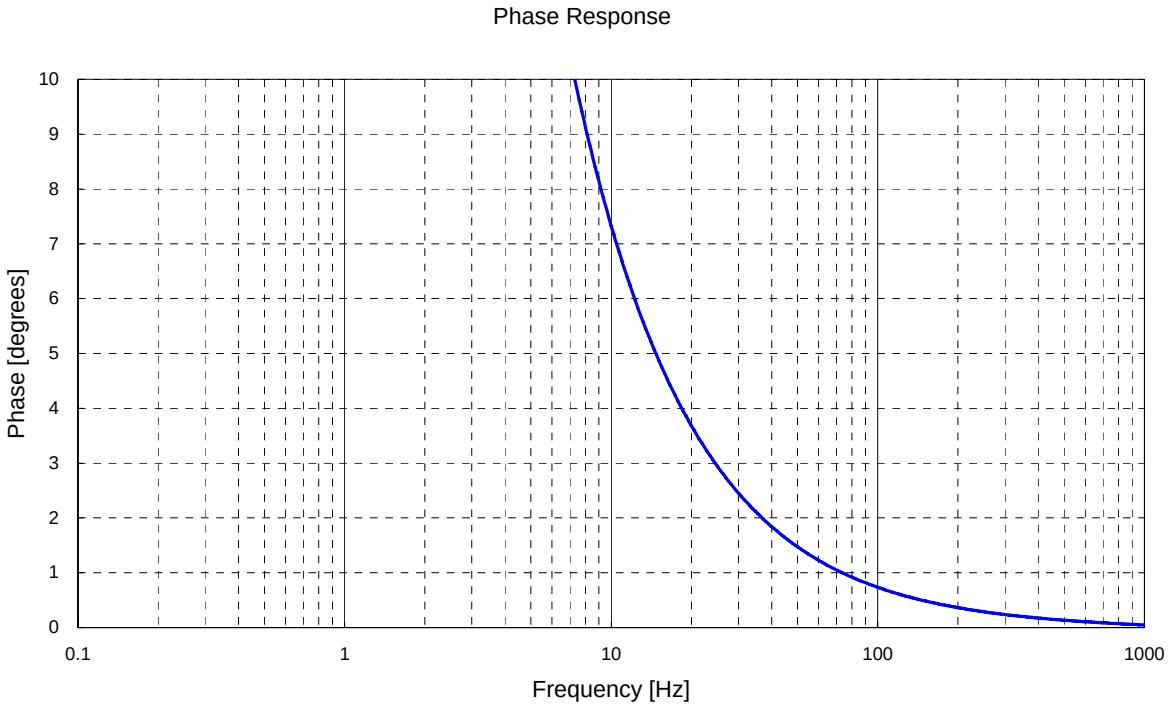


Fig.14 Phase –Frequency characteristics

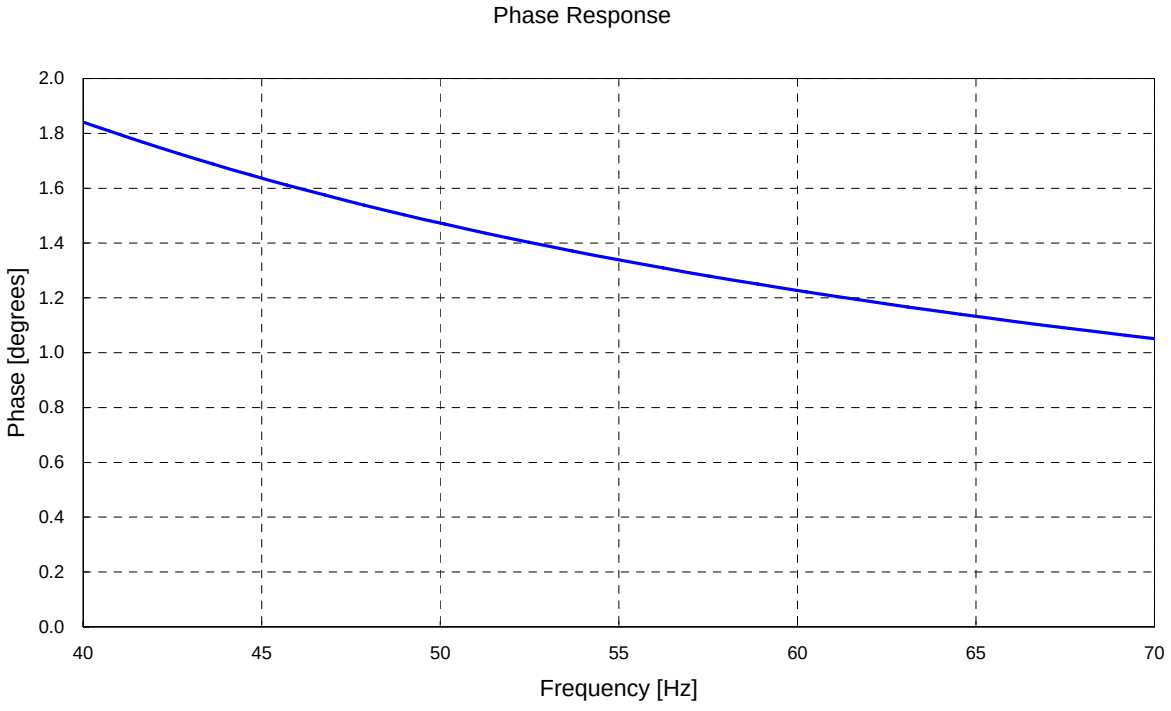


Fig.15 Phase – Frequency Characteristics (40Hz to 70Hz)

5.6 RMS calculation

RMS calculation block calculates RMS value of V1, I1, V2, I2, V3 and I3 from ADC value. These values can be read from RMS registers.

RMS calculation flow is shown in fig.16

(1) To calculate square value of V1 (I1, V2, I2, V3, I3)

(2) Averaging

(3) To calculate the square root

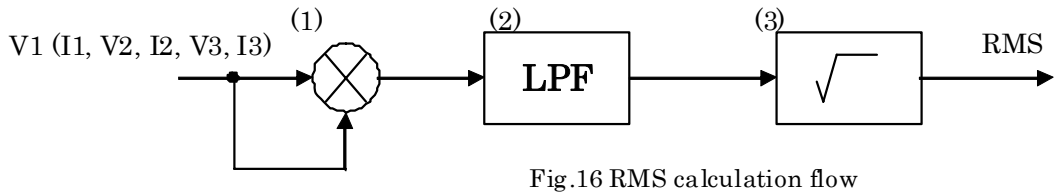


Fig.16 RMS calculation flow

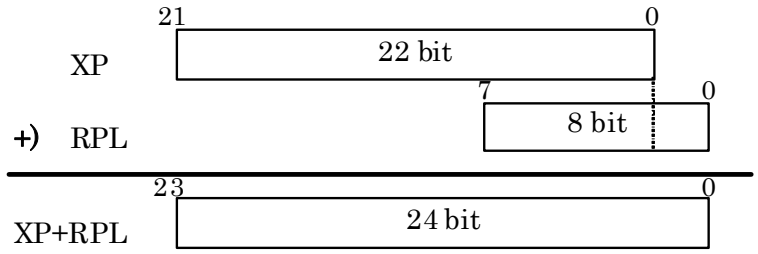
5.7 Active power and reactive power to frequency converter

XP+RPL or -XP+TPL data, which consists of significant 24bit, is supplied to active or reactive frequency converter at the rate of 3.15kHz. (note 1)

Active or reactive power to frequency converter is making an arithmetic operation at the rate of 16/3 (16.8kHz) and produces RPO (RQO), TPO (TQO), RPST (RQST) and TPST (TQST) output.

Active or reactive power to frequency converter stops its operation with $\overline{\text{RST}}$ = "L" or $\overline{\text{STBY}}$ = "L" or $\overline{\text{DIS}}$ = "L".

(note 1) The structure of XP+RPL



It is possible to select an apparent power as an input of reactive power to frequency converter by setting '1' of bit14 at Power addition "disable" setting register, ADD.'1Dh'.

Furthermore, as an apparent power does not have the light load register, 22 bit apparent power value is shift in two bits left. As the result, 24 bit format data is input at ALU and is converted into the power pulse.

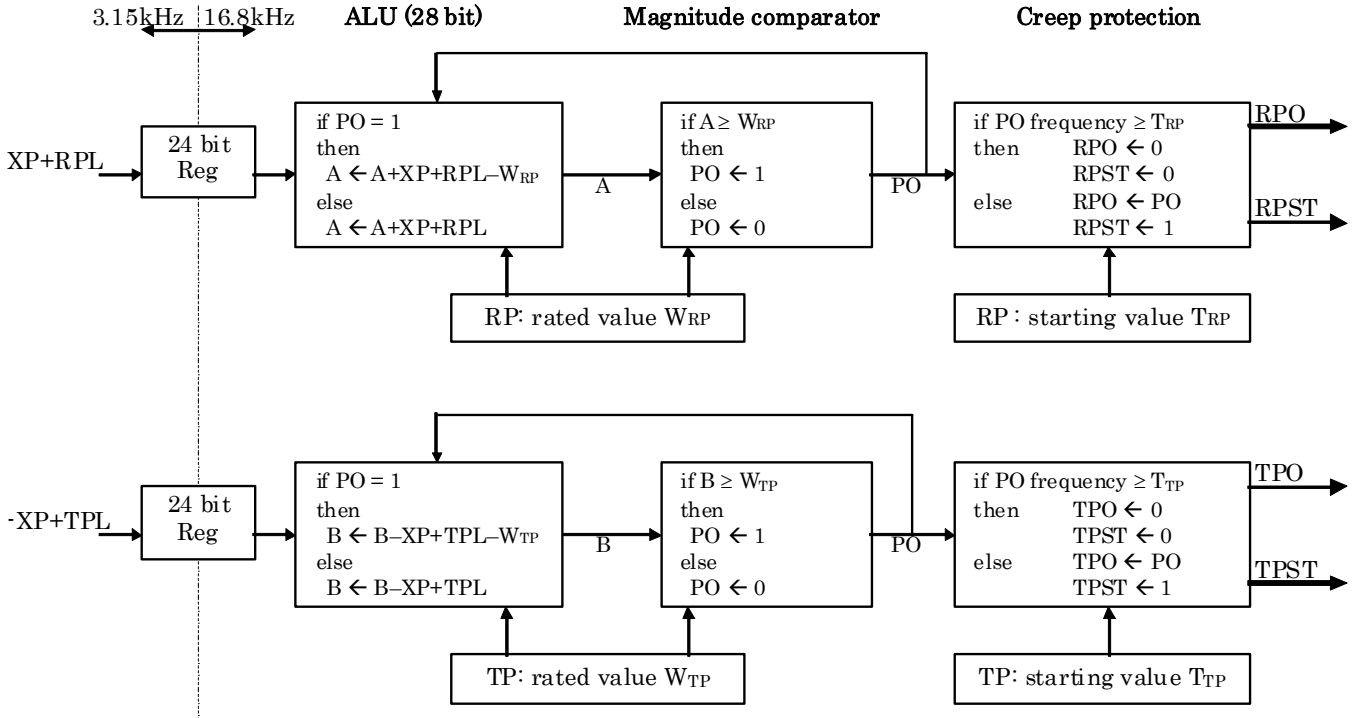


Fig.17 Active power to frequency conversion

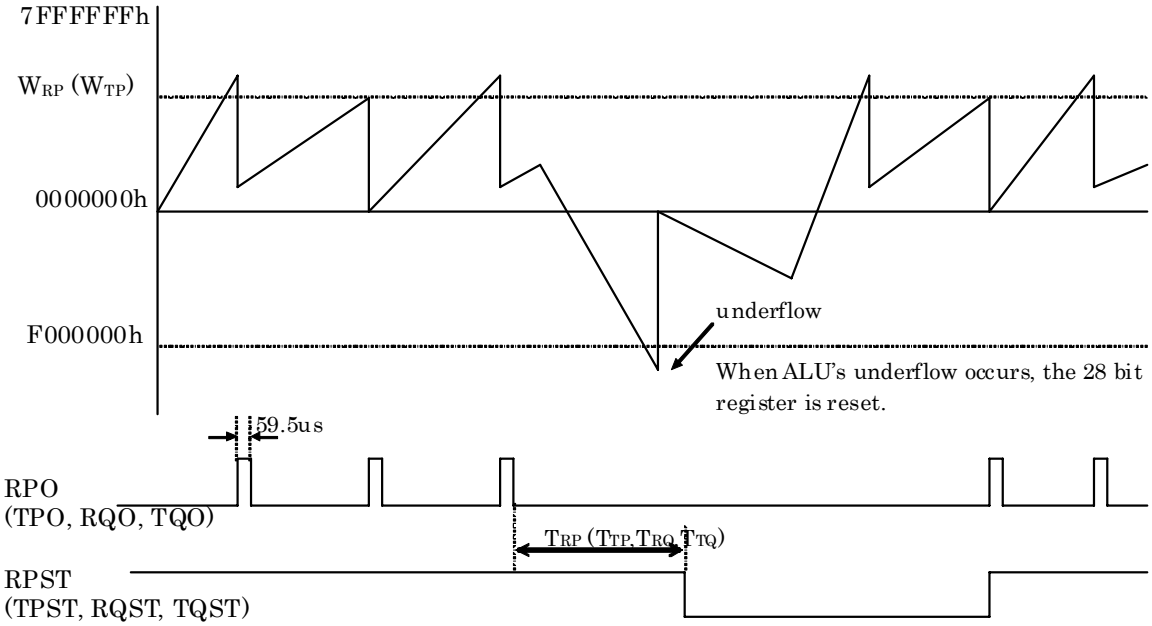


Fig.18 RPO (TPO, RQO, TQO) OUTPUT timing

5.8 Frequency pulse output of V1, V2 and V3

The frequencies of voltage inputs are detected, being based on ADC value of V1, V2 and V3. For example, when the rising threshold value of F1, F2,and F3 is set at '3000h' and the falling threshold value is set at '2000h', the waveform will be shown below.
When V1, V2, V3 equals or greater than '3000h', Fn (n=1, 2, 3) becomes "H".
When V1, V2, V3 equals or smaller than '2000h', Fn (n=1, 2, 3) becomes "L".

This function is stopped at $\overline{\text{RST}}$ = "L" or $\overline{\text{STBY}}$ = "L".

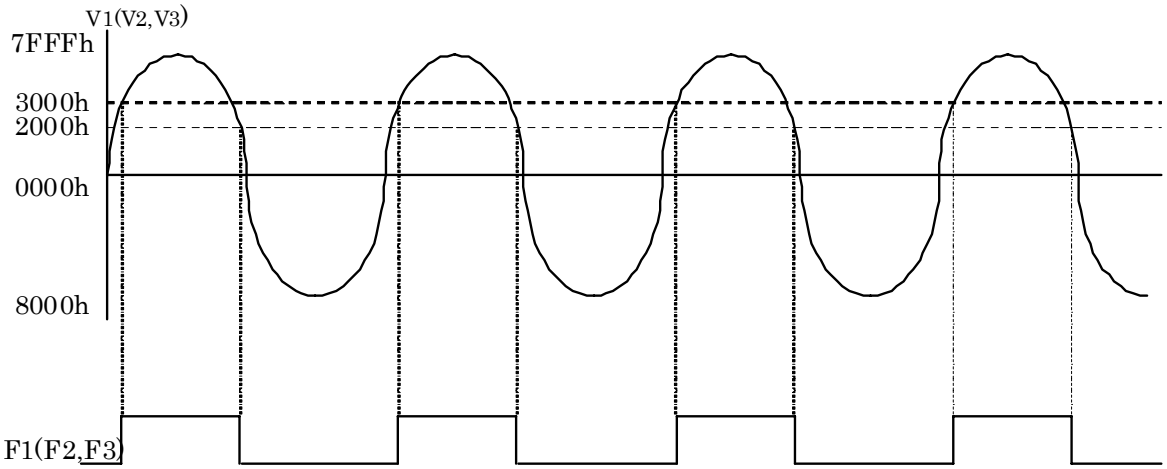


Fig.19 V1(V2,V3) frequency pulse output

5.9 The way of various system calibrations

5.9.1 Calibration procedures of active power and reactive power (Japanese specification)

Japanese standard of power metering specifies that 1000 of power pulses per one second should be output when rated input voltages and currents are applied to the system.

AK5602A provides an easy calibration method to comply with the specification.

By adjusting rated active or reactive power threshold value in receiving and transmitting side, the accuracy of the equipment would be attained. General way of the calibration is described below.

(1) Power on the system.

(2) To control $\overline{\text{RST}}$ = "H"

(3) To control $\overline{\text{STBY}}$ = "H"

(4) To control $\overline{\text{DIS}}$ = "H"

(5) To write '0080h' at Function setting register, ADD. '20h' to calibrate ADCs

(6) To write '0008h' at Function setting register, ADD. '20h' to insert HPF on each voltage and current input

(7) When calibrating receiving active power, apply 50Hz or 60Hz of 0.35Vrms(0.5Vop) AC signal to each current and voltage input. The phase difference between voltage and current of the signal on each channel should be '0' degree. This means that the power factor of each channel should be '1.0'. The amplitude of the signal should be 0.35Vrms when the PGA is set ×1. If the value of PGA is set other value rather than ×1 , the amplitude of the signal should be changed accordingly. For instance, if the PGA set ×2, the amplitude of the signal should be the half of 0.35Vrms. Under the condition, the number of output pulses at RPO pin is counted over checking RPST flag and should be adjusted until the number equals to 1000 for one second by modifying the value of RP rated active power threshold value register, ADD.'00h' and '01h'.

(8) When calibrating tranmitting active power, apply 50Hz or 60Hz of 0.35Vrms(0.5Vop) AC signal to each current and voltage input. The phase difference between voltage and current of the signal on each channel should be set at '180' degree. This means that the power factor of each channel should be '-1.0'. Under the condition, the number of output pulses at TPO pin is counted over checking TPST flag and should be adjusted until the number equals to 1000 for one second by modifying the value of TP rated active power threshold value register, ADD. '02h' and '03h'.

(9) When calibrating receiving reactive power, apply 50Hz or 60Hz of 0.35Vrms(0.5Vop) AC signal to each current and voltage input. The phase difference between voltage and current of the signal on each channel should be '90' degree. This means that the power factor of each channel should be 0. The amplitude of the signal should be 0.35Vrms when the PGA is set ×1. If the value of PGA is set other value rather than ×1 , the amplitude of the signal should be changed accordingly. For instance, if the PGA set ×2, the amplitude of the signal should be the half of 0.35Vrms. Under the condition, the number of output pulses at QPO pin is counted over checking RQST flag and should be adjusted until the number equals to 1000 for one second by modifying the value of RQ rated reactive power threshold value register, ADD.'04h' and '05h'.

(10) When calibrating tranmitting reactive power, apply 50Hz or 60Hz of 0.35Vrms(0.5Vop) AC signal to each current and voltage input. The phase difference between voltage and current of the signal on each channel should be '270' degree. This means that the power factor of each channel should be '0'. Under the condition, the number of output pulses at

TQO pin is counted over checking TQST flag and should be adjusted until the number equals to 1000 for every one second by modifying the value of TQ rated active power threshold value register,ADD. '06h' and '07h'.

(11) It is possible to use pulse count values,ADD. '48h' and '49h' as the mothod of measuring the number of output pulses instead of counting the number of output pulses from pulse output pins(RPO, TPO, RQO, TQO). In this case, the inside timer of the AK5602A is used for one second timer and the value of the timer will be changed according to the frequency of using crystal. AK5602A defines that one second timer is attained when 12.9024MHz crystal is used.

5.9.2 Initial value of Rated power threshold value (Japanese specification)

The initial value of Rated power threshold value is set so that 1000 power pulses for one second would be output when the half of full scale AC signal is applied to each current input and each voltage input. The initial value is calculated as follows.

Power value per channel is expressed as follows.

$$XP^1=1/2\times Vin\times Iin$$

,where Vin = maximum voltage input (±1.0Vpp)

Iin = maximum current input (±1.0Vpp)

Initial value of Rated power threshold value is defined when half of maximum input voltage and maximum input current is applied. Input voltage and current per channel is

$$Vin = 1/2 \times (2\text{^}15) = 16384$$

$$Iin = 1/2 \times (2\text{^}17) = 65536$$

And the bit width of Vin × Iin is 34 bit width, which is 16bit + 18bit, but it is needed to be shrinked to 20bit wide by taking upper 20 bit and the result should be devided by 2^13.

So, power value per channel is $XP^1 = (1/2) \times 16384 \times 65536 \times (1/(2\text{^}13)) = 65536$

In a case that the same signal is applied to all 3ch, total power would be

$$XP = 65536 \times 3 = 196608$$

The light load value is added to the XP, so the relsult is shifted left by 2 bit.

In a case of calculating receiving active power, using light load power value is RPL.

$$XP = XP + RPL = XP \times 4 = 786432$$

This value is accumulated at the rate of 16.8 kHz and the pulse is output 1000 pulses per one second. So, the enegy, W is described below.

$$W = (XP + RPL) \times 16.8 = 13212057 = C99999h$$

This value is an initial value of receiving Rated active power threshold value.

This initial value is also applied to the initial value of transmitting Rated active power threshold value, receiving Rated reactive power threshold value and transmitting Rated reactive power threshold value.

5.9.3 Calibration procedures of active power and reactive power (IEC specification)

In IEC specification, the specification of creeping, starting current, pulse outputs is different from that of Japanese standard. To comply with the IEC standard, it is needed to change initial values of some registers. The following example shows that 1000 of power pulses per one second are output and general relationship between power pulses and rated power threshold value. Please calibrate the energy of the system by adjusting rated power threshold values.

(1) Power on the system.

(2) To control $\overline{RST}$ = "H"

To set registers to comply with the IEC standard.

1. To set the starting power threshold value register 'o' second : 'FFFFh' at Starting power threshold value register,ADD. '08h'
2. To set the accumulation frequency of IEC power pulse width setting register '4.2kHz' : '8000h' at IEC power pulse width setting register,ADD. '1Fh'
3. To set the Function setting register 'IEC creeping threshold value' : '0010h' at Function setting register,ADD. '20h'

(3) To set rated active or reactive power threshold values in receiving and transmitting side so that 1000 pulses per second would be output. In this case, it is assumed that using crystal frequency is 12.9024MHz. When setting the IEC standard mode, the relationship between the number of pulses and rated power threshold value is expressed as follows.

F (the number of pulses) = 3225600 / W (rated power threshold value)

W = 3225600 / 1000 = 3225.6 = 0C99h

'0C99h' is set at ADD.'00h', '02h', '04h', '06h' and '0000h' is set at ADD. '01h', '03h', '05h', '07h'.

(4) To control $\overline{\text{STBY}}$ = "H"

(5) To control $\overline{\text{DIS}}$ = "H"

(6) To write '0080h' at Function setting register,ADD.'20h' to calibrate ADCs

(7) To write '0008h' at Function setting register,ADD.'20h' to insert HPF on each voltage and current input

(8) When calibrating receiving active power, apply 50Hz or 60Hz of 0.35Vrms (0.5Vop) AC signal to each current and voltage input. The phase difference between voltage and current of the signal on each channel should be '0' degree. This means that the power factor of each channel should be '1.0'. The amplitude of the signal should be 0.35Vrms when the PGA is set ×1. If the value of PGA is set other value rather than ×1, the amplitude of the signal should be changed accordingly. For instance, if the PGA is set ×2, the amplitude of the signal should be the half of 0.35Vrms. Under the condition, the number of output pulses at RPO pin is counted and should be adjusted until the number equals to 1000 for every one second by modifying the value of RP rated active power threshold value register at ADD.'00h' and '01h'.

(9) When calibrating tranmitting active power, apply 50Hz or 60Hz of 0.35Vrms (0.5Vop) AC signal to each current and voltage input. The phase difference between voltage and current of the signal on each channel should be '180' degree. This means that the power factor of each channel should be '-1.0'. Under the condition, the number of output pulses at TPO pin is counted and should be adjusted until the number equals to 1000 for every one second by modifying the value of TP rated active power threshold value register at ADD. '02h' and '03h'.

(10) When calibrating receiving reactive power, apply 50Hz or 60Hz of 0.35Vrms (0.5Vop) AC signal to each current and voltage input. The phase difference between voltage and current of the signal on each channel should be '90' degree. This means that the power factor of each channel should be 0. The amplitude of the signal should be 0.35Vrms when the PGA is set ×1. If the value of PGA is set other value rather than ×1 , the amplitude of the signal should be changed accordingly. For instance, if the PGA set ×2, the amplitude of the signal should be the half of 0.35Vrms. Under the condition, the number of output pulses at QPO pin is counted and should be adjusted until the number is equal to 1000 for one second by modifying the value of RQ rated reactive power threshold value register at ADD.'04h' and '05h'.

(11) When calibrating tranmitting active power, apply 50Hz or 60Hz of 0.35Vrms(0.5Vop) AC signal to each current and voltage input. The phase difference between voltage and current of the signal on each channel should be '270' degree. This means that the power factor of each channel should be '0'. Under the condition, the number of output pulses at TQO pin is counted and should be adjusted until the number is equal to 1000 for one second by modifying the value of TQ rated active power threshold value register at ADD. '06h' and '07h'.

(12) It is possible to use pulse count values at ADD.'48h' and '49h' as the mothod of measuring the number of output pulses instead of counting the number of output pulses from pulse output pins (RPO, TPO, RQO, TQO). In this case, the inside timer in the AK5602A is used for one second timer and the value of the timer will be changed according to the frequency of using crystal. AK5602A defines that one second timer is attained when 12.9024MHz crystal is used.

(13) In IEC setting mode, the pulse frequency per second, F is expressed as follows.

F (the number of pulses) = 3225600 / W (rated power threshold value)

Pulse frequency,F is varied according to the value of rated power threshold in the following.

$$0.048065186263\text{Hz} \leq F \leq 8400\text{Hz} \quad \text{----------(a)}$$

5.9.4 Initial value of Rated power threshold value (IEC specification)

The initial value of Rated power threshold value is set in Japanese specification so that 1000 power pulses for one second would be output when a half of full-scale of 50 to 60 Hz of AC signal is applied to each current input and each voltage input. When AK5602A is used in IEC mode, related registers and Rated power threshold value should be modified. The initial value in IEC standard is calculated as follows.

Power value per channel is

$$XP^1 = 1/2 \times Vin \times Iin$$

,where Vin = maximum voltage input (±1.0Vpp)

Iin = maximum current input (±1.0Vpp)

Initial value of Rated power threshold value is defined when half of maximum input voltage and maximum input current is applied. Input voltage and current per channel is

$$Vin = 1/2 \times (2\text{^}15) = 16384$$

$$Iin = 1/2 \times (2\text{^}17) = 65536$$

And the bit width of Vin × Iin is 34 bit wide, which is 16bit + 18bit but it is needed to be shrinked to 20bit wide by taking upper 20 bit and the result should be devided by 2^13.

So, power value per channel is $XP^1 = (1/2) \times 16384 \times 65536 \times (1/(2\text{^}13)) = 65536$

In a case that the same signal is applied to all 3ch, total power is expressed as follows.

$$XP = 65536 \times 3 = 196608$$

The light load value is added to the XP, so the relsult is shifted left by 2 bit.

In a case of calculating receiving active power, using light load power value is RPL.

$$XP = XP + RPL = XP \times 4 = 786432$$

And in IEC mode, pulse frequency,F is

$$F = 4200 \times P / (W \times 1024)$$

,where P = Total power, W = rated power threshold value

When half of maximum input voltage and maximum input current is applied to each channel ,

$$F = 4200 \times 786432 / W \times 1024 = 3225600 / W \quad \text{----------(b)}$$

In other expression, W = 3225600 / F

Maximum value of W(rated power threshold) is 3FFFFFh (67108863) and pulse frequency at the value, F_{MIN} is expressed as follows.

F_{MIN} = 3225600 / 67108863 = 0.048065186Hz

When the pulse frequency,F is 1000, W = 3225600 / 1000 = 3225.6 = C99h

In IEC mode, the value of pulse frequency should be set from around 0.1Hz to 2 or 3Hz.

The value of rated power threshold can be set according to the equation (a) and (b).

Explained setting rated power thereshold method is applied to transmitting active power threshold value, receiving reactive power threshold value and transmitting reactive power threshold value as well.

5.9.5 Calibration measure between input voltage and input current on each channel

(1) Please apply the rated input voltage and rated input current on each channel of the system. In order to calibrate the phase error at only the 1st channel, the incoming signal at 2nd channel and 3rd channel should be shortened by using shorting bits 'ZV2', 'ZV3', 'ZI2', 'ZI3' at Function setting register '20h' lest should powers other than 1st channel be accumulated.

(2) The number of receiving power pulses when voltage input and current input at power factor being '1' is defined as 'A'. The number of receiving power pulses when voltage input and current input at power factor being '0.5' is defined as 'B'. The phase error,α is expresed as follows.

$$\alpha = (B - A /2) / (A/2)$$

Therefore the phase difference, β(degree) is

$$\beta = -SIN^{-1}(\alpha / \sqrt{3})$$

To set value at Power factor adjustment value setting register(ADD. 0Dh, 0Eh, 0Fh) so that α is equal to zero. When input signal frequency is 50Hz and using crystal frequency is 12.9024 MHz in AK5602A, the phase adjustment range, γ is expressed as followed.

$$-613.84us\ (-11.05°) \le \gamma \le +613.84us\ (+11.05°)$$

It is possible to adjust the phase error with the resolution of 1.25us (0.0225°) per step.

(3) The phase error of 2nd channel and 3rd channel is also adjusted in the same manner as the 1st channel. Adjustment range and resolution are affected by using crystal frequency. For example, the resolution of calibration range at 12.8MHz crystal is 1.25us (0.0225°).

5.9.6 Full scale vaue adjustment

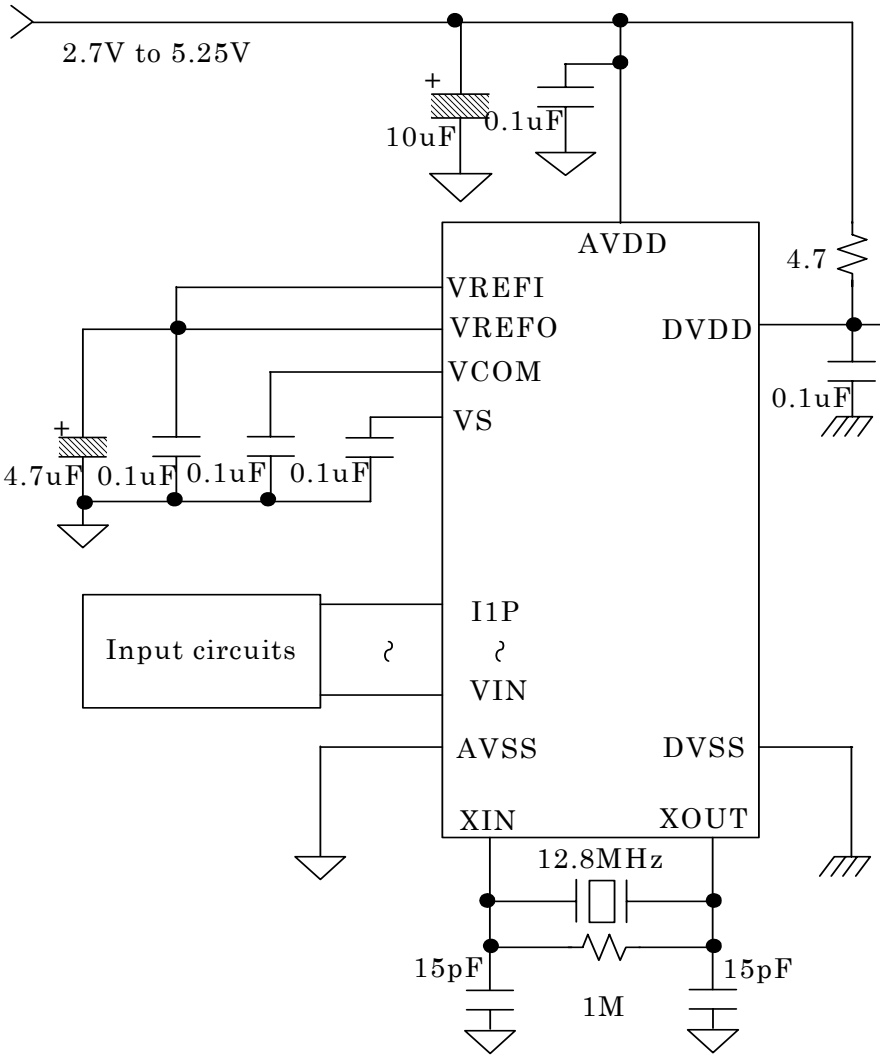
This function is to adjust the variations produced by PGA and / or VREF from ideal value so that the result of ADC has an ideal ADC code when a half of full-scale DC voltage, 0.5 V is applied to each voltage and current channel. When using this function, the gain of all voltage channels should be the same value as well as the gain of all current channels. The gain between current and voltage can be changed. It is noted that after the adjustment, every calculation including an instantaneous value, RMS value and active & reactive power is affected. This is the only way to adjust RMS voltage value and RMS current value.

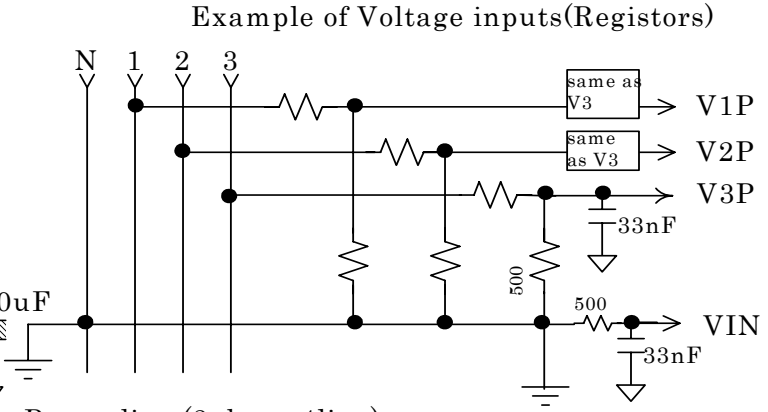
The adjustment of gain on voltage side is performed by setting '1' to 'bit0', FULLV of Function setting register at address '20h'.

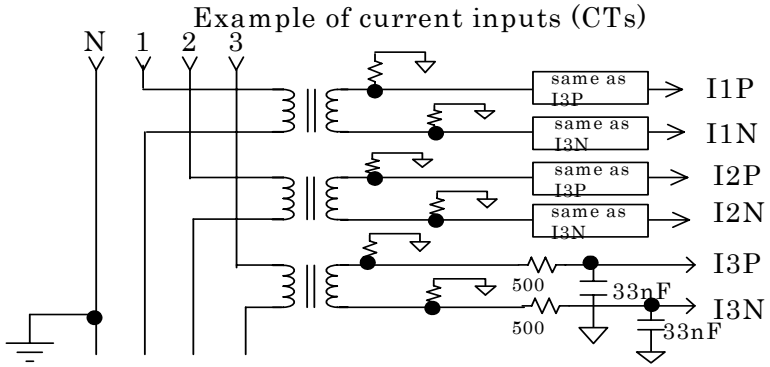
And the adjustment of gain on current side is performed by setting '1' to 'bit1', FULLI of Function setting register at address '20h'.

After the execution of this command, the adjustment values can be read from ADD.'16h', '17h', '18h'. It is also possible to set the values as well by writing the values directly into these registers.

6. Recommended circuit diagram around AK5602A







(1) Input circuits to power lines above are only examples. It is recommended that capacitors and resistors should be selected so that the frequency of anti-aliasing filters is higher to prevent from producing the phase error.

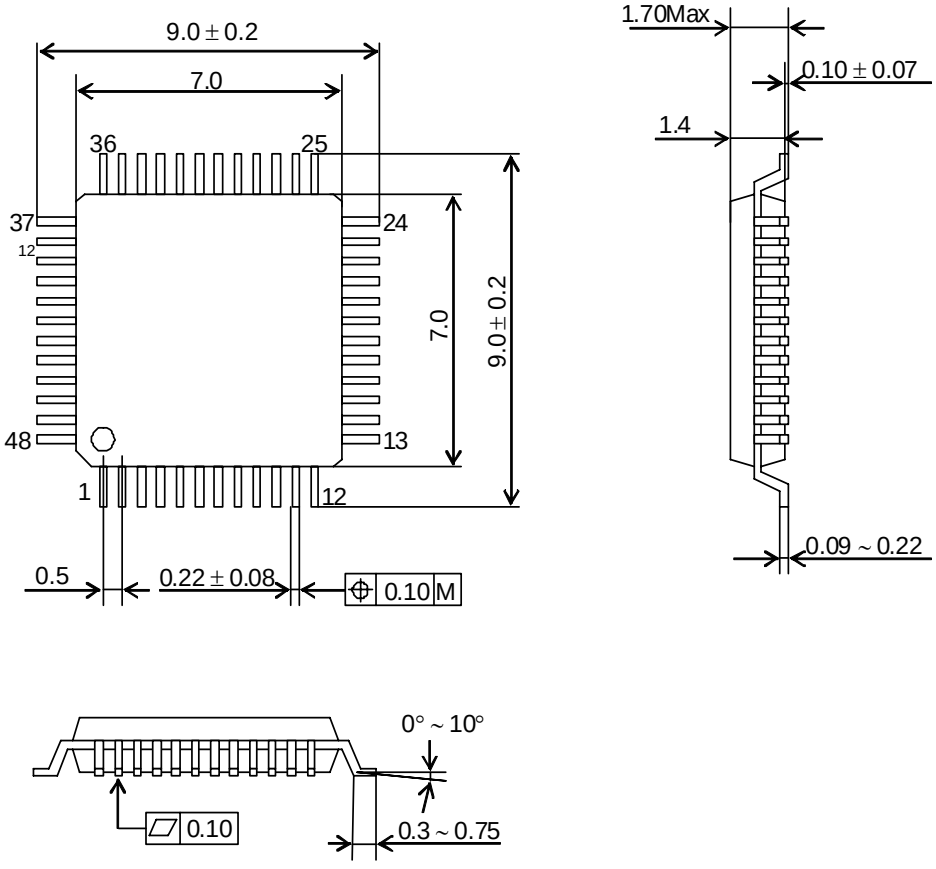
(2) It can not be guranteed that the value of resistors and capacitors around the crystal oscillator is the best constants. It is recommended to confirm the technical data of manufactures of crystal oscillators.

7.0 Package conditions

1) Shape: LQFP
2) Pin count: 48PIN
3) Marking: Marking of the package is specified as follows.
   a. No1 pin indication: There is a round mark and cutting edge.
   b. AKM's logo and product name
   c. Date code XXXXXXX (7 digits)

7.1 Package outline

48pin LQFP (Unit: mm)



Revision History

Date	Revision	Reason	Page	Contents
01/02/03	00	First edition		

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  Note1) A critical component is one whose failure to function or perform may reasonably be expected to result, whether directly or indirectly, in the loss of the safety or effectiveness of the device or system containing it, and which must therefore meet very high standards of performance and reliability.

  Note2) A hazard related device or system is one designed or intended for life support or maintenance of safety or for applications in medicine, aerospace, nuclear energy, or other fields, in which its failure to function or perform may reasonably be expected to result in loss of life or in significant injury or damage to person or property.
- It is the responsibility of the buyer or distributor of AKM products, who distributes, disposes of, or otherwise places the product with a third party, to notify such third party in advance of the above content and conditions, and the buyer or distributor agrees to assume any and all responsibility and liability for and hold AKM harmless from any and all claims arising from the use of said product in the absence of such notification.