Ordering number : ENA0015

SANYO Semiconductors
DATA SHEET

Monolithic Linear IC

LA72700V — US MTS (Multi Channel Television Sound) Decoder

Overview

LA72700V is a US MTS (Multi Channel Television Sound) decoder.

Features

- With SIF circuit, STEREO channel separation is alignment-free.
- Built-in filters are adjustment free.
- SAP output level is selectable 2 levels.
- Included control function for STEREO and SAP detection sensitivity.

Functions

- SIF FM-Demodulator.
- STEREO decoder.
- ALC function is included.
- dbx Noise Reduction system.
- SAP demodulator.
- STEREO detection.
- SAP detection.

Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum power supply voltage	V_{CC} max		9.6	V
Allowable power dissipation	Pd max	Ta≤70°C *	810	mW
Operating temperature	Topr		-10 to +70	°C
Storage temperature	Tstg		-55 to +150	°C

* ON board (114.3 × 76.1 × 1.6 mm Glass Epoxy resin board)

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Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Recommended operating voltage	V_{CC}		9.0	V
Operating voltage range	V_{CC} op		8.5 to 9.5	V

Electrical Characteristics at Ta = 25°C, V_{CC} = 9.0V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Current dissipation	I_{CC}	No signal Inflow current at pin 31 * Default condition	50	60	70	mA
SIF input level (Reference)	VILIM	fc = 4.5MHz Deviation MONO (300Hz, Mod = 100%, Pre-emphasis ON) → ±25kHz	(80)	(90)	(100)	dBμV
Base band input level (Reference)	VILIMB	100% Modulation MONO(L+R): 530mVp-p (300Hz, Pre-emphasis ON) SUB(L-R): 380mVp-p (300Hz, dbx-NR ON), Pilot: 110mVp-p SAP: 300mVp-p (300Hz, dbx-NR ON)				
MONO output level	VOMON	Input: fm = 1kHz, 100% Mod, MONORAL Measure OUT (L), OUT (R)	-7.0	-6.0	-5.0	dBV
MONO distortion	THDMON	Input: fm = 1kHz, 100% Mod, MONORAL Measure OUT (L), OUT (R)		0.15	0.6	%
MONO frequency characteristics	FCM1	Input: fm = 8kHz, 30% Mod, MONORAL Measure OUT(L), OUT(R), Ratio from fm = 1kHz level.	-2	0	2	dB
MONO S/N ratio	SNM	S = VOMON, N = 0% Mod Measure OUT (L), OUT (R) With 15kHz LPF, JIS-A	55	65		dB
STEREO output level	VOST	Input: fm = 1kHz, 100% Mod, STEREO Measure OUT (L), OUT(R)	-7.0	-6.0	-5.0	dBV
STEREO distortion	THDS	Input: fm = 1kHz, 100% Mod, STEREO Measure OUT (L), OUT (R)		1.0	2.5	%
STEREO frequency characteristics	FCS1	fm = 8kHz, 30% Mod, STEREO Measure OUT (L), OUT (R), Ratio from fm = 1kHz level.	-3	0	3	dB
STEREO S/N ratio	SNS	S = VOST, N = 0% Mod Measure OUT (L), OUT (R) With 15kHz LPF, JIS-A	50	60		dB
STEREO separation 1	STSE1	f = 300Hz (R/L), 30% Mod Measure ratio OUT (L) with OUT (R)	20	25		dB
STEREO separation 2	STSE2	f = 3kHz (R/L), 30% Mod Measure ratio OUT (L) with OUT (R)	20	25		dB
STEREO Detection level-1	VINSD1	Except Stereo Detection → Stereo Detection Measure PILOT level, at STERO det.	52	57	62	%
STEREO Detection level-2	VINSD2	Except Stereo Detection → Stereo Detection * Insert Resistor pin 14 to GND (ex. 51kΩ) Measure PILOT level, at STERO det.	62	67	72	%

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Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
STEREO detection hysteresis	HYST	Input Mod. Difference at Stereo /Except Stereo Det. * at default condition	10	15	25	%
SAP output level-1	VOSA	Fm = 1kHz, 100% Mod, SAP Measure OUT (L), OUT * at bit6 = 0	-7.5	-6.5	-5.5	dBV
SAP output level-2	VOSA2	Fm = 1kHz, 100% Mod, SAP Measure OUT (L), OUT * at bit6 = 1	-5.5	-4.5	-3.5	dBV
SAP distortion	THDSA	Fm = 1kHz, 100% Mod, SAP Measure OUT (L), OUT		1.5	3.5	%
SAP S/N ratio	SNSA	S = VOSA, N = 0% Mod, Measure OUT (L), OUT (R) With 15kHz LPF, JIS-A	55	65		dB
SAP detection level-1	VINSA1	Measure SAP carrier level, when SAP det * Default condition	13	18	23	%
SAP detection level-2 (Reference)	VINSA2	Measure SAP carrier level, when SAP det * pin15 to GND (ex 33kΩ)	(5)	(10)	(15)	%
SAP detection level-3 (Reference)	VINSA3	Measure SAP carrier level, when SAP det * pin15 to GND (ex 8.2kΩ)	(20)	(25)	(30)	%
SAP detection hysteresis	HYSA	Input Mod. Difference at SAP/Except SAP Det. * at default condition	2	5	10	%
MODE output MONO	MODMO	Input = MONO: f = 1kHz, 0% Mod Measure pin32	0.7	1	1.3	V
MODE output SAP	MODSA	Input = SAP: Carrier Measure pin32	1.7	2	2.3	V
MODE output STEREO	MODST	Input = STEREO: Pilot Measure pin32	2.7	3	3.3	V
MODE output ST + SAP	MODSS	Input = STEREO: Pilot, SAP: Carrier Measure pin32	3.5	3.8	4.2	V
Distortion	THDALC	MONO 1kHz Mod 100% * ALC on Measure OUT (L), OUT (R)		0.3	0.5	%

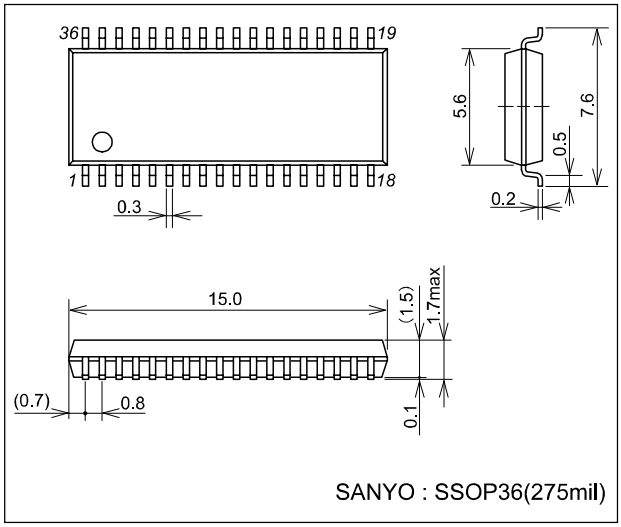
* Normally measurement condition is Input = SIF mode (-90dBμV), ALC = OFF

* " Reference " Items are reference levels, their specs are no-guarantee.

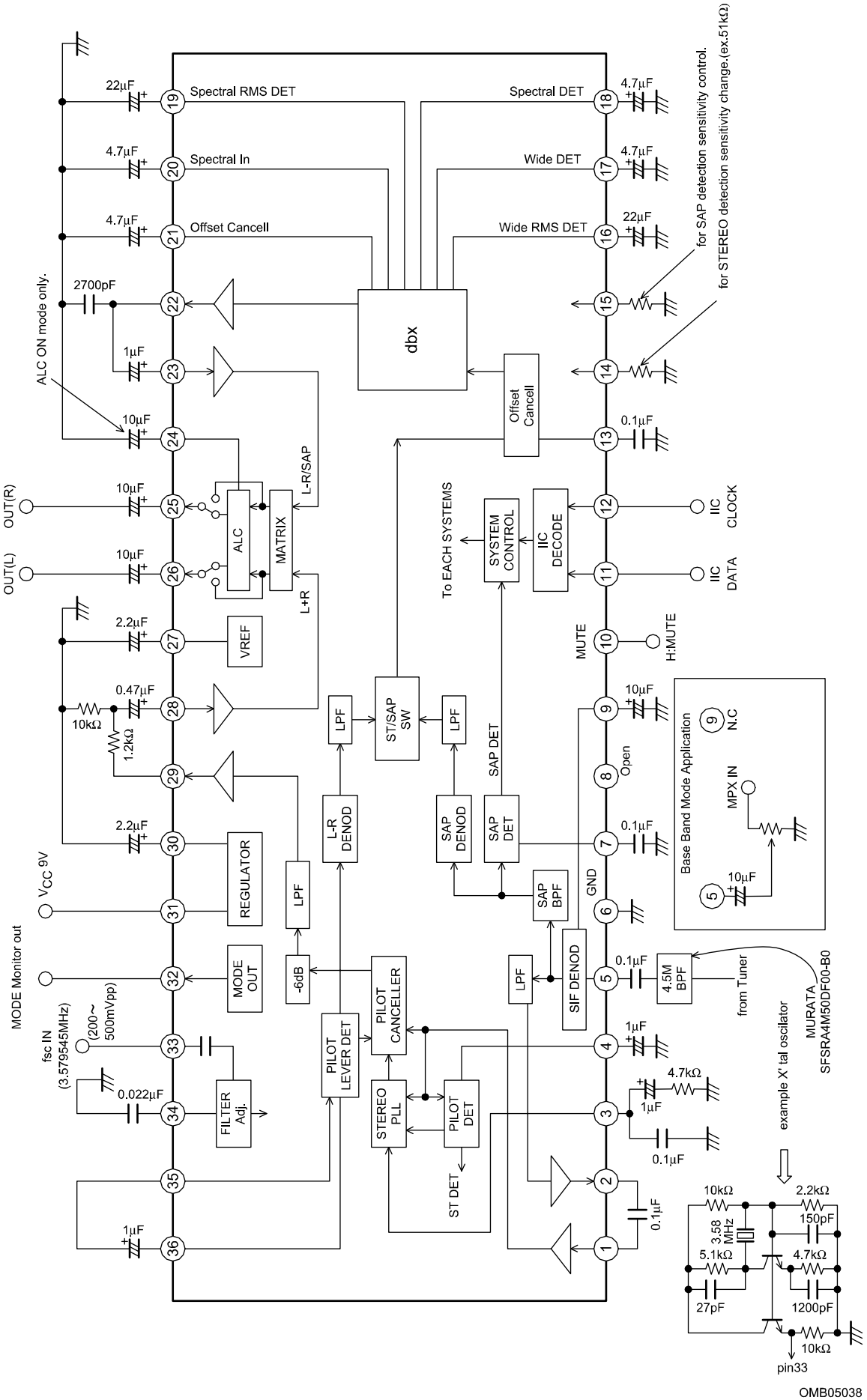
Package Dimensions

unit : mm

3247B



Block Diagram and Application Circuit Example



00p-1 (Normally use : group-1 only)

	D8	D7	D6	D5	D4	D3	D2	D1	Condition
*							0	0	Stereo
							0	1	SAP
							1	0	Both
							1	1	Prohibit
*						0			Normal (Auto det)
						1			Forced Mono
*					0				Normal (MUTE off)
					1				MUTE
*				0					ALC off (Through)
				1					ALC on
*			0						SAP LEVEL-1
			1						SAP LEVEL-2
*		0							SIF mode
		1							Base Band mode
*	0								Fix
	1								Prohibit (TEST MODE)

*: Initial condition

Read out data

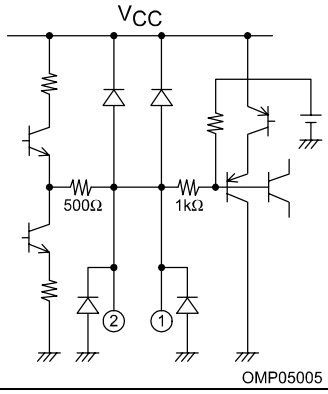
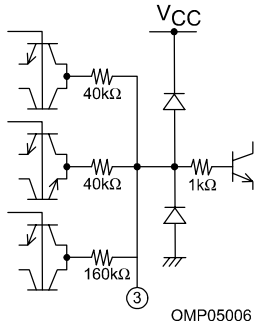
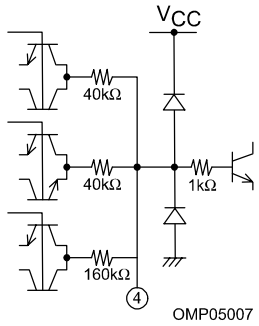
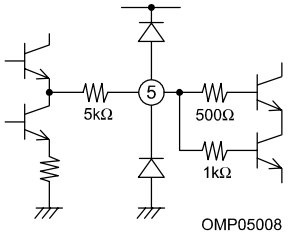
D8	D7	D6	D5	D4	D3	D2	D1	Condition
		0	0	0	0	0	0	Fixed
	0							Normal
	1							SAP det
0								Normal
1								Stereo det

Test mode condition

When STOP condition transform at Grp-1 data-end, controlled NORMAL mode.
Grp-2(Only test condition: Normally, this data is no-need)

D8	D7	D6	D5	D4	D3	D2	D1	Condition/Monitor position
0	0	0	0	0	0	0	0	Normal (Usually, Fixed)
0	0	0	0	0	0	0	1	TEST-1 SIF output
0	0	0	0	0	0	1	0	TEST-2 SAP BPF
0	0	0	0	0	0	1	1	TEST-3 SAP VCO
0	0	0	0	0	1	0	0	TEST-4 ST VCO
0	0	0	0	0	1	0	1	TEST-5 ADJ VCO
0	0	0	0	0	1	1	0	TEST-6 dbx input
0	0	0	0	0	1	1	1	TEST-7 L-R Demod output
0	0	0	0	1	0	0	0	TEST-8 Pilot cancel
0	0	0	0	1	0	0	1	TEST-9 dbx 2.19k LPF
0	0	0	0	1	0	1	0	TEST-10 dbx 408 LPF
0	0	0	0	1	0	1	1	TEST-11 dbx DET 10k LPF
0	0	0	0	1	1	0	0	TEST-12 dbx SPEC 7.6k LPF
0	0	0	0	1	1	0	1	TEST-13 dbx SPEC output
0	0	0	0	1	1	1	0	TEST-14 (No operation)
0	0	0	0	1	1	1	1	TEST-15 (No operation)

Pin Functions

No.	Pin function	DC voltage / AC level	Input/output form	Reference
1	PC_DC_IN	DC: 3.8V AC: 2.4Vp-p		AC coupling (Input)
2	PC_DCOUT	DC: 3.8V AC: 2.4Vp-p		AC coupling (Output)
3	PCSTFILT	DC: 3.8V		Stereo VCO PLL filter
4	PCPLDET	DC: 3.8V		Pilot level detect
5	PISIF	DC: 3.7V		Signal input

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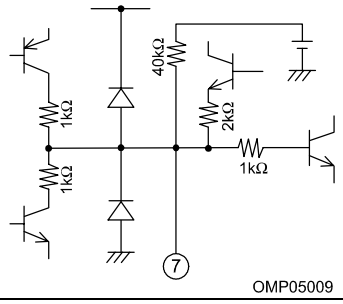
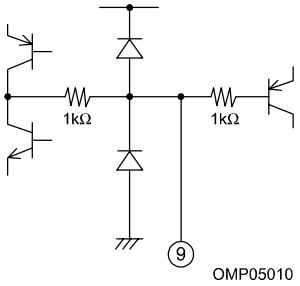
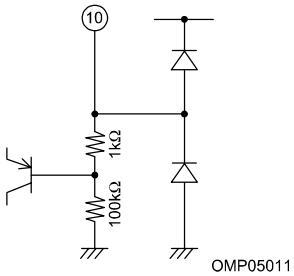
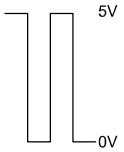
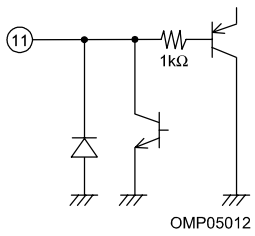
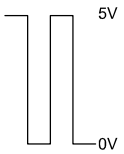
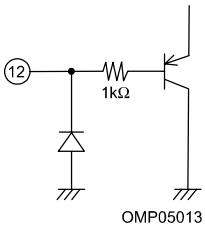
No.	Pin function	DC voltage / AC level	Input/output form	Reference
6	GND			
	CSAPDET	DC: 2.8V		SAP carrier level detect
8	NC			No connect
9	PC FIL	DC: 2.9V		SIF offset cancel
10	MUTE	DC: 0V		MUTE = 5V
11	SDA			Serial data input
12	SCL			Serial clock input

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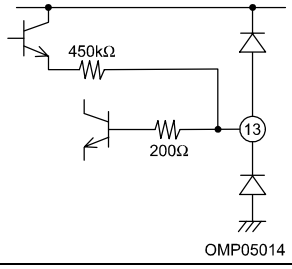
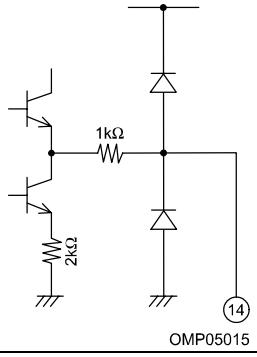
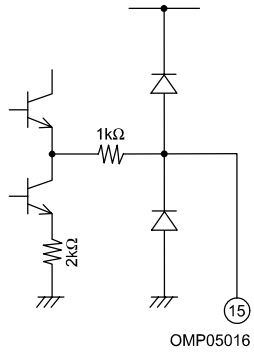
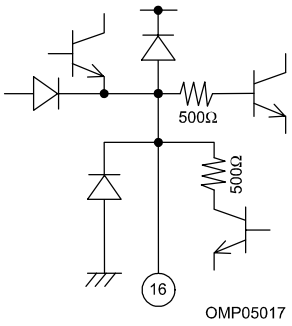
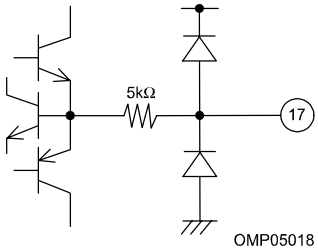
No.	Pin function	DC voltage / AC level	Input/output form	Reference
13	PC DBXIN	DC: 2.5V		Offset cancel filter
14	PSTSENS	DC: 3.1V		Stereo det sensitivity change OPEN = default Insert resistor(30k or over) = Low sensitivity
15	PSAPSENS	DC: 3.1V		SAP detect sensitivity control OPEN = default controlled by insert resistor * see electrical reference
16	PCTNWID	DC: 4.0V		dbx RMS detect(wide band)
17	PCDETWID	DC: 3.8V		dbx wide detect

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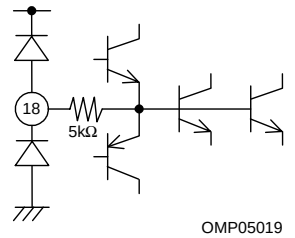
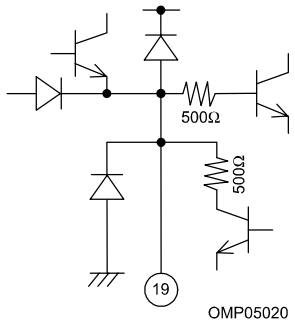
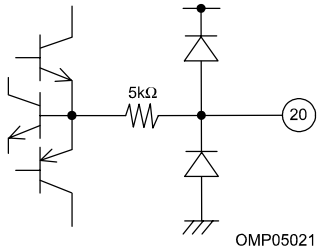
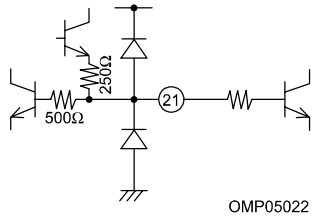
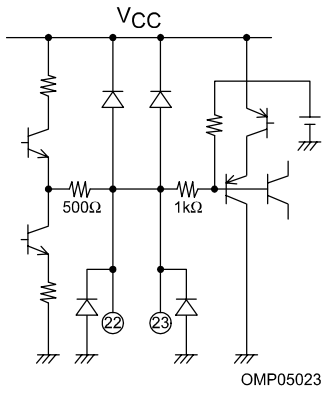
No.	Pin function	DC voltage / AC level	Input/output form	Reference
18	PCTIMSPE	DC: 3.8V		dbx spectral detect
19	PCDETSPE	DC: 3.8V		dbx RMS detect (Spectral band)
20	PCSPECIN	DC: 3.8V		dbx main signal V/I convert filter
21	PCDOSPE	DC: 3.8V AC: 220mVp-p		Offset cancel filter
22	PCDBXOUT	DC: 3.8V AC: 220mVp-p		AC coupling (Output)
23	PCDBX_IN			AC coupling (Input)

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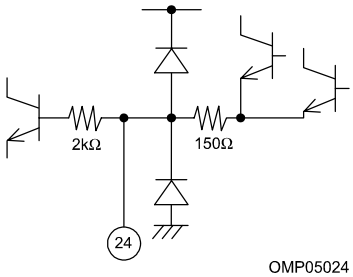
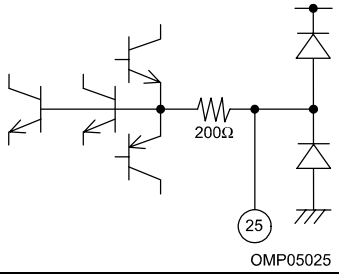
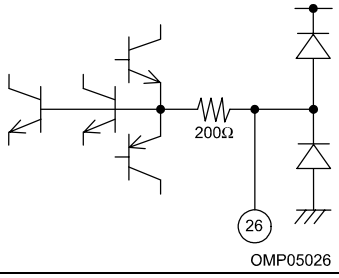
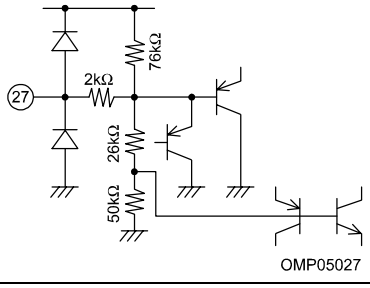
No.	Pin function	DC voltage / AC level	Input/output form	Reference
24	PCALCFIL	DC: 0.6V		ALC filter * When ALC function no-use, this terminal is open.
25	PORCH	DC: 3.8V AC: 1.4mVp-p		Line out R
26	POLCH	DC: 3.8V AC: 1.4mVp-p		Line out L
27	PCREG	DC: 3.8V		Reference Voltage

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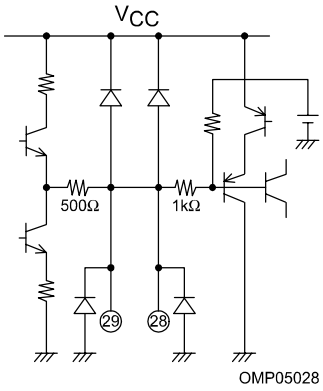
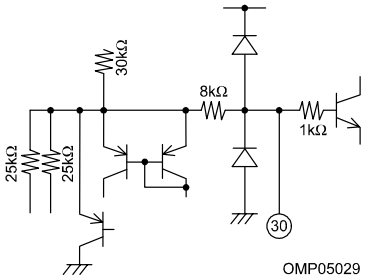
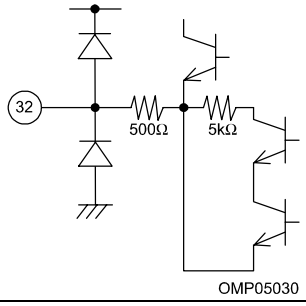
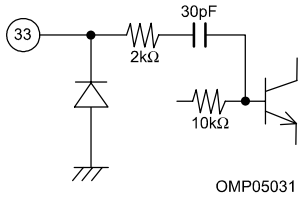
No.	Pin function	DC voltage / AC level	Input/output form	Reference
28	PMAIN_IN	DC: 3.5V AC: 220mVp-p		AC coupling (Input)
29	PMAINOUT	DC: 3.8V AC: 220mVp-p		AC coupling (Output)
30	PCREG76	DC: 1.2V		Regulator
31	V_{CC}			
32	POLED	DC* * See Mode table		Mode out MONO = 0.9V SAP = 2.0V STEREO = 3.0V STEREO+SAP = 3.8V
33	PICLKFSC	DC: 0V AC* * 200mVp-p Recommend		Fsc input 3.579545MHz, 200mVp-p

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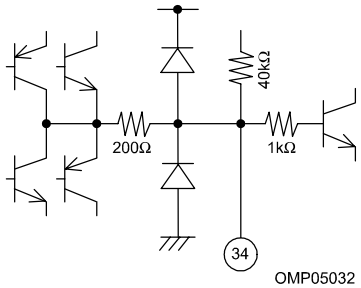
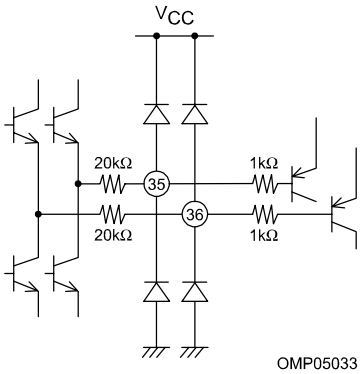
No.	Pin function	DC voltage / AC level	Input/output form	Reference
34	PCDJFIL	DC: 2.5V		Filter adjustment signal detect
35	PCPLC	DC: 6.3V		Pilot canceller reference-1
36	PCPLC2	DC: 6.3V		Pilot canceller reference-2

Serial Control (I^2C)

(1) Data Transfer Manual

This LSI adopts control method (I^2C -BUS) with serial data, and controlled by two terminals which called SCL (serial clock) and SDA (serial data). At first, set up *1 the condition of starting data transfer, and after that, input 8 bit data to SDA terminal with synchronized SCL terminal clock. The order of transferring is first, MSB (the Most Scale of Bit), and save the order. The 9th bit takes ACK (Acknowledge) period, during SCL terminal takes 'H', this LSI pull down the SDA terminal. After transferred the necessary data, two terminals lead to set up and of *2 data transfer stop condition, thus the transfer comes to close.

*1 Defined by SCL rise down SDA during 'H' period.

*2 Defined by SCL rise up SDA during 'H' period.

(2) Transfer Data Format

After transfer start condition, transfers slave address (1000000*) to SDA terminal, control data, then, stop condition (See figure 1).

Slave address is made up of 7bits, *3 8th bit shows the direction of transferring data, if it is "L", takes write mode (As this LSI side, this is input operation mode), and in case of 'H', reading mode (As this LSI side, this is output operation mode).

Data works with all of bit, transfer the stop condition before stop 8bit transfer, and to stop transfer, it will be canceled the transfer dates.

*3 It is called R/W bit.

Fig.1 DATA STRUCTURE " WRITE " mode

START Condition	Slave Address	R/W L	ACK	Control data	ACK	STOP condition

Fig.2 DATA STRUCTURE " READ " mode

START condition	Slave Address	R/W H	ACK	Internal Data*	ACK	STOP condition

* Output 5bits data as follows;

bit8 is result of STERO DET (H: STEREO)

bit7 is result of SAP DET (H: SAP)

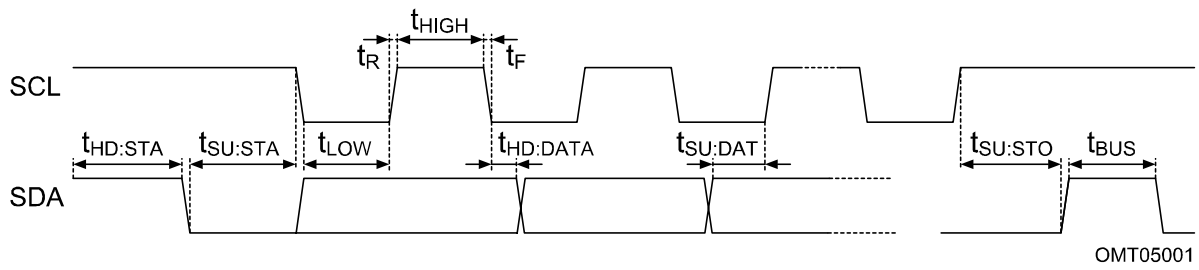
bit6 to bit1 are fixed to "L"

(3) Initialize

This LSI is initialized for circuit protection. Initial condition is “0 (all bits)”.

Parameter	Symbol	Min	Max	Unit
LOW level input voltage	V_{IL}	-0.5	1.5	V
HIGH level input voltage	VI_{IH}	3.0	5.5	V
LOW level output current	I_{OL}		3.0	mA
SCL clock frequency	f_{SCL}	0	100	kHz
Set-up time for a repeated START condition	$t_{SU: STA}$	4.7		µs
Hold time START condition. After this period, the first clock pulse is generated	$t_{HD: STA}$	4.0		µs
LOW period of the SCL clock	t_{LOW}	4.7		µs
Rise time of both SDA and SDL signals	t_R	0	1.0	µs
HIGH period of the SCL clock	t_{HIGH}	4.0		µs
Fall time of both SDA and SDL signals	t_F	0	1.0	µs
Data hold time	$t_{HD: DAT}$	0		µs
Data set-up time	$t_{SU: DAT}$	250		ns
Set-up time for STOP condition	$t_{SU: STO}$	4.0		µs
BUS free time between a STOP and START condition	t_{BUF}	4.7		µs

Timing Chart



Measurement Circuit