

FEATURES

Internal HDCP keys

HDMI interface

Supports high bandwidth digital content protection

RGB to YCbCr 2-way color conversion

1.8 V/3.3 V power supply

100-lead Pb-free LQFP

RGB and YCbCr output formats

Digital video interface

HDMI 1.1, DVI 1.0

150 MHz HDMI receiver

Supports high bandwidth digital content protection (HDCP 1.1)

Digital audio interface

HDMI 1.1-compatible audio interface

S/PDIF (IEC90658-compatible) digital audio output

Multichannel I²S audio output (up to 8 channels)

APPLICATIONS

Advanced TVs

HDTVs

Projectors

LCD monitors

GENERAL DESCRIPTION

The AD9381 offers a high definition multimedia interface (HDMI) receiver integrated on a single chip. Also included is support for high bandwidth digital content protection (HDCP) via an internal key storage.

The AD9381 contains an HDMI 1.0-compatible receiver and supports all HDTV formats (up to 1080p) and display resolutions up to SXGA (1280×1024 @ 75 Hz). The receiver features an intrapair skew tolerance of up to one full clock cycle. With the inclusion of HDCP, displays may now receive encrypted video content. The AD9381 allows for authentication of a video receiver, decryption of encoded data at the receiver, and renewability of that authentication during transmission as specified by the HDCP 1.1 protocol.

FUNCTIONAL BLOCK DIAGRAM

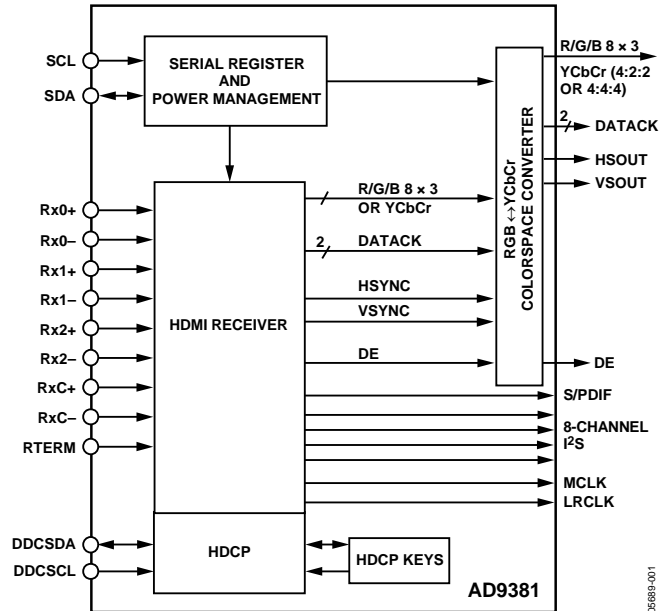


Figure 1.

Fabricated in an advanced CMOS process, the AD9381 is provided in a space-saving, 100-lead, surface-mount, Pb-free plastic LQFP and is specified over the 0°C to 70°C temperature range.

Rev. 0

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REVISION HISTORY**10/05—Revision 0: Initial Version**

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

V_{DD} , $V_D = 3.3$ V, $DV_{DD} = PV_{DD} = 1.8$ V, ADC clock = maximum.

Table 1.

| Parameter | Temp | Test Level | AD9381KSTZ-100 | | | AD9381KSTZ-150 | | | Unit |
|------------------------------------|------|------------|----------------|--------|-----|----------------|--------|-----|------|
| | | | Min | Typ | Max | Min | Typ | Max | |
| DIGITAL INPUTS (5 V Tolerant) | | | | | | | | | |
| Input Voltage, High (V_{IH}) | Full | VI | 2.6 | | | 2.6 | | | V |
| Input Voltage, Low (V_{IL}) | Full | VI | | | 0.8 | | | 0.8 | V |
| Input Current, High (I_{IH}) | Full | V | | −82 | | | −82 | | μA |
| Input Current, Low (I_{IL}) | Full | V | | 82 | | | 82 | | μA |
| Input Capacitance | 25°C | V | | 3 | | | 3 | | pF |
| DIGITAL OUTPUTS | | | | | | | | | |
| Output Voltage, High (V_{OH}) | Full | VI | $V_{DD} - 0.1$ | | | $V_{DD} - 0.1$ | | | V |
| Output Voltage, Low (V_{OL}) | Full | VI | | | 0.4 | | | 0.4 | V |
| Duty Cycle, DATAACK | Full | V | 45 | 50 | 55 | 45 | 50 | 55 | % |
| Output Coding | | | | Binary | | | Binary | | |
| THERMAL CHARACTERISTICS | | | | | | | | | |
| θ_{JA} -Junction-to-Ambient | | V | | 35 | | | 35 | | °C/W |

DIGITAL INTERFACE ELECTRICAL CHARACTERISTICS

$V_{DD} = V_D = 3.3$ V, $DV_{DD} = PV_{DD} = 1.8$ V, ADC clock = maximum.

Table 2.

| Parameter | Test Level | Conditions | AD9381KSTZ-100 | | | AD9381KSTZ-150 | | | Unit |
|---|------------|---------------------|----------------|-----|------------------|----------------|-----|------------------|------|
| | | | Min | Typ | Max | Min | Typ | Max | |
| RESOLUTION | | | | 8 | | | 8 | | Bit |
| DC DIGITAL I/O Specifications | | | | | | | | | |
| High-Level Input Voltage, (V_{IH}) | VI | | 2.5 | | | 2.5 | | | V |
| Low-Level Input Voltage, (V_{IL}) | VI | | | | 0.8 | | | 0.8 | V |
| High-Level Output Voltage, (V_{OH}) | VI | | $V_{DD} - 0.1$ | | | | | | V |
| Low-Level Output Voltage, (V_{OL}) | VI | | $V_{DD} - 0.1$ | | 0.1 | | | 0.1 | V |
| DC SPECIFICATIONS | | | | | | | | | |
| Output High Level | IV | Output drive = high | | 36 | | | 36 | | mA |
| I_{OHD} , ($V_{OUT} = V_{OH}$) | IV | Output drive = low | | 24 | | | 24 | | mA |
| Output Low Level | IV | Output drive = high | | 12 | | | 12 | | mA |
| I_{OLD} , ($V_{OUT} = V_{OL}$) | IV | Output drive = low | | 8 | | | 8 | | mA |
| DATAACK High Level | IV | Output drive = high | | 40 | | | 40 | | mA |
| V_{OHC} , ($V_{OUT} = V_{OH}$) | IV | Output drive = low | | 20 | | | 20 | | mA |
| DATAACK Low Level | IV | Output drive = high | | 30 | | | 30 | | mA |
| V_{OLC} , ($V_{OUT} = V_{OL}$) | IV | Output drive = low | | 15 | | | 15 | | mA |
| Differential Input Voltage, Single-Ended Amplitude | IV | | 75 | | 700 | 75 | | 700 | mV |
| POWER SUPPLY | | | | | | | | | |
| V_D Supply Voltage | IV | | 3.15 | 3.3 | 3.47 | 3.15 | 3.3 | 3.47 | V |
| V_{DD} Supply Voltage | IV | | 1.7 | 3.3 | 347 | 1.7 | 3.3 | 347 | V |
| DV_{DD} Supply Voltage | IV | | 1.7 | 1.8 | 1.9 | 1.7 | 1.8 | 1.9 | V |
| PV_{DD} Supply Voltage | IV | | 1.7 | 1.8 | 1.9 | 1.7 | 1.8 | 1.9 | V |
| I_{VD} Supply Current (Typical Pattern) ¹ | V | | | 80 | 100 | | 80 | 110 | mA |
| I_{VDD} Supply Current (Typical Pattern) ² | V | | | 40 | 100 ³ | | 55 | 175 ³ | mA |

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| Parameter | Test Level | Conditions | AD9381KSTZ-100 | | | AD9381KSTZ-150 | | | Unit |
|---|------------|---|----------------|-----|------|----------------|-----|------|--------------|
| | | | Min | Typ | Max | Min | Typ | Max | |
| I _{DVDD} Supply Current (Typical Pattern) ^{1, 4} | V | | | 88 | 110 | | 110 | 145 | mA |
| I _{PVDD} Supply Current (Typical Pattern) ¹ | V | | | 26 | 35 | | 30 | 40 | mA |
| Power-Down Supply Current (I _{PD}) | VI | | | 130 | | | 130 | | mA |
| AC SPECIFICATIONS | | | | | | | | | |
| Intrapair (+ to -) Differential Input Skew (T _{DPS}) | IV | | | | | | | 360 | ps |
| Channel to Channel Differential Input Skew (T _{CCS}) | IV | | | | | | | 6 | Clock Period |
| Low-to-High Transition Time for Data and Controls (D _{LHT}) | IV | Output drive = high; C _L = 10 pF | | | | | | 900 | ps |
| | IV | Output drive = low; C _L = 5 pF | | | | | | 1300 | ps |
| Low-to-High Transition Time for DATAACK (D _{LHT}) | IV | Output drive = high; C _L = 10 pF | | | | | | 650 | ps |
| | IV | Output drive = low; C _L = 5 pF | | | | | | 1200 | ps |
| High-to-Low Transition Time for Data and Controls (D _{HLT}) | IV | Output drive = high; C _L = 10 pF | | | | | | 850 | ps |
| | IV | Output drive = low; C _L = 5 pF | | | | | | 1250 | ps |
| High-to-Low Transition Time for DATAACK (D _{HLT}) | IV | Output drive = high; C _L = 10 pF | | | | | | 800 | ps |
| | IV | Output drive = low; C _L = 5 pF | | | | | | 1200 | ps |
| Clock to Data Skew ⁵ (T _{SKEW}) | IV | | -0.5 | | +2.0 | -0.5 | | +2.0 | ns |
| Duty Cycle, DATAACK ⁵ | IV | | 45 | 50 | | | | 55 | % |
| DATAACK Frequency (F _{CIP}) | VI | | 20 | | | | | 150 | MHz |

¹ The typical pattern contains a gray scale area, output drive = high. Worst-case pattern is alternating black and white pixels.

² The typical pattern contains a gray scale area, output drive = high.

³ Specified current and power values with a worst-case pattern (on/off).

⁴ DATAACK load = 10 pF, data load = 5 pF.

⁵ Drive strength = high.

ABSOLUTE MAXIMUM RATINGS

Table 3.

| Parameter | Rating |
|------------------------------|-----------------|
| V_D | 3.6 V |
| V_{DD} | 3.6 V |
| DV_{DD} | 1.98 V |
| PV_{DD} | 1.98 V |
| Analog Inputs | V_D to 0.0 V |
| Digital Inputs | 5 V to 0.0 V |
| Digital Output Current | 20 mA |
| Operating Temperature Range | -25°C to +85°C |
| Storage Temperature Range | -65°C to +150°C |
| Maximum Junction Temperature | 150°C |
| Maximum Case Temperature | 150°C |

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

EXPLANATION OF TEST LEVELS

Table 4.

| Level | Test |
|-------|--|
| I | 100% production tested. |
| II | 100% production tested at 25°C and sample tested at specified temperatures. |
| III | Sample tested only. |
| IV | Parameter is guaranteed by design and characterization testing. |
| V | Parameter is a typical value only. |
| VI | 100% production tested at 25°C; guaranteed by design and characterization testing. |

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

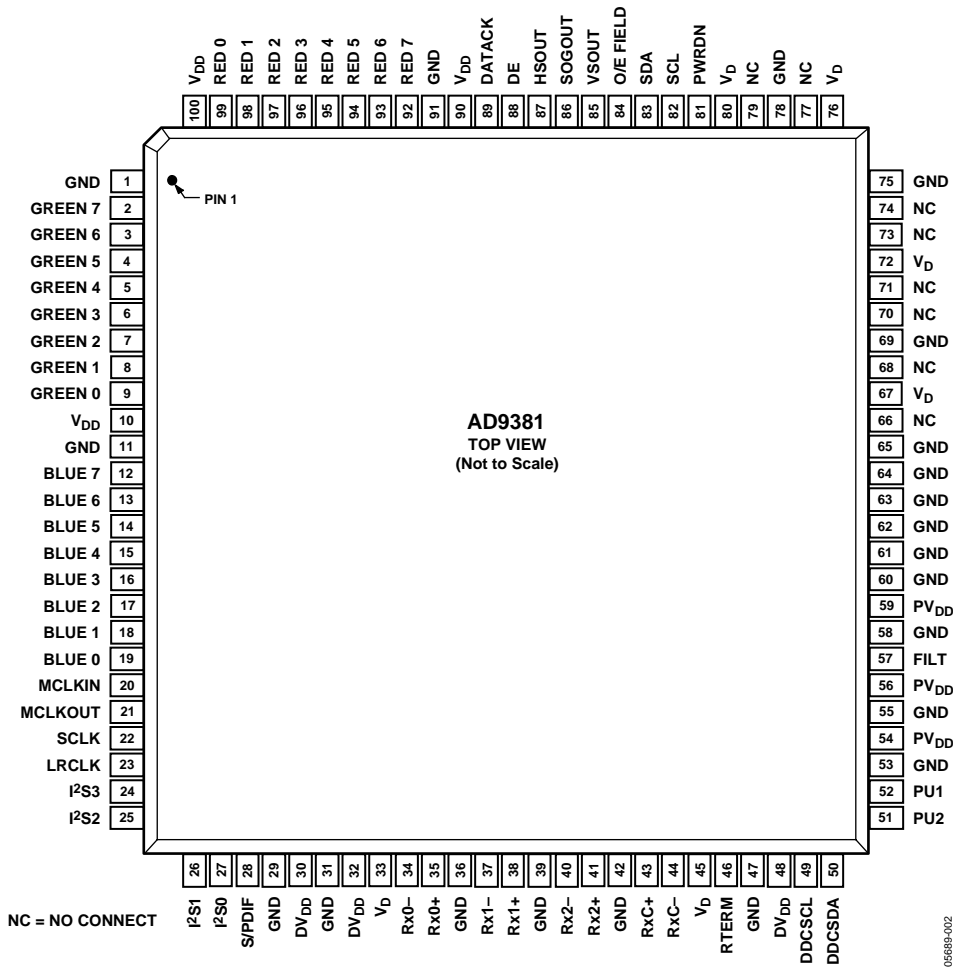


Figure 2. Pin Configuration

Table 5. Complete Pinout List

| Pin Type | Pin No. | Mnemonic | Function | Value |
|----------------------------|----------|-------------|---|-----------------|
| INPUTS | 81 | PWRDN | Power-Down Control | 3.3 V CMOS |
| DIGITAL VIDEO DATA INPUTS | 35 | Rx0+ | Digital Input Channel 0 True | TMDS |
| | 34 | Rx0- | Digital Input Channel 0 Complement | TMDS |
| | 38 | Rx1+ | Digital Input Channel 1 True | TMDS |
| | 37 | Rx1- | Digital Input Channel 1 Complement | TMDS |
| | 41 | Rx2+ | Digital Input Channel 2 True | TMDS |
| | 40 | Rx2- | Digital Input Channel 2 Complement | TMDS |
| DIGITAL VIDEO CLOCK INPUTS | 43 | RxC+ | Digital Data Clock True | TMDS |
| | 44 | RxC- | Digital Data Clock Complement | TMDS |
| OUTPUTS | 92 to 99 | RED [7:0] | Outputs of Red Converter, Bit 7 is MSB | V _{DD} |
| | 2 to 9 | GREEN [7:0] | Outputs of Green Converter, Bit 7 is MSB | V _{DD} |
| | 12 to 19 | BLUE [7:0] | Outputs of Blue Converter, Bit 7 is MSB | V _{DD} |
| | 89 | DATAACK | Data Output Clock | V _{DD} |
| | 87 | HSOUT | HSYNC Output Clock (Phase-Aligned with DATAACK) | V _{DD} |
| | 85 | VSOUT | VSYNC Output Clock (Phase-Aligned with DATAACK) | V _{DD} |
| | 86 | SOGOUT | SOG Slicer Output | V _{DD} |
| | 84 | O/E FIELD | Odd/Even Field Output | V _{DD} |

| Pin Type | Pin No. | Mnemonic | Function | Value |
|--------------------|------------------------|-------------------|--|------------------|
| REFERENCES | 57 | FILT | Connection for External Filter Components for Audio PLL | PV _{DD} |
| POWER SUPPLY | 80, 76, 72, 67, 45, 33 | V _D | Analog Power Supply and DVI Terminators | 3.3 V |
| | 100, 90, 10 | V _{DD} | Output Power Supply | 1.8 V to 3.3 V |
| | 59, 56, 54 | PV _{DD} | PLL Power Supply | 1.8 V |
| | 48, 32, 30 | DV _{DD} | Digital Logic Power Supply | 1.8 V |
| | | GND | Ground | 0 V |
| CONTROL | 83 | SDA | Serial Port Data I/O | 3.3 V CMOS |
| | 82 | SCL | Serial Port Data Clock | 3.3 V CMOS |
| HDCP | 49 | DDCSCL | HDCP Slave Serial Port Data Clock | 3.3 V CMOS |
| | 50 | DDCSDA | HDCP Slave Serial Port Data I/O | 3.3 V CMOS |
| | 51 | PU2 | This should be pulled up to 3.3 V through a 10 k Ω resistor | 3.3 V CMOS |
| | 52 | PU1 | This should be pulled up to 3.3 V through a 10 k Ω resistor | 3.3 V CMOS |
| AUDIO DATA OUTPUTS | 28 | S/PDIF | S/PDIF Digital Audio Output | V _{DD} |
| | 27 | I ² S0 | I ² S Audio (Channel 1, Channel 2) | V _{DD} |
| | 26 | I ² S1 | I ² S Audio (Channels 3, Channel 4) | V _{DD} |
| | 25 | I ² S2 | I ² S Audio (Channels 5, Channel 6) | V _{DD} |
| | 24 | I ² S3 | I ² S Audio (Channels 7, Channel 8) | V _{DD} |
| | 20 | MCLKIN | External Reference Audio Clock In | V _{DD} |
| | 21 | MCLKOUT | Audio Master Clock Output | V _{DD} |
| | 22 | SCLK | Audio Serial Clock Output | V _{DD} |
| | 23 | LRCLK | Data Output Clock for Left and Right Audio Channels | V _{DD} |
| DATA ENABLE | 88 | DE | Data Enable | 3.3 V CMOS |
| RTERM | 46 | RTERM | Sets Internal Termination Resistance | 500 Ω |

Table 6. Pin Function Descriptions

| Mnemonic | Description |
|----------|--|
| INPUTS | |
| Rx0+ | Digital Input Channel 0 True. |
| Rx0- | Digital Input Channel 0 Complement. |
| Rx1+ | Digital Input Channel 1 True. |
| Rx1- | Digital Input Channel 1 Complement. |
| Rx2+ | Digital Input Channel 2 True. |
| Rx2- | Digital Input Channel 2 Complement. |
| | These six pins receive three pairs of transition minimized differential signaling (TMDS) pixel data (at 10 \times the pixel rate) from a digital graphics transmitter. |
| RxC+ | Digital Data Clock True. |
| RxC- | Digital Data Clock Complement. |
| | This clock pair receives a TMDS clock at 1 \times pixel data rate. |
| FILT | External Filter Connection. For proper operation, the audio clock generator PLL requires an external filter. Connect the filter shown in Figure 8 to this pin. For optimal performance, minimize noise and parasitics on this node. For more information see the PCB Layout Recommendations section . |
| PWRDN | Power-Down Control/Three-State Control. The function of this pin is programmable via Register 0x26 [2:1]. |

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| Mnemonic | Description |
|----------------------------------|---|
| OUTPUTS | |
| HSOUT | Horizontal Sync Output. A reconstructed and phase-aligned version of the HSYNC input. Both the polarity and duration of this output can be programmed via serial bus registers. By maintaining alignment with DATAACK and Data, data timing with respect to horizontal sync can always be determined. |
| VSOUT | Vertical Sync Output. The separated VSYNC from a composite signal or a direct pass through of the VSYNC signal. The polarity of this output can be controlled via the serial bus bit (Register 0x24[6]). |
| O/E FIELD | Odd/Even Field Bit for Interlaced Video. This output identifies whether the current field (in an interlaced signal) is odd or even. The polarity of this signal is programmable via Register 0x24[4]. |
| SERIAL PORT | |
| SDA | Serial Port Data I/O for Programming AD9381 Registers—I ² C Address is 0x98. |
| SCL | Serial Port Data Clock for Programming AD9381 Registers. |
| DDCSDA | Serial Port Data I/O for HDCP Communications to Transmitter—I ² C Address is 0x74 or 0x76. |
| DDCSCL | Serial Port Data Clock for HDCP Communications to Transmitter. |
| PU2 | This should be pulled up to 3.3 V through a 10 k Ω resistor. |
| PU1 | This should be pulled up to 3.3 V through a 10 k Ω resistor. |
| DATA OUTPUTS | |
| Red [7:0] | Data Output, Red Channel. |
| Green [7:0] | Data Output, Green Channel. |
| Blue [7:0] | Data Output, Blue Channel. |
| | The main data outputs. Bit 7 is the MSB. The delay from pixel sampling time to output is fixed, but will be different if the color space converter is used. When the sampling time is changed by adjusting the phase register, the output timing is shifted as well. The DATAACK and HSOUT outputs are also moved, so the timing relationship among the signals is maintained. |
| DATA CLOCK OUTPUT | |
| DATAACK | Data Clock Output. This is the main clock output signal used to strobe the output data and HSOUT into external logic. Four possible output clocks can be selected with Register 0x25[7:6]. These are related to the pixel clock (1/2 \times pixel clock, 1 \times pixel clock, 2 \times frequency pixel clock, and a 90° phase shifted pixel clock). They are produced either by the internal PLL clock generator or EXTCLK and are synchronous with the pixel sampling clock. The polarity of DATAACK can also be inverted via Register 0x24[0]. The sampling time of the internal pixel clock can be changed by adjusting the phase register. When this is changed, the pixel-related DATAACK timing is shifted as well. The DATA, DATAACK, and HSOUT outputs are all moved, so the timing relationship among the signals is maintained. |
| POWER SUPPLY ¹ | |
| V _D (3.3 V) | Analog Power Supply. These pins supply power to the ADCs and terminators. They should be as quiet and filtered as possible. |
| V _{DD} (1.8 V to 3.3 V) | Digital Output Power Supply. A large number of output pins (up to 27) switching at high speed (up to 150 MHz) generates many power supply transients (noise). These supply pins are identified separately from the V _D pins so special care can be taken to minimize output noise transferred into the sensitive analog circuitry. If the AD9381 is interfacing with lower voltage logic, V _{DD} may be connected to a lower supply voltage (as low as 1.8 V) for compatibility. |
| PV _{DD} (1.8 V) | Clock Generator Power Supply. The most sensitive portion of the AD9381 is the clock generation circuitry. These pins provide power to the clock PLL and help the user design for optimal performance. The designer should provide quiet, noise-free power to these pins. |
| DV _{DD} (1.8 V) | Digital Input Power Supply. This supplies power to the digital logic. |
| GND | Ground. The ground return for all circuitry on chip. It is recommended that the AD9381 be assembled on a single solid ground plane, with careful attention to ground current paths. |

¹ The supplies should be sequenced such that V_D and V_{DD} are never less than 300 mV below DV_{DD}. At no time should DV_{DD} be more than 300 mV greater than V_D or V_{DD}.

DESIGN GUIDE

GENERAL DESCRIPTION

The AD9381 is a fully integrated solution for receiving DVI/HDMI signals and is capable of decoding HDCP-encrypted signals through connections to an internal EEPROM. The circuit is ideal for providing an interface for HDTV monitors or as the front end to high performance video scan converters.

Implemented in a high performance CMOS process, the interface can capture signals with pixel rates of up to 150 MHz.

The AD9381 includes all necessary circuitry for decoding TMDS signaling including those encrypted with HDCP. The output data formatting includes a color space converter (CSC), which accommodates any input color space and can output any color space. All controls are programmable via a 2-wire serial interface. Full integration of these sensitive mixed signal functions makes system design straight-forward and less sensitive to the physical and electrical environment.

DIGITAL INPUTS

The digital control inputs (I^2C) on the AD9381 operate to 3.3 V CMOS levels. In addition, all digital inputs, except the TMDS (HDMI/DVI) inputs, are 5 V tolerant (applying 5 V to them does not cause damage). The TMDS input pairs (Rx0+/Rx0-, Rx1+/Rx1-, Rx2+/Rx2-, and RxC+/RxC-) must maintain a 100 Ω differential impedance (through proper PCB layout) from the connector to the input where they are internally terminated (50 Ω to 3.3 V). If additional ESD protection is desired, use of a California Micro Devices (CMD) CM1213 (among others) series low capacitance ESD protection offers 8 kV of protection to the HDMI TMDS lines.

SERIAL CONTROL PORT

The serial control port is designed for 3.3 V logic. However, it is tolerant of 5 V logic signals.

OUTPUT SIGNAL HANDLING

The digital outputs operate from 1.8 V to 3.3 V (V_{DD}).

Power Management

The AD9381 uses the activity detect circuits, the active interface bits in the serial bus, the active interface override bits, the power-down bit, and the power-down pin to determine the correct power state. There are four power states: full-power, seek mode, auto power-down, and power-down.

Table 7 summarizes how the AD9381 determines which power mode to use and which circuitry is powered on/off in each of these modes. The power-down command has priority and then the automatic circuitry. The power-down pin (Pin 81—polarity set by Register 0x26[3]) can drive the chip into four power-down options. Bit 2 and Bit1 of Register 0x26 control these four options. Bit 0 controls whether the chip is powered down or the outputs are placed in high impedance mode (with the exception of SOG). Bit 7 to Bit 4 of Register 0x26 control whether the outputs, SOG, Sony Philips digital interface (S/PDIF) or Inter-IC sound bus (I^2S or IIS) outputs are in high impedance mode or not. See the 2-Wire Serial Control Register Detail section for more details.

Table 7. Power-Down Mode Descriptions

| Mode | Inputs | | | Power-On or Comments |
|------------|-------------------------|--------------------------|-----------------------------|---|
| | Power-Down ¹ | Sync Detect ² | Auto PD Enable ³ | |
| Full Power | 1 | 1 | X | Everything |
| Seek Mode | 1 | 0 | 0 | Everything |
| Seek Mode | 1 | 0 | 1 | Serial bus, sync activity detect, SOG, band gap reference |
| Power-Down | 0 | X | | Serial bus, sync activity detect, SOG, band gap reference |

¹ Power-down is controlled via Bit 0 in Serial Bus Register 0x26.

² Sync detect is determined by OR'ing Bits 7 to Bit 2 in Serial Bus Register 0x15.

³ Auto power-down is controlled via Bit 7 in Serial Bus Register 0x27.

TIMING

The output data clock signal is created so that its rising edge always occurs between data transitions and can be used to latch the output data externally.

Figure 3 shows the timing operation of the AD9381.

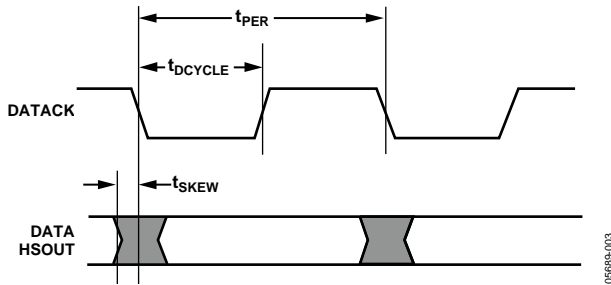


Figure 3. Output Timing

VSYNC FILTER AND ODD/EVEN FIELDS

The VSYNC filter eliminates spurious VSYNCs, maintains a consistent timing relationship between the VSYNC and HSYNC output signals, and generates the odd/even field output.

The filter works by examining the placement of VSYNC with respect to HSYNC and, if necessary, slightly shifting it in time at the VSOUT output. The goal is to keep the VSYNC and HSYNC leading edges from switching at the same time, eliminating confusion as to when the first line of a frame occurs. Enabling the VSYNC filter is done with Register 0x21[5]. Use of the VSYNC filter is recommended for all cases, including interlaced video, and is required when using the HSYNC per VSYNC counter. Figure 4 and Figure 5 illustrate even/odd field determination in two situations.

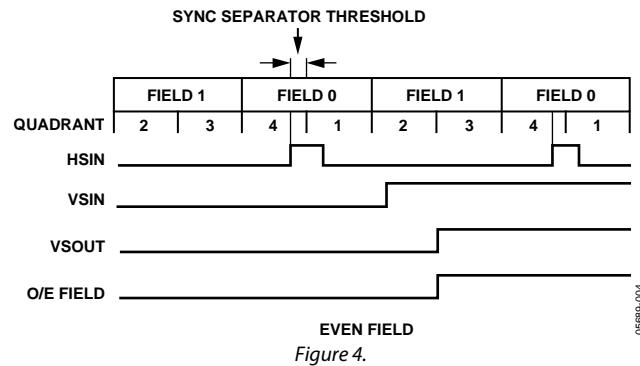


Figure 4.

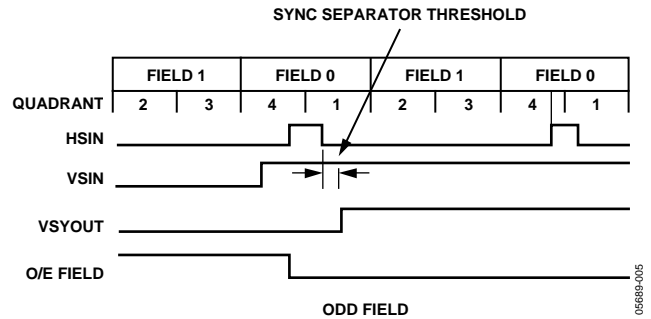


Figure 5. VSYNC Filter—Odd/Even

HDMI RECEIVER

The HDMI receiver section of the AD9381 allows the reception of a digital video stream, which is backward compatible with DVI and able to accommodate not only video of various formats (RGB, YCrCb 4:4:4, 4:2:2), but also up to eight channels of audio. Infoframes are transmitted carrying information about the video format, audio clocks, and many other items necessary for a monitor to use fully the information stream available.

The earlier digital visual interface (DVI) format was restricted to an RGB 24-bit color space only. Embedded in this data stream were HSYNCs, VSYNCs, and display enable (DE) signals, but no audio information. The HDMI specification allows transmission of all the DVI capabilities, but adds several YCrCb formats that make the inclusion of a programmable color space converter (CSC) a very desirable feature. With this, the scaler following the AD9381 can specify that it always wishes to receive a particular format—for instance, 4:2:2 YCrCb—regardless of the transmitted mode. If RGB is sent, the CSC can easily convert that to 4:2:2 YCrCb while relieving the scaler of this task.

In addition, the HDMI specification supports the transmission of up to eight channels of S/PDIF or I²S audio. The audio information is packetized and transmitted during the video blanking periods along with specific information about the clock frequency. Part of this audio information (audio Infoframe) tells the user how many channels of audio are being transmitted, where they should be placed, information regarding the source (make, model), and other data.

DE GENERATOR

The AD9381 has an onboard generator for DE, for start of active video (SAV) and for end of active video (EAV), all of which is necessary for describing the complete data stream for a BT656-compatible output. In addition to this particular output, it is possible to generate the DE for cases in which a scaler is not used. This signal alerts the following circuitry as to which are displayable video pixels.

4:4:4 TO 4:2:2 FILTER

The AD9381 contains a filter that allows it to convert a signal from YCrCb 4:4:4 to YCrCb 4:2:2 while maintaining the maximum accuracy and fidelity of the original signal.

Input Color Space to Output Color Space

The AD9381 can accept a wide variety of input formats and either retain that format or convert to another. Input formats supported are:

- 4:4:4 YCrCb 8-bit
- 4:2:2 YCrCb 8-bit, 10-bit, and 12-bit
- RGB 8-bit

Output modes supported are:

- 4:4:4 YCrCb 8-bit
- 4:2:2 YCrCb 8-bit, 10-bit, and 12-bit
- Dual 4:2:2 YCrCb 8-bit

Color Space Conversion (CSC) Matrix

The CSC matrix in the AD9381 consists of three identical processing channels. In each channel, three input values are multiplied by three separate coefficients. Also included are an offset value for each row of the matrix and a scaling multiple for all values. Each value has a 13-bit, two's complement resolution to ensure the signal integrity is maintained. The CSC is designed to run at speeds up to 150 MHz supporting resolutions up to 1080p at 60 Hz. With any-to-any color space support, formats such as RGB, YUV, YCbCr, and others are supported by the CSC.

The main inputs, R_{IN} , G_{IN} , and B_{IN} come from the 8- to 12-bit inputs from each channel. These inputs are based on the input format detailed in Table 7. The mapping of these inputs to the CSC inputs is shown in Table 8.

Table 8. CSC Port Mapping

| Input Channel | CSC Input Channel |
|---------------|-------------------|
| R/CR | R_{IN} |
| Gr/Y | G_{IN} |
| B/CB | B_{IN} |

One of the three channels is represented in Figure 6. In each processing channel, the three inputs are multiplied by three separate coefficients marked a_1 , a_2 , and a_3 . These coefficients are divided by 4096 to obtain nominal values ranging from -0.9998 to $+0.9998$. The variable labeled a_4 is used as an offset control. The CSC_Mode setting is the same for all three processing channels. This multiplies all coefficients and offsets by a factor of 2^{CSC_Mode} .

The functional diagram for a single channel of the CSC, as shown in Figure 6, is repeated for the remaining G and B channels. The coefficients for these channels are b_1 , b_2 , b_3 , b_4 , c_1 , c_2 , c_3 , and c_4 .

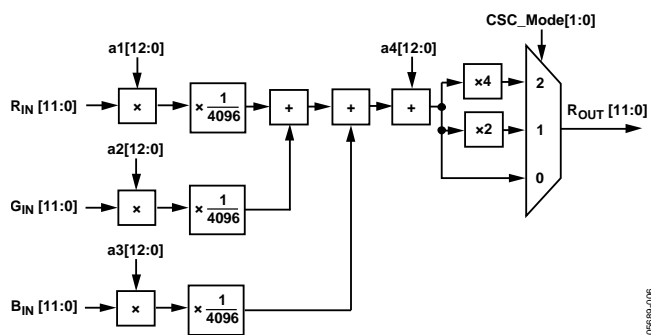


Figure 6. Single CSC Channel

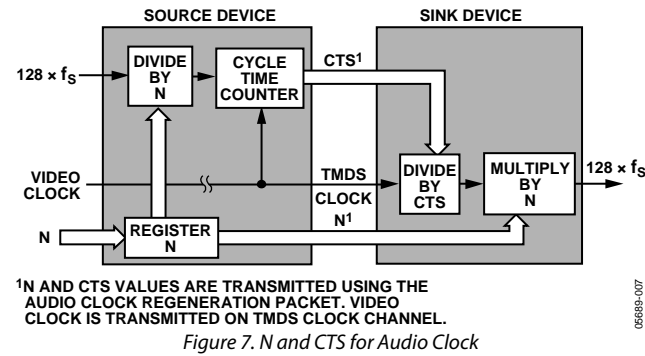
A programming example and register settings for several common conversions are listed in the Color Space Converter (CSC) Common Settings section.

For a detailed functional description and more programming examples, please refer to the application note [AN-795, AD9800 Color Space Converter User's Guide](#).

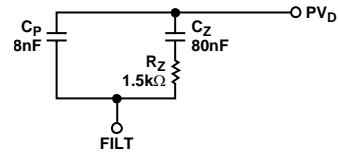
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AUDIO PLL SETUP

Data contained in the audio inframes, among other registers, define for the AD9381 HDMI receiver not only the type of audio, but the sampling frequency (f_s). The audio inframe also contains information about the N and CTS values used to recreate the clock. With this information it is possible to regenerate the audio sampling frequency. The audio clock is regenerated by dividing the 20-bit CTS value into the TMDS clock, then multiplying by the 20-bit N value. This yields a multiple of the f_s (sampling frequency) of either $128 \times f_s$ or $256 \times f_s$. It is possible for this to be specified up to $1024 \times f_s$.



In order to provide the most flexibility in configuring the audio sampling clock, an additional PLL is employed. The PLL characteristics are determined by the loop filter design, the PLL charge pump current, and the VCO range setting. The loop filter design is shown in Figure 8.



To fully support all audio modes for all video resolutions up to 1080p, it is necessary to adjust certain audio-related registers from their power-on default values. Table 9 describes these registers and gives their recommended settings.

Table 9. AD9398 Audio Register Settings

| Register | Bits | Recommended Setting | Function | Comments |
|----------|----------------------|----------------------|--|--|
| 0x01 | 7:0 | 0x00 | PLL Divisor (MSBs) | The analog video PLL is also used for the audio clock circuit when in HDMI mode. This is done automatically. |
| 0x02 | 7:4 | 0x40 | PLL Divisor (Lab's) | |
| 0x03 | 7:6 5:3 2 | 01 010 1 | VCO Range Charge Pump Current PLL Enable | |
| 0x34 | 4 | 0 | Audio Frequency Mode Override | Allows the chip to determine the low frequency mode of the audio PLL. |
| 0x58 | 7 6:4 3 2:0 | 1 011 0 0** | PLL Enable MCLK PLL Divisor N/CTS Disable MCLK Sampling Frequency | This enables the analog PLL to be used for audio MCLK generation. When the analog PLL is enabled for MCLK generation, another frequency divider is provided. These bits set the divisor to 4. The N and CTS values should always be enabled. 000 = $128 \times f_s$ 001 = $256 \times f_s$ 010 = $384 \times f_s$ 011 = $512 \times f_s$ |

AUDIO BOARD LEVEL MUTING

The audio can be muted through the infoframes or locally via the serial bus registers. This can be controlled with Register R0x57, Bits [7:4].

AVI Infoframes

The HDMI TMDS transmission contains Infoframes with specific information for the monitor such as:

- Audio information
 - 2 to 8 channels of audio identified
 - Audio coding
 - Audio sampling frequency
- Speaker placement
- N and CTS values (for reconstruction of the audio)
- Muting
- Source information
 - CD
 - SACD
 - DVD
- Video information
 - Video ID code (per CEA861B)
 - Color space
 - Aspect ratio
 - Horizontal and vertical bar information
 - MPEG frame information (I, B, or P frame)
- Vendor (transmitter source) name and product model

This information is the fundamental difference between DVI and HDMI transmissions and is located in read-only registers R0x5A to R0xEE. In addition to this information, registers are provided to indicate that new information has been received. Registers with addresses ending in 0xX7 or 0xXF beginning at R0x87 contain the new data flags (NDF) information. All of these registers contain the same information and all are reset once any of them are read. Although there is no external interrupt signal, it is easy for the user to read any of these registers and see if there is new information to be processed.

OUTPUT DATA FORMATS

The AD9398 supports 4:4:4, 4:2:2, double data-rate (DDR), and BT656 output formats. Register 0x25[3:0] controls the output mode. These modes and the pin mapping are shown in Table 10.

Table 10.

| Port | Red | | | | | | | | Green | | | | | | | | Blue | | | | | | | |
|-------------|----------------------------|---|---|---|---------------|---|---|---|---------------|---|---|---|-------------------------|---|---|---|-------------------------|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 4:4:4 | Red/Cr [7:0] | | | | | | | | Green/Y [7:0] | | | | | | | | Blue/Cb [7:0] | | | | | | | |
| 4:2:2 | CbCr [7:0] | | | | | | | | Y [7:0] | | | | | | | | DDR 4:2:2 ↑ CbCr ↓ Y, Y | | | | | | | |
| 4:4:4 DDR | DDR ↑ ¹ G [3:0] | | | | DDR ↑ B [7:4] | | | | DDR ↑ B [3:0] | | | | DDR 4:2:2 ↑ CbCr [11:0] | | | | | | | | | | | |
| | DDR ↓ R [7:0] | | | | | | | | DDR ↓ G [7:4] | | | | DDR 4:2:2 ↓ Y, Y [11:0] | | | | | | | | | | | |
| 4:2:2 to 12 | CbCr [11:0] | | | | | | | | Y [11:0] | | | | | | | | | | | | | | | |

¹ Arrows in the table indicate clock edge. Rising edge of clock = ↑, falling edge = ↓.

2-WIRE SERIAL REGISTER MAP

The AD9381 is initialized and controlled by a set of registers that determines the operating modes. An external controller is employed to write and read the control registers through the 2-wire serial interface port.

Table 11. Control Register Map

| Hex Address | Read/Write or Read Only | Bits | Default Value | Register Name | Description |
|-------------|-------------------------|--|--|---|---|
| 0x00 | Read | [7:0] | 00000000 | Chip Revision | Chip revision ID. Revision is read [7:4]. [3:0]. |
| 0x01 | Read/Write | [7:0] | 01101001 | PLL Divider MSB | PLL feedback divider value MSB. |
| 0x02 | Read/Write | [7:4] | 1101**** | PLL Divider | PLL feedback divider value. |
| 0x03 | Read/Write | [7:6] [5:3] [2] | 01***** **001*** *****0** | VCO Range Charge Pump PLL Enable | VCO range. Charge pump current control for PLL. This bit enables a lower frequency to be used for audio MCLK generation |
| 0x11 | Read/Write | [7] [6] [5] [4] [3] [2] [1] [0] | 0***** *0***** **0***** ***0**** ****0*** *****0** *****0* *****0 | HSYNC Source HSYNC Source Override VSYNC Source VSYNC Source Override Channel Select Channel Select Override Interface Select Interface Override | 0 = HSYNC. 1 = SOG. 0 = auto HSYNC source. 1 = manual HSYNC source. 0 = VSYNC. 1 = VSYNC from SOG. 0 = auto HSYNC source. 1 = manual HSYNC source. 0 = Channel 0. 1 = Channel 1. 0 = autochannel select. 1 = manual channel select. 0 = analog interface. 1 = digital interface. 0 = auto-interface select. 1 = manual interface select. |
| 0x12 | Read/Write | [7] [6] [5] [4] | 1***** *0***** **1***** ***0**** | Input HSYNC Polarity HSYNC Polarity Override Input VSYNC Polarity VSYNC Polarity Override | 0 = active low. 1 = active high. 0 = auto HSYNC polarity. 1 = manual HSYNC polarity. 0 = active low. 1 = active high. 0 = auto VSYNC polarity. 1 = manual VSYNC polarity. |
| 0x17 | Read | [3:0] | ****0000 | HSYNCS Per VSYNC MSB | MSB of HSYNCS per VSYNC. |
| 0x18 | Read | [7:0] | 00000000 | HSYNCS Per VSYNC | HSYNCS per VSYNC count. |
| 0x22 | Read/Write | [7:0] | 4 | VSYNC Duration | VSYNC duration. |
| 0x23 | Read/Write | [7:0] | 32 | HSYNC Duration | HSYNC duration. Sets the duration of the output HSYNC in pixel clocks. |
| 0x24 | Read/Write | [7] [6] [5] | 1***** *1***** **1***** | HSYNC Output Polarity VSYNC Output Polarity DE Output Polarity | Output HSYNC polarity. 0 = active low out. 1 = active high out. Output VSYNC polarity. 0 = active low out. 1 = active high out. Output DE polarity. 0 = active low out. 1 = active high out. |

| Hex Address | Read/Write or Read Only | Bits | Default Value | Register Name | Description |
|-------------|-------------------------|-------|---------------|------------------------------|---|
| | | [4] | ***1**** | Field Output Polarity | Output field polarity. 0 = active low out. 1 = active high out. |
| | | [0] | *****0 | Output CLK Invert | 0 = don't invert clock out. 1 = invert clock out. |
| 0x25 | Read/Write | [7:6] | 01***** | Output CLK Select | Selects which clock to use on output pin. 1× CLK is divided down from TMDS clock input when pixel repetition is in use. 00 = ½× CLK. 01 = 1× CLK. 10 = 2× CLK. 11 = 90° phase 1× CLK. |
| | | [5:4] | **11**** | Output Drive Strength | Sets the drive strength of the outputs. 00 = lowest, 11 = highest. |
| | | [3:2] | ****00** | Output Mode | Selects the data output mapping. 00 = 4:4:4 mode (normal). 01 = 4:2:2 + DDR 4:2:2 on blue. 10 = DDR 4:4:4 + DDR 4:2:2 on blue. 11 = 12-bit 4:2:2 (HDMI option only). |
| | | [1] | *****1* | Primary Output Enable | Enables primary output. |
| | | [0] | *****0 | Secondary Output Enable | Enables secondary output (DDR 4:2:2 in Output Mode 1 and Mode 2). |
| 0x26 | Read/Write | [7] | 0***** | Output Three-State | Three-state the outputs. |
| | | [5] | **0***** | SPDIF Three-State | Three-state the S/PDIF output. |
| | | [4] | ***0**** | I ² S Three-State | Three-state the I ² S output and the MCLK out. |
| | | [3] | ***1*** | Power-Down Pin Polarity | Sets polarity of power-down pin. 0 = active low. 1 = active high. |
| | | [2:1] | *****00* | Power-Down Pin Function | Selects the function of the power-down pin. 00 = power-down. 01 = power-down and three-state SOG. 10 = three-state outputs only. 11 = three-state outputs and SOG. |
| | | [0] | *****0 | Power-Down | 0 = normal. 1 = power-down. |
| 0x27 | Read/Write | [7] | 1***** | Auto Power-Down Enable | 0 = disable auto low power state. 1 = enable auto low power state. |
| | | [6] | *0***** | HDCP A0 | Sets the LSB of the address of the HDCP I ² C. Set to 1 only for a second receiver in a dual-link configuration. 0 = use internally generated MCLK. 1 = use external MCLK input. |
| | | [5] | **0***** | MCLK External Enable | If an external MCLK is used, it must be locked to the video clock according to the CTS and N available in the I ² C. Any mismatch between the internal MCLK and the input MCLK results in dropped or repeated audio samples. |
| | | [4] | ***0**** | BT656 EN | Enables EAV/SAV codes to be inserted into the video output data. |
| | | [3] | ***0*** | Force DE Generation | Allows use of the internal DE generator in DVI mode. |

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| Hex Address | Read/Write or Read Only | Bits | Default Value | Register Name | Description |
|-------------|-------------------------|-------|---------------|----------------------------|--|
| | | [2:0] | *****000 | Interlace Offset | Sets the difference (in HSYNCs) in field length between Field 0 and Field 1. |
| 0x28 | Read/Write | [7:2] | 011000** | VS Delay | Sets the delay (in lines) from the VSYNC leading edge to the start of active video. |
| | | [1:0] | *****01 | HS Delay MSB | MSB, Register 0x29. |
| 0x29 | Read/Write | [7:0] | 00000100 | HS Delay | Sets the delay (in pixels) from the HSYNC leading edge to the start of active video. |
| 0x2A | Read/Write | [3:0] | ****0101 | Line Width MSB | MSB, Register 0x2B. |
| 0x2B | Read/Write | [7:0] | 00000000 | Line Width | Sets the width of the active video line in pixels. |
| 0x2C | Read/Write | [3:0] | ****0010 | Screen Height MSB | MSB, Register 0x2D. |
| 0x2D | Read/Write | [7:0] | 11010000 | Screen Height | Sets the height of the active screen in lines. |
| 0x2E | Read/Write | [7] | 0***** | Ctrl EN | Allows Ctrl [3:0] to be output on the I ² S data pins. 00 = I ² S mode. |
| | | [6:5] | *00***** | I ² S Out Mode | 01 = right-justified. 10 = left-justified. 11 = raw IEC60958 mode. |
| | | [4:0] | ***11000 | I ² S Bit Width | Sets the desired bit width for right-justified mode. |
| 0x2F | Read | [6] | *0***** | TMDS Sync Detect | Detects a TMDS DE. |
| | | [5] | **0***** | TMDS Active | Detects a TMDS clock. |
| | | [4] | ***0**** | AV Mute | Gives the status of AV mute based on general control packets. |
| | | [3] | ****0*** | HDCP Keys Read | Returns 1 when read of EEPROM keys is successful. |
| | | [2:0] | *****000 | HDMI Quality | Returns quality number based on DE edges. |
| 0x30 | Read | [6] | *0***** | HDMI Content Encrypted | This bit is high when HDCP decryption is in use (content is protected). The signal goes low when HDCP is not being used. Customers can use this bit to allow copying of the content. The bit should be sampled at regular intervals because it can change on a frame-by-frame basis. |
| | | [5] | **0***** | DVI HSYNC Polarity | Returns DVI HSYNC polarity. |
| | | [4] | ***0**** | DVI VSYNC Polarity | Returns DVI VSYNC polarity. |
| | | [3:0] | ****0000 | HDMI Pixel Repetition | Returns current HDMI pixel repetition amount. 0 = 1x, 1 = 2x, ... The clock and data outputs automatically de-repeat by this value. |
| 0x31 | Read/Write | [7:4] | 1001**** | MV Pulse Max | Sets the maximum pseudo sync pulse width for Macrovision® detection. |
| | | [3:0] | ****0110 | MV Pulse Min | Sets the minimum pseudo sync pulse width for Macrovision detection. |
| 0x32 | Read/Write | [7] | 0***** | MV Oversample En | Tells the Macrovision detection engine whether we are oversampling or not. |
| | | [6] | *0***** | MV Pal En | Tells the Macrovision detection engine to enter PAL mode. |
| | | [5:0] | **001101 | MV Line Count Start | Sets the start line for Macrovision detection. |
| 0x33 | Read/Write | [7] | 1***** | MV Detect Mode | 0 = standard definition. 1 = progressive scan mode. |
| | | [6] | *0***** | MV Settings Override | 0 = use hard-coded settings for line counts and pulse widths. 1 = use I ² C values for these settings. |
| | | [5:0] | **010101 | MV Line Count End | Sets the end line for Macrovision detection. |
| 0x34 | Read/Write | [7:6] | 10***** | MV Pulse Limit Set | Sets the number of pulses required in the last 3 lines (SD mode only). |
| | | [5] | **0***** | Low Freq Mode | Sets audio PLL to low frequency mode. Low frequency mode should only be set for pixel clocks <80 MHz. |

| Hex Address | Read/Write or Read Only | Bits | Default Value | Register Name | Description |
|-------------|-------------------------|-------|---------------|--------------------|--|
| | | [4] | ***0*** | Low Freq Override | Allows the previous bit to be used to set low frequency mode rather than the internal auto-detect. |
| | | [3] | ***0*** | Up Conversion Mode | 0 = repeat Cr and Cb values. 1 = interpolate Cr and Cb values. |
| | | [2] | *****0** | CrCb Filter Enable | Enables the FIR filter for 4:2:2 CrCb output. |
| | | [1] | *****0* | CSC_Enable | Enables the color space converter (CSC). The default settings for the CSC provide HDT-to-RGB conversion. Sets the fixed-point position of the CSC coefficients, including the A4, B4, and C4 offsets. |
| 0x35 | Read/Write | [6:5] | *01* **** | CSC_Mode | 00 = ± 1.0 , -4096 to 4095. 01 = ± 2.0 , -8192 to 8190. 1 \times = ± 4.0 , -16384 to 16380. |
| | | [4:0] | ***01100 | CSC_Coeff_A1 MSB | MSB, Register 0x36. |
| 0x36 | Read/Write | [7:0] | 01010010 | CSC_Coeff_A1 LSB | Color space converter (CSC) coefficient for equation: $R_{OUT} = (A1 \times R_{IN}) + (A2 \times G_{IN}) + (A3 \times B_{IN}) + A4$ $G_{OUT} = (B1 \times R_{IN}) + (B2 \times G_{IN}) + (B3 \times B_{IN}) + B4$ $B_{OUT} = (C1 \times R_{IN}) + (C2 \times G_{IN}) + (C3 \times B_{IN}) + C4$ |
| 0x37 | Read/Write | [4:0] | ***01000 | CSC_Coeff_A2 MSB | MSB, Register 0x38. |
| 0x38 | Read/Write | [7:0] | 00000000 | CSC_Coeff_A2 LSB | CSC coefficient for equation: $R_{OUT} = (A1 \times R_{IN}) + (A2 \times G_{IN}) + (A3 \times B_{IN}) + A4$ $G_{OUT} = (B1 \times R_{IN}) + (B2 \times G_{IN}) + (B3 \times B_{IN}) + B4$ $B_{OUT} = (C1 \times R_{IN}) + (C2 \times G_{IN}) + (C3 \times B_{IN}) + C4$ |
| 0x39 | Read/Write | [4:0] | ***00000 | CSC_Coeff_A3 MSB | MSB, Register 0x3A. |
| 0x3A | Read/Write | [7:0] | 00000000 | CSC_Coeff_A3 LSB | CSC coefficient for equation: $R_{OUT} = (A1 \times R_{IN}) + (A2 \times G_{IN}) + (A3 \times B_{IN}) + A4$ $G_{OUT} = (B1 \times R_{IN}) + (B2 \times G_{IN}) + (B3 \times B_{IN}) + B4$ $B_{OUT} = (C1 \times R_{IN}) + (C2 \times G_{IN}) + (C3 \times B_{IN}) + C4$ |
| 0x3B | Read/Write | [4:0] | ***11001 | CSC_Coeff_A4 MSB | MSB, Register 0x3C. |
| 0x3C | Read/Write | [7:0] | 11010111 | CSC_Coeff_A4 LSB | CSC coefficient for equation: $R_{OUT} = (A1 \times R_{IN}) + (A2 \times G_{IN}) + (A3 \times B_{IN}) + A4$ $G_{OUT} = (B1 \times R_{IN}) + (B2 \times G_{IN}) + (B3 \times B_{IN}) + B4$ $B_{OUT} = (C1 \times R_{IN}) + (C2 \times G_{IN}) + (C3 \times B_{IN}) + C4$ |
| 0x3D | Read/Write | [4:0] | ***11100 | CSC_Coeff_B1 MSB | MSB, Register 0x3E. |
| 0x3E | Read/Write | [7:0] | 01010100 | CSC_Coeff_B1 LSB | CSC coefficient for equation: $R_{OUT} = (A1 \times R_{IN}) + (A2 \times G_{IN}) + (A3 \times B_{IN}) + A4$ $G_{OUT} = (B1 \times R_{IN}) + (B2 \times G_{IN}) + (B3 \times B_{IN}) + B4$ $B_{OUT} = (C1 \times R_{IN}) + (C2 \times G_{IN}) + (C3 \times B_{IN}) + C4$ |
| 0x3F | Read/Write | [4:0] | ***01000 | CSC_Coeff_B2 MSB | MSB, Register 0x40. |
| 0x40 | Read/Write | [7:0] | 00000000 | CSC_Coeff_B2 | CSC coefficient for equation: $R_{OUT} = (A1 \times R_{IN}) + (A2 \times G_{IN}) + (A3 \times B_{IN}) + A4$ $G_{OUT} = (B1 \times R_{IN}) + (B2 \times G_{IN}) + (B3 \times B_{IN}) + B4$ $B_{OUT} = (C1 \times R_{IN}) + (C2 \times G_{IN}) + (C3 \times B_{IN}) + C4$ |
| 0x41 | Read/Write | [4:0] | ***11110 | CSC_Coeff_B3 MSB | MSB, Register 0x42. |
| 0x42 | Read/Write | [7:0] | 10001001 | CSC_Coeff_B3 LSB | Color space converter (CSC) coefficient for equation: $R_{OUT} = (A1 \times R_{IN}) + (A2 \times G_{IN}) + (A3 \times B_{IN}) + A4$ $G_{OUT} = (B1 \times R_{IN}) + (B2 \times G_{IN}) + (B3 \times B_{IN}) + B4$ $B_{OUT} = (C1 \times R_{IN}) + (C2 \times G_{IN}) + (C3 \times B_{IN}) + C4$ |

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| Hex Address | Read/Write or Read Only | Bits | Default Value | Register Name | Description |
|-------------|-------------------------|--|---|--|---|
| 0x43 | Read/Write | [4:0] | ***00010 | CSC_Coeff_B4 MSB | MSB, Register 0x44. |
| 0x44 | Read/Write | [7:0] | 10010010 | CSC_Coeff_B4 LSB | CSC coefficient for equation: $R_{OUT} = (A1 \times R_{IN}) + (A2 \times G_{IN}) + (A3 \times B_{IN}) + A4$ $G_{OUT} = (B1 \times R_{IN}) + (B2 \times G_{IN}) + (B3 \times B_{IN}) + B4$ $B_{OUT} = (C1 \times R_{IN}) + (C2 \times G_{IN}) + (C3 \times B_{IN}) + C4$ |
| 0x45 | Read/Write | [4:0] | ***00000 | CSC_Coeff_C1 MSB | MSB, Register 0x46. |
| 0x46 | Read/Write | [7:0] | 00000000 | CSC_Coeff_C1 LSB | CSC coefficient for equation: $R_{OUT} = (A1 \times R_{IN}) + (A2 \times G_{IN}) + (A3 \times B_{IN}) + A4$ $G_{OUT} = (B1 \times R_{IN}) + (B2 \times G_{IN}) + (B3 \times B_{IN}) + B4$ $B_{OUT} = (C1 \times R_{IN}) + (C2 \times G_{IN}) + (C3 \times B_{IN}) + C4$ |
| 0x47 | Read/Write | [4:0] | ***01000 | CSC_Coeff_C2 MSB | MSB, Register 0x48. |
| 0x48 | Read/Write | [7:0] | 00000000 | CSC_Coeff_C2 LSB | CSC coefficient for equation: $R_{OUT} = (A1 \times R_{IN}) + (A2 \times G_{IN}) + (A3 \times B_{IN}) + A4$ $G_{OUT} = (B1 \times R_{IN}) + (B2 \times G_{IN}) + (B3 \times B_{IN}) + B4$ $B_{OUT} = (C1 \times R_{IN}) + (C2 \times G_{IN}) + (C3 \times B_{IN}) + C4$ |
| 0x49 | Read/Write | [4:0] | ***01110 | CSC_Coeff_C3 MSB | MSB, Register 0x4A. |
| 0x4A | Read/Write | [7:0] | 10000111 | CSC_Coeff_C3 LSB | CSC coefficient for equation: $R_{OUT} = (A1 \times R_{IN}) + (A2 \times G_{IN}) + (A3 \times B_{IN}) + A4$ $G_{OUT} = (B1 \times R_{IN}) + (B2 \times G_{IN}) + (B3 \times B_{IN}) + B4$ $B_{OUT} = (C1 \times R_{IN}) + (C2 \times G_{IN}) + (C3 \times B_{IN}) + C4$ |
| 0x4B | Read/Write | [4:0] | ***11000 | CSC_Coeff_C4 MSB | MSB, Register 0x4C. |
| 0x4C | Read/Write | [7:0] | 10111101 | CSC_Coeff_C4 LSB | CSC coefficient for equation: $R_{OUT} = (A1 \times R_{IN}) + (A2 \times G_{IN}) + (A3 \times B_{IN}) + A4$ $G_{OUT} = (B1 \times R_{IN}) + (B2 \times G_{IN}) + (B3 \times B_{IN}) + B4$ $B_{OUT} = (C1 \times R_{IN}) + (C2 \times G_{IN}) + (C3 \times B_{IN}) + C4$ |
| 0x50 | Read/Write | [7:0] | 00100000 | Test | Must be written to 0x20 for proper operation. |
| 0x56 | Read/Write | [7:0] | 00001111 | Test | Must be written to default of 0x0F for proper operation. |
| 0x57 | Read/Write | [7] [6] [3] [2] | 0***** *0***** ****0*** *****0** | A/V Mute Override AV Mute Value Disable Video Mute Disable Audio Mute | A1 overrides the AV mute value with Bit 6. Sets AV mute value if override is enabled. Disables mute of video during AV mute. Disables mute of audio during AV mute. |
| 0x58 | Read/Write | [7] [6:4] [3] [2:0] | | MCLK PLL Enable MCLK PLL_N N_CTS_Disable MCLK FS_N | MCLK PLL enable—uses analog PLL. MCLK PLL N [2:0]—this controls the division of the MCLK out of the PLL: 0 = /1, 1 = /2, 2 = /3, 3 = /4, etc. Prevents the N/CTS packet on the link from writing to the N and CTS registers. Controls the multiple of 128 F _s , used for MCLK out. 0 = 128 f _s , 1 = 256 f _s , 2 = 384, 7 = 1024 f _s . |
| 0x59 | Read/Write | [6] [5] [4] [2] [1] [0] | | MDA/MCL PU CLKTerm O/R Manual CLKTerm FIFO Reset UF FIFO Reset OF MDA/MCL Three-State | This disables the MDA/MCL pull-ups. Clock termination power-down override: 0 = auto, 1 = manual. Clock termination: 0 = normal, 1 = disconnected. This bit resets the audio FIFO if underflow is detected. This bit resets the audio FIFO if overflow is detected. This bit three-states the MDA/MCL lines. |

| Hex Address | Read/Write or Read Only | Bits | Default Value | Register Name | Description |
|-----------------------------|-------------------------|---|---------------|--|--|
| 0x5A | Read | [6:0] | | Packet Detected | These 7 bits are updated if any specific packet has been received since last reset or loss of clock detect. Normal is 0x00. Bit Data Packet Detected 0 AVI infoframe. 1 Audio infoframe. 2 SPD infoframe. 3 MPEG source infoframe. 4 ACP packets. 5 ISRC1 packets. 6 ISRC2 packets. |
| 0x5B | Read | [3] | | HDMI Mode | 0 = DVI, 1 = HDMI. |
| 0x5E | Read | [7:6] [5:3] 2 1 0 | | Channel Status | Mode = 00. All others are reserved. When Bit 1 = 0 (Linear PCM). 000 = 2 audio channels without pre-emphasis. 001 = 2 audio channels with 50/15 μ s pre-emphasis. 010 = reserved. 011 = reserved. 0 = software for which copyright is asserted. 1 = software for which no copyright is asserted. 0 = audio sample word represents linear PCM samples. 1 = audio sample word used for other purposes. 0 = consumer use of channel status block. |
| Audio Channel Status | | | | | |
| 0x5F | Read | [7:0] | | Channel Status Category Code | |
| 0x60 | Read | [7:4] [3:0] | | Channel Number Source Number | |
| 0x61 | Read | [5:4] [3:0] | | Clock Accuracy Sampling Frequency | Clock accuracy. 00 = Level II. 01 = Level III. 10 = Level I. 11 = reserved. 0011 = 32 kHz 0000 = 44.1 kHz 1000 = 88.2 kHz. 1100 = 176.4 kHz. 0010 = 48 kHz. 1010 = 96 kHz. 1110 = 192 kHz. |

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| Hex Address | Read/Write or Read Only | Bits | Default Value | Register Name | Description |
|----------------------|-------------------------|--|---------------|---|--|
| 0x62 | Read | [3:0] | | Word Length | Word length. 0000 not specified. 0100 = 16 bits. 0011 = 17 bits. 0010 = 18 bits. 0001 = 19 bits. 0101 = 20 bits. 1000 not specified. 1100 = 20 bits. 1011 = 21 bits. 1010 = 22 bits. 1001 = 23 bits. 1101 = 24 bits. |
| 0x7B | Read | [7:0] | | CTS [19:12] | Cycle time stamp—this 20-bit value is used with the N value to regenerate an audio clock. For remaining bits, see Register 0x7C and Register 0x7D. |
| 0x7C | Read | [7:0] | | CTS [11:4] | |
| 0x7D | Read Read | [7:4] [3:0] | | CTS [3:0] N [19:16] | 20-bit N used with CTS to regenerate the audio clock. For remaining bits, see Register 0x7E and Register 0x7F. |
| 0x7E | Read | [7:0] | | N [15:8] | |
| 0x7F | Read | [7:0] | | N [7:0] | |
| AVI Infoframe | | | | | |
| 0x80 | Read | [7:0] | | AVI Infoframe Version | |
| 0x81 | Read | [6:5] 4 [3:2] [1:0] | | Active Format Information Status Bar Information Scan Information | Y [1:0] Indicates RGB, 4:2:2 or 4:4:4. 00 = RGB. 01 = YCbCr 4:2:2. 10 = YCbCr 4:4:4. Active format information present. 0 = no data. 1 = active format information valid. B [1:0]. 00 = no bar information. 01 =horizontal bar information valid. 10 = vertical bar information valid. 11 = horizontal and vertical bar information valid. S [1:0]. 00 = no information. 01 = overscanned (television). 10 = underscanned (computer). |
| 0x82 | Read | [7:6] [5:4] | | Colorimetry Picture Aspect Ratio | C [1:0]. 00 = no data. 01 = SMPTE 170M, ITU601. 10 = ITU709. M [1:0]. 00 = no data. 01 = 4:3. 10 = 16:9. |

| Hex Address | Read/Write or Read Only | Bits | Default Value | Register Name | Description |
|-------------|-------------------------|-------|---------------|----------------------------|--|
| | | [3:0] | | Active Format Aspect Ratio | R [3:0]. 1000 = same as picture aspect ratio. 1001 = 4:3 (center). 1010 = 16:9 (center). 1011 = 14:9 (center). |
| 0x83 | Read | [1:0] | | Nonuniform Picture Scaling | SC [1:0]. 00 = no known nonuniform scaling. 01 = picture has been scaled horizontally. 10 = picture has been scaled vertically. 11 = picture has been scaled horizontally and vertically. |
| 0x84 | Read | [6:0] | | Video Identification Code | VIC [6:0] video identification code—refer to CEA EDID short video descriptors. |
| 0x85 | Read | [3:0] | | Pixel Repeat | PR [3:0]—This specifies how many times a pixel has been repeated. 0000 = no repetition (pixel sent once). 0001 = pixel sent twice (repeated once). 0010 = pixel sent 3 times. 1001 = pixel sent 10 times. 0xA—0xF reserved. |
| 0x86 | Read | [7:0] | | Active Line Start LSB | This represents the line number of the end of the top horizontal bar. If 0, there is no horizontal bar. Combines with Register 0x88 for a 16-bit value. |
| 0x87 | Read | [6:0] | | New Data Flags | New data flags. These 8 bits are updated if any specific data changes. Normal (no NDFs) is 0x00. When any NDF register is read, all bits reset to 0x00. All NDF registers contain the same data. Bit Data Packet Changed 0 AVI infoframe. 1 Audio infoframe. 2 SPD infoframe. 3 MPEG source infoframe. 4 ACP packets. 5 ISRC1 packets. 6 ISRC2 packets. |
| 0x88 | Read | [7:0] | | Active Line Start MSB | Active line start MSB (see Register 0x86). |
| 0x89 | Read | [7:0] | | Active Line End LSB | This represents the line number of the beginning of a lower horizontal bar. If greater than the number of active video lines, there is no lower horizontal bar. Combines with Register 0x8A for a 16-bit value. |
| 0x8A | Read | [7:0] | | Active Line End MSB | Active line end MSB. See Register 0x89. |
| 0x8B | Read | [7:0] | | Active Pixel Start LSB | This represents the last pixel in a vertical pillar bar at the left side of the picture. If 0, there is no left bar. Combines with Register 0x8C for a 16-bit value. |
| 0x8C | Read | [7:0] | | Active Pixel Start MSB | Active pixel start MSB. See Register 0x8B. |
| 0x8D | Read | [7:0] | | Active Pixel End LSB | This represents the first horizontal pixel in a vertical pillar-bar at the right side of the picture. If greater than the maximum number of horizontal pixels, there is no vertical bar. Combines with Register 0x8E for a 16-bit value. |
| 0x8E | Read | [7:0] | | Active Pixel End MSB | Active pixel end MSB. See Register 0x8D. |
| 0x8F | Read | [6:0] | | New Data Flags | New data flags (see 0x87). |

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| Hex Address | Read/Write or Read Only | Bits | Default Value | Register Name | Description |
|-------------|-------------------------|-------|---------------|-----------------------|--|
| 0x90 | Read | [7:0] | | Audio Inframe Version | |
| 0x91 | Read | [7:4] | | Audio Coding Type | CT [3:0]. Audio coding type. 0x00 = refer to stream header. 0x01 = IEC60958 PCM. 0x02 = AC3. 0x03 = MPEG1 (Layer 1 and Layer 2). 0x04 = MP3 (MPEG1 Layer 3). 0x05 = MPEG2 (multichannel). 0x06 = AAC. 0x07 = DTS. 0x08 = ATRAC. |
| | | [2:0] | | Audio Coding Count | CC [2:0]. Audio channel count. 000 = refer to stream header. 001 = 2 channels. 010 = 3 channels. 111 = 8 channels. |
| 0x92 | Read | [4:2] | | Sampling Frequency | SF [2:0]. Sampling frequency. 000 = refer to stream header. 001 = 32 kHz. 010 = 44.1 kHz (CD). 011 = 48 kHz. 100 = 88.2 kHz. 101 = 96 kHz. 110 = 176.4 kHz. 111 = 192 kHz. |
| | | [1:0] | | Sample Size | SS [1:0]. Sample size. 00 = refer to stream header. 01 = 16-bit. 10 = 20-bit. 11 = 24-bit. |
| 0x93 | Read | [7:0] | | Max Bit Rate | Max bit rate (compressed audio only).The value of this field multiplied by 8 kHz represents the maximum bit rate. |
| 0x94 | Read | [7:0] | | Speaker Mapping | CA [7:0]. Speaker mapping or placement for up to 8 channels. See Table 33. |
| 0x95 | Read | 7 | | Down-Mix | DM_INH—down-mix inhibit. 0 = permitted or no information. 1 = prohibited. |
| | | [6:3] | | Level Shift | LSV [3:0]—level shift values with attenuation information. 0000 = 0 dB attenuation. 0001 = 1 dB attenuation. 1111 = 15 dB attenuation. |
| 0x96 | Read | [7:0] | | | Reserved. |
| 0x97 | Read | [6:0] | | New Data Flags | New data flags (see 0x87). |

| Hex Address | Read/Write or Read Only | Bits | Default Value | Register Name | Description |
|--|-------------------------|----------------|---------------|--|---|
| Source Product Description (SPD) Inframe | | | | | |
| 0x98 | Read | [7:0] | | Source Product Description (SPD) Inframe Version | |
| 0x99 | Read | [7:0] | | Vendor Name Character 1 | Vendor name character 1 (VN1) 7-bit ASCII code. The first character in 8 that is the name of the company that appears on the product. |
| 0x9A | Read | [7:0] | | VN2 | VN2. |
| 0x9B | Read | [7:0] | | VN3 | VN3. |
| 0x9C | Read | [7:0] | | VN4 | VN4. |
| 0x9D | Read | [7:0] | | VN5 | VN5. |
| 0x9E | Read | [7:0] | | VN6 | VN6. |
| 0x9F | Read | [6:0] | | New Data Flags | New data flags (see 0x87). |
| 0xA0 | Read | [7:0] | | VN7 | VN7. |
| 0xA1 | Read | [7:0] | | VN8 | VN8. |
| 0xA2 | Read | [7:0] | | Product Description Character 1 | Product Description Character 1 (PD1) 7-bit ASCII code. The first character of 16 that contains the model number and a short description. |
| 0xA3 | Read | [7:0] | | PD2 | PD2. |
| 0xA4 | Read | [7:0] | | PD3 | PD3. |
| 0xA5 | Read | [7:0] | | PD4 | PD4. |
| 0xA6 | Read | [7:0] | | PD5 | PD5. |
| 0xA7 | Read | [7:0] | | New Data Flags | New data flags (see 0x87). |
| 0xA8 | Read | [6:0] | | PD6 | PD6. |
| 0xA9 | Read | [7:0] | | PD7 | PD7. |
| 0xAA | Read | [7:0] | | PD8 | PD8. |
| 0xAB | Read | [7:0] | | PD9 | PD9. |
| 0xAC | Read | [7:0] | | PD10 | PD10. |
| 0xAD | Read | [7:0] | | PD11 | PD11. |
| 0xAE | Read | [7:0] | | PD12 | PD12. |
| 0xAF | Read | [6:0] | | New Data Flags | New data flags (see 0x87). |
| 0xB0 | Read | [7:0] | | PD13 | PD13. |
| 0xB1 | Read | [7:0] | | PD14 | PD14. |
| 0xB2 | Read | [7:0] | | PD15 | PD15. |
| 0xB3 0xB4 | Read Read | [7:0] [7:0] | | PD16 Source Device Information Code | PD16. This is a code that classifies the source device. 0x00 = unknown. 0x01 = digital STB. 0x02 = DVD. 0x03 = D-VHS. 0x04 = HDD video. 0x05 = DVC. 0x06 = DSC. 0x07 = video CD. 0x08 = game. 0x09 = PC general. |
| 0xB7 | Read | [6:0] | | New Data Flags | New data flags (see 0x87). |

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| Hex Address | Read/Write or Read Only | Bits | Default Value | Register Name | Description |
|------------------------------|-------------------------|-------------------------|---------------|--|--|
| MPEG Source Infoframe | | | | | |
| 0xB8 | Read | [7:0] | | MPEG Source Infoframe Version | |
| 0xB9 | Read | [7:0] | | MB[0] | MB [0] (Lower byte of MPEG bit rate: Hz). The lower 8 bits of 32 bits (4 bytes) that specify the MPEG bit rate in Hz. |
| 0xBA | Read | [7:0] | | MB[1] | MB [1]. |
| 0xBB | Read | [7:0] | | MB[2] | MB [2]. |
| 0xBC | Read | [7:0] 4 | | Field Repeat | MB [3] (upper byte). FR—New field or repeated field. 0 = New field or picture. 1 = Repeated field. |
| 0xBD | Read | [1:0] | | MPEG Frame | MF [1:0] This identifies whether frame is an I, B, or P picture. 00 = unknown. 01 = I picture. 10 = B picture. 11 = P picture. |
| 0xBE | Read | [7:0] | | | Reserved. |
| 0xBF | Read | [6:0] | | New Data Flags | New data flags (see 0x87). |
| 0xC0 | Read | [7:0] | | Audio Content Protection Packet (ACP) Type | Audio content protection packet (ACP) type. 0x00 = generic audio. 0x01 = IEC 60958-identified audio. 0x02 = DVD-audio. 0x03 = reserved for super audio CD (SACD). 0x04 = 0xFF reserved. |
| 0xC1 | Read | [7:0] | | ACP Packet Byte 0 | ACP Packet Byte 0 (ACP_PB0). |
| 0xC2 | Read | [7:0] | | ACP_PB1 | ACP_PB1. |
| 0xC3 | Read | [7:0] | | ACP_PB2 | ACP_PB2. |
| 0xC4 | Read | [7:0] | | ACP_PB3 | ACP_PB3. |
| 0xC5 | Read | [7:0] | | ACP_PB4 | ACP_PB4. |
| 0xC6 | Read | [7:0] | | ACP_PB5 | ACP_PB5. |
| 0xC7 | Read | [6:0] | | NDF | New data flags (see 0x87). |
| 0xC8 | Read | 7 6 [2:0] | | ISRC1 Continued ISRC1 Valid ISRC1 Status | International standard recording code (ISRC1) continued. This indicates an ISRC2 packet is being transmitted. 0 = ISRC1 status bits and PBs not valid. 1 = ISRC1 status bits and PBs valid. 001 = starting position. 010 = intermediate position. 100 = final position. |
| 0xC9 | Read | [7:0] | | ISRC1 Packet Byte 0 | ISRC1 Packet Byte 0 (ISRC1_PB0). |
| 0xCA | Read | [7:0] | | ISRC1_PB1 | ISRC1_PB1. |
| 0xCB | Read | [7:0] | | ISRC1_PB2 | ISRC1_PB2. |
| 0xCC | Read | [7:0] | | ISRC1_PB3 | ISRC1_PB3. |
| 0xCD | Read | [7:0] | | ISRC1_PB4 | ISRC1_PB4. |
| 0xCE | Read | [7:0] | | ISRC1_PB5 | ISRC1_PB5. |
| 0xCF | Read | [6:0] | | NDF | New data flags (see 0x87). |
| 0xD0 | Read | [7:0] | | ISRC1_PB6 | ISRC1_PB6. |
| 0xD1 | Read | [7:0] | | ISRC1_PB7 | ISRC1_PB7. |

| Hex Address | Read/Write or Read Only | Bits | Default Value | Register Name | Description |
|-------------|-------------------------|-------|---------------|---------------------|---|
| 0xD2 | Read | [7:0] | | ISRC1_PB8 | ISRC1_PB8. |
| 0xD3 | Read | [7:0] | | ISRC1_PB9 | ISRC1_PB9. |
| 0xD4 | Read | [7:0] | | ISRC1_PB10 | ISRC1_PB10. |
| 0xD5 | Read | [7:0] | | ISRC1_PB11 | ISRC1_PB11. |
| 0xD6 | Read | [7:0] | | ISRC1_PB12 | ISRC1_PB12. |
| 0xD7 | Read | [6:0] | | NDF | New data flags (see 0x87). |
| 0xD8 | Read | [7:0] | | ISRC1_PB13 | ISRC1_PB13. |
| 0xD9 | Read | [7:0] | | ISRC1_PB14 | ISRC1_PB14. |
| 0xDA | Read | [7:0] | | ISRC1_PB15 | ISRC1_PB15. |
| 0xDB | Read | [7:0] | | ISRC1_PB16 | ISRC1_PB16. |
| 0xDC | Read | [7:0] | | ISRC2 Packet Byte 0 | ISRC2 Packet Byte 0 (ISRC2_PB0). This is transmitted only when the ISRC_ continue bit (Register 0xC8, Bit 7) is set to 1. |
| 0xDD | Read | [7:0] | | ISRC2_PB1 | ISRC2_PB1. |
| 0xDE | Read | [7:0] | | ISRC2_PB2 | ISRC2_PB2. |
| 0xDF | Read | [6:0] | | New Data Flags | New data flags (see 0x87). |
| 0xE0 | Read | [7:0] | | ISRC2_PB3 | ISRC2_PB3. |
| 0xE1 | Read | [7:0] | | ISRC2_PB4 | ISRC2_PB4. |
| 0xE2 | Read | [7:0] | | ISRC2_PB5 | ISRC2_PB5. |
| 0xE3 | Read | [7:0] | | ISRC2_PB6 | ISRC2_PB6. |
| 0xE4 | Read | [7:0] | | ISRC2_PB7 | ISRC2_PB7. |
| 0xE5 | Read | [7:0] | | ISRC2_PB8 | ISRC2_PB8. |
| 0xE6 | Read | [7:0] | | ISRC2_PB9 | ISRC2_PB9. |
| 0xE7 | Read | [6:0] | | New Data Flags | New data flags (see 0x87). |
| 0xE8 | Read | [7:0] | | ISRC2_PB10 | ISRC2_PB10. |
| 0xE9 | Read | [7:0] | | ISRC2_PB11 | ISRC2_PB11. |
| 0xEA | Read | [7:0] | | ISRC2_PB12 | ISRC2_PB12. |
| 0xEB | Read | [7:0] | | ISRC2_PB13 | ISRC2_PB13. |
| 0xEC | Read | [7:0] | | ISRC2_PB14 | ISRC2_PB14. |
| 0xED | Read | [7:0] | | ISRC2_PB15 | ISRC2_PB15. |
| 0xEE | Read | [7:0] | | ISRC2_PB16 | ISRC2_PB16. |

2-WIRE SERIAL CONTROL REGISTER DETAILS

CHIP IDENTIFICATION

0x00—Bits[7:0] Chip Revision

An 8-bit value that reflects the current chip revision.

0x11—Bit[7] HSYNC Source

0 = HSYNC, 1 = SOG. The power-up default is 0. These selections are ignored if Register 0x11, Bit 6 = 0.

0x11—Bit[6] HSYNC Source Override

0 = auto HSYNC source, 1 = manual HSYNC source. Manual HSYNC source is defined in Register 0x11, Bit 7. The power-up default is 0.

0x11—Bit[5] VSYNC Source

0 = VSYNC, 1 = VSYNC from SOG. The power-up default is 0. These selections are ignored if Register 0x11, Bit 4 = 0.

0x11—Bit[4] VSYNC Source Override

0 = auto VSYNC source, 1 = manual VSYNC source. Manual VSYNC source is defined in Register 0x11, Bit 5. The power-up default is 0.

0x11—Bit[3] Channel Select

0 = Channel 0, 1 = Channel 1. The power-up default is 0. These selections are ignored if Register 0x11, Bit 2 = 0.

0x11—Bit[2] Channel Select Override

0 = auto channel select, 1 = manual channel select. Manual channel select is defined in Register 0x11, Bit 3. The power-up default is 0.

0x11—Bit[1] Interface Select

0 = analog interface, 1 = digital interface. The power-up default is 0. These selections are ignored if Register 0x11, Bit 0 = 0.

0x11—Bit[0] Interface Select Override

0 = auto interface select, 1 = manual interface select. Manual interface select is defined in Register 0x11, Bit 1. The power-up default is 0.

0x12—Bit[7] Input HSYNC Polarity

0 = active low, 1 = active high. The power-up default is 1. These selections are ignored if Register 10x2, Bit 6 = 0.

0x12—Bit[6] HSYNC Polarity Override

0 = auto HSYNC polarity, 1 = manual HSYNC polarity. Manual HSYNC polarity is defined in Register 0x11, Bit 7. The power-up default is 0.

0x12—Bit[5] Input VSYNC Polarity

0 = active low, 1 = active high. The power-up default is 1. These selections are ignored if Register 0x11, Bit 4 = 0.

0x12—Bit[4] VSYNC Polarity Override

0 = auto VSYNC polarity, 1 = manual VSYNC polarity. Manual VSYNC polarity is defined in Register 0x11, Bit 5. The power-up default is 0.

0x17—Bits[3:0] HSYNCs per VSYNC MSBs

The 4 MSBs of the 12-bit counter that reports the number of HSYNCs/VSYNC on the active input. This is useful in determining the mode and an aid in setting the PLL divide ratio.

0x18—Bits[7:0] HSYNCs per VSYNC LSBs

The 8 LSBs of the 12-bit counter that reports the number of HSYNCs/VSYNC on the active input.

0x21—Bit[5] VSYNC Filter Enable

The purpose of the VSYNC filter is to guarantee the position of the VSYNC edge with respect to the HSYNC edge and to generate a field signal. The filter works by examining the placement of VSYNC and regenerating a correctly placed VSYNC one line later. The VSYNC is first checked to see whether it occurs in the Field 0 position or the Field 1 position. This is done by checking the leading edge position against the sync separator threshold and the HSYNC position. The HSYNC width is divided into four quadrants with Quadrant 1 starting at the HSYNC leading edge plus a sync separator threshold. If the VSYNC leading edge occurs in Quadrant 1 or Quadrant 4, the field is set to 0 and the output VSYNC is placed coincident with the HSYNC leading edge. If the VSYNC leading edge occurs in Quadrant 2 or Quadrant 3, the field is set to 1 and the output VSYNC leading edge is placed in the center of the line. In this way, the VSYNC filter creates a predictable relative position between HSYNC and VSYNC edges at the output.

If the VSYNC occurs near the HSYNC edge, this guarantees that the VSYNC edge follows the HSYNC edge. This performs filtering also in that it requires a minimum of 64 lines between VSYNCs. The VSYNC filter cleans up extraneous pulses that might occur on the VSYNC. This should be enabled whenever the HSYNC/VSYNC count is used. Setting this bit to 0 disables the VSYNC filter. Setting this bit to 1 enables the VSYNC filter. Power-up default is 0.

0x21—Bit[4] VSYNC Duration Enable

This enables the VSYNC duration block that is designed to be used with the VSYNC filter. Setting the bit to 0 leaves the VSYNC output duration unchanged; setting the bit to 1 sets the VSYNC output duration based on Register 0x22. The power-up default is 0.

0x22—Bits[7:0] VSYNC Duration

This is used to set the output duration of the VSYNC, and is designed to be used with the VSYNC filter. This is valid only if Register 0x21, Bit 4 is set to 1. Power-up default is 4.

0x23—Bits[7:0] HSYNC Duration

An 8-bit register that sets the duration of the HSYNC output pulse. The leading edge of the HSYNC output is triggered by the internally generated, phase-adjusted PLL feedback clock. The AD9381 then counts a number of pixel clocks equal to the value in this register. This triggers the trailing edge of the HSYNC output, which is also phase-adjusted. The power-up default is 32.

0x24—Bit[7] HSYNC Output Polarity

This bit sets the polarity of the HSYNC output. Setting this bit to 0 sets the HSYNC output to active low. Setting this bit to 1 sets the HSYNC output to active high. Power-up default setting is 1.

0x24—Bit[6] VSYNC Output Polarity

This bit sets the polarity of the VSYNC output (both DVI and analog). Setting this bit to 0 sets the VSYNC output to active low. Setting this bit to 1 sets the VSYNC output to active high. Power-up default is 1.

0x24—Bit[5] Display Enable Output Polarity

This bit sets the polarity of the display enable (DE) for both DVI and analog. 0 = DE output polarity is negative. 1 = DE output polarity is positive.

The power-up default is 1.

0x24—Bit[4] Field Output Polarity

This bit sets the polarity (both DVI and analog) of the field output signal on Pin 21. 0 = active low out. 1 = active high out. The power-up default is 1.

0x24—Bit[0] Output Clock Invert

This bit allows inversion of the output clock as specified by Register 0x25, Bits 7 to 6. 0 = noninverted clock. 1 = inverted clock. The power-up default setting is 0.

0x25—Bits[7:6] Output Clock Select

These bits select the clock output on the DATACLK pin. They include 1/2× clock, a 2× clock, a 90° phase shifted clock or the normal pixel clock. The power-up default setting is 01.

Table 12. Output Clock Select

| Select | Result |
|--------|--------------------------|
| 00 | 1/2× pixel clock |
| 01 | 1× pixel clock |
| 10 | 2× pixel clock |
| 11 | 90° phase 1× pixel clock |

0x25—Bits[5:4] Output Drive Strength

These two bits select the drive strength for all the high speed digital outputs (except VSOUT, A0 and O/E field). Higher drive strength results in faster rise/fall times and in general makes it easier to capture data. Lower drive strength results in slower rise/fall times and helps to reduce EMI and digitally generated power supply noise. The power-up default setting is 11.

Table 13. Output Drive Strength

| Output Drive | Result |
|--------------|-----------------------------------|
| 00 | Low output drive strength |
| 01 | Medium low output drive strength |
| 10 | Medium high output drive strength |
| 11 | High output drive strength |

0x25—Bits[3:2] Output Mode

These bits choose between four options for the output mode, one of which is exclusive to an HDMI input. 4:4:4 mode is standard RGB; 4:2:2 mode is YCrCb, which reduces the number of active output pins from 24 to 16; 4:4:4 is double data rate (DDR) output mode; and the data is RGB mode that changes on every clock edge. The power-up default setting is 00.

Table 14. Output Mode

| Output Mode | Result |
|-------------|---|
| 00 | 4:4:4 RGB mode |
| 01 | 4:2:2 YCrCb mode + DDR 4:2:2 on blue (secondary) |
| 10 | DDR 4:4:4: DDR mode + DDR 4:2:2 on blue (secondary) |
| 11 | 12-bit 4:2:2 (HDMI option only) |

0x25—Bit[1] Primary Output Enable

This bit places the primary output in active or high impedance mode. The primary output is designated when using either 4:2:2 or DDR 4:4:4. In these modes, the data on the red and green output channels is the primary output, while the output data on the blue channel (DDR YCrCb) is the secondary output. 0 = primary output is in high impedance mode. 1 = primary output is enabled. The power-up default setting is 1.

0x25—Bit[0] Secondary Output Enable

This bit places the secondary output in active or high impedance mode. The secondary output is designated when using either 4:2:2 or DDR 4:4:4. In these modes, the data on the blue output channel is the secondary output while the output data on the red and green channels is the primary output. Secondary output is always a DDR YCrCb data mode. The power-up default setting is 0. 0 = secondary output is in high impedance mode. 1 = secondary output is enabled.

0x26—Bit[7] Output Three-State

When enabled, this bit puts all outputs (except SOGOUT) in a high impedance state. 0 = normal outputs. 1 = all outputs (except SOGOUT) in high impedance mode. The power-up default setting is 0.

0x26—Bit[5] S/PDIF Three-State

When enabled, this bit places the S/PDIF audio output pins in a high impedance state. 0 = normal S/PDIF output. 1 = S/PDIF pins in high impedance mode. The power-up default setting is 0.

0x26—Bit[4] I²S Three-State

When enabled, this bit places the I²S output pins in a high impedance state. 0 = normal I²S output. 1 = I²S pins in high impedance mode. The power-up default setting is 0.

0x26—Bit[3] Power-Down Polarity

This bit defines the polarity of the input power-down pin. 0 = power-down pin is active low. 1 = power-down pin is active high. The power-up default setting is 1.

0x26—Bits[2-1] Power-Down Pin Function

These bits define the different operational modes of the power-down pin. These bits are functional only when the power-down pin is active; when it is not active, the part is powered up and functioning. 0 = chip is powered down and all outputs are in high impedance mode. 1 = chip remains powered up, but all outputs are in high impedance mode. The power-up default setting is 00.

0x26—Bit[0] Power-Down

This bit is used to put the chip in power-down mode. In this mode, the power dissipation is reduced to a fraction of the typical power (see Table 1 for exact power dissipation). When in power-down, the HSOUT, VSOUT, DATAACK, and all 30 of the data outputs are put into a high impedance state. Note that the SOGOUT output is not put into high impedance. Circuit blocks that continue to be active during power-down include the voltage references, sync processing, sync detection, and the serial register. These blocks facilitate a fast start-up from power-down. 0 = normal operation. 1 = power-down. The power-up default setting is 0.

0x27—Bit[7] Auto Power-Down Enable

This bit enables the chip to go into low power mode, or seek mode if no sync inputs are detected. 0 = auto power-down disabled. 1 = chip powers down if no sync inputs present. The power-up default setting is 1.

0x27—Bit[6] HDCP A0 Address

This bit sets the LSB of the address of the HDCP I²C. This should be set to 1 only for a second receiver in a dual-link configuration. The power-up default is 0.

0x27—Bit[5] MCLK External Enable

This bit enables the MCLK to be supplied externally. If an external MCLK is used, then it must be locked to the video clock according to the CTS and N available in the I²C. Any mismatch between the internal MCLK and the input MCLK results in dropped or repeated audio samples. 0 = use internally generated MCLK. 1 = use external MCLK input. The power-up default setting is 0.

BT656 GENERATION**0x27—Bit[4] BT656 Enable**

This bit enables the output to be BT656 compatible with the defined start of active video (SAV) and the end of active video (EAV) controls to be inserted. These require specification of the number of active lines, active pixels per line, and delays to place these markers. 0 = disable BT656 video mode. 1 = enable BT656 video mode. The power-up default setting is 0.

0x27—Bit[3] Force DE Generation

This bit allows the use of the internal DE generator in DVI mode. 0 = internal DE generation disabled. 1 = force DE generation via programmed registers. The power-up default setting is 0.

0x27—Bits[2:0] Interlace Offset

These bits define the offset in HSYNCs from Field 0 to Field 1. The power-up default setting is 000.

0x28—Bits[7:2] VSYNC Delay

These bits set the delay (in lines) from the leading edge of VSYNC to active video. The power-up default setting is 24.

0x28—Bits[1:0] HSYNC Delay MSBs

Along with register 0x29, these ten bits set the delay (in pixels) from the HSYNC leading edge to the start of active video. The power-up default setting is 0x104.

0x29—Bits[7:0] HSYNC Delay LSBs

See the HSYNC Delay MSBs section.

0x2A—Bits[3:0] Line Width MSBs

Along with register 0x2B, these 12 bits set the width of the active video line (in pixels). The power-up default setting is 0x500.

0x2B—Bits[7:0] Line Width LSBs

See the line width MSBs section.

0x2C—Bits[3:0] Screen Height MSBs

Along with register 0x2D, these 12 bits, set the height of the active screen (in lines). The power-up default setting is 0x2D0.

0x2D—Bits[7:0] Screen Height LSBs

See the Screen Height MSBs section.

0x2E—Bit[7] Ctrl Enable

When set, this bit allows Ctrl [3:0] signals decoded from the DVI to be output on the I²S data pins. 0 = I²S signals on I²S lines. 1 = Ctrl [3:0] output on I²S lines. The power-up default setting is 0.

0x2E—Bits[6:5] I²S Output Mode

These bits select between four options for the I²S output: I²S, right-justified, left-justified, or raw IEC60958 mode. The power-up default setting is 00.

Table 15. I²S Output Select

| I ² S Output Mode | Result |
|------------------------------|-----------------------|
| 00 | I ² S mode |
| 01 | Right-justified |
| 10 | Left-justified |
| 11 | Raw IEC60958 mode |

0x2E—Bits[4:0] I²S Bit Width

These bits set the I²S bit width for right-justified mode. The power-up default setting is 24 bits.

0x2F—Bit[6] TMDS Sync Detect

This read-only bit indicates the presence of a TMDS DE. 0 = no TMDS DE present. 1 = TMDS DE detected.

0x2F—Bit[5] TMDS Active

This read-only bit indicates the presence of a TMDS clock. 0 = no TMDS clock present. 1 = TMDS clock detected.

0x2F—Bit[4] AV Mute

This read-only bit indicates the presence of AV mute based on general control packets. 0 = AV not muted. 1 = AV muted.

0x2F—Bit[3] HDCP Keys Read

This read-only bit reports if the HDCP keys were read successfully. 0 = failure to read HDCP keys. 1 = HDCP keys read.

0x2F—Bits[2:0] HDMI Quality

These read-only bits indicate a level of HDMI quality based on the DE (display enable) edges. A larger number indicates a higher quality.

0x30—Bit[6] HDMI Content Encrypted

This read-only bit is high when HDCP decryption is in use (content is protected). The signal goes low when HDCP is not being used. Customers can use this bit to determine whether or not to allow copying of the content. The bit should be sampled at regular intervals since it can change on a frame by frame basis. 0 = HDCP not in use. 1 = HDCP decryption in use.

0x30—Bit[5] DVI HSYNC Polarity

This read-only bit indicates the polarity of the DVI HSYNC. 0 = DVI HSYNC polarity is low active. 1 = DVI HSYNC polarity is high active.

0x30—Bit[4] DVI VSYNC Polarity

This read-only bit indicates the polarity of the DVI VSYNC. 0 = DVI VSYNC polarity is low active. 1 = DVI VSYNC polarity is high active.

0x30—Bits[3:0] HDMI Pixel Repetition

These read-only bits indicate the pixel repetition on DVI. 0 = 1×, 1 = 2×, 2 = 3×, up to a maximum repetition of 10× (0x9).

Table 16.

| Select | Repetition Multiplier |
|--------|-----------------------|
| 0000 | 1× |
| 0001 | 2× |
| 0010 | 3× |
| 0011 | 4× |
| 0100 | 5× |
| 0101 | 6× |
| 0110 | 7× |
| 0111 | 8× |
| 1000 | 9× |
| 1001 | 10× |

MACROVISION®**0x31—Bits[7:4] Macrovision Pulse Max**

These bits set the pseudo sync pulse width maximum for Macrovision detection in pixel clocks. This is functional for 13.5 MHz SDTV or 27 MHz progressive scan. Power-up default is 9.

0x31—Bits[3:0] Macrovision Pulse Min

These bits set the pseudo sync pulse width minimum for Macrovision detection in pixel clocks. This is functional for 13.5 MHz SDTV or 27 MHz progressive scan. Power-up default is 6.

0x32—Bit[7] Macrovision Oversample Enable

Tells the Macrovision detection engine whether oversampling is used. This accommodates 27 MHz sampling for SDTV and 54 MHz sampling for progressive scan and is used as a correction factor for clock counts. Power-up default is 0.

0x32—Bit[6] Macrovision PAL Enable

Tells the Macrovision detection engine to enter PAL mode when set to 1. Default is 0 for NTSC mode.

0x32—Bits[5:0] Macrovision Line Count Start

Set the start line for Macrovision detection. Along with Register 0x33, Bits [5:0], they define the region where MV pulses are expected to occur. The power-up default is Line 13.

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0x33—Bit[7] Macrovision Detect Mode

0 = standard definition. 1 = progressive scan mode.

0x33—Bit[6] Macrovision Settings Override

This defines whether preset values are used for the MV line counts and pulse widths or the values stored in I²C registers. 0 = use hard-coded settings for line counts and pulse widths. 1 = use I²C values for these settings.

0x33—Bits[5:0] Macrovision Line Count End

Set the end line for Macrovision detection. Along with Register 0x32, Bits [5:0], they define the region where MV pulses are expected to occur. The power-up default is Line 21.

0x34—Bits[7:6] Macrovision Pulse Limit Select

Set the number of pulses required in the last three lines (SD mode only). If there is not at least this number of MV pulses, the engine stops. These 2 bits define these pulse counts:

- 00 = 6
- 01 = 4
- 10 = 5 (default)
- 11 = 7

0x34—Bit[5] Low Frequency Mode

Sets the audio PLL to low frequency mode. Low frequency mode should only be set for pixel clocks < 80 MHz.

0x34—Bit[4] Low Frequency Override

Allows the previous bit to be used to set low frequency mode rather than the internal auto-detect.

0x34—Bit[3] Up Conversion Mode

0 = repeat Cb/Cr values. 1 = interpolate Cb/Cr values.

0x34—Bit[2] CbCr Filter Enable

Enables the FIR filter for 4:2:2 CbCr output.

COLOR SPACE CONVERSION

The default power-up values for the color space converter coefficients (R0x35 through R0x4C) are set for ATSC RGB-to-YCbCr conversion. They are completely programmable for other conversions.

0x34—Bit[1] Color Space Converter Enable

This bit enables the color space converter. 0 = disable color space converter. 1 = enable color space converter. The power-up default setting is 0.

0x35—Bits[6:5] Color Space Converter Mode

These two bits set the fixed point position of the CSC coefficients, including the A4, B4, and C4 offsets.

Table 17. CSC Fixed Point Converter Mode

| Select | Result |
|--------|------------------------|
| 00 | ±1.0, -4096 to +4095 |
| 01 | ±2.0, -8192 to +8190 |
| 1x | ±4.0, -16384 to +16380 |

0x35—Bits[4:0] Color Space Conversion Coefficient A1 MSBs

These 5 bits form the 5 MSBs of the Color Space Conversion Coefficient A1. This, combined with the 8 LSBs of the following register, form a 13-bit, two's complement coefficient which is user programmable. The equation takes the form of:

$$\begin{aligned}R_{OUT} &= (A1 \times R_{IN}) + (A2 \times G_{IN}) + (A3 \times B_{IN}) + A4 \\G_{OUT} &= (B1 \times R_{IN}) + (B2 \times G_{IN}) + (B3 \times B_{IN}) + B4 \\B_{OUT} &= (C1 \times R_{IN}) + (C2 \times G_{IN}) + (C3 \times B_{IN}) + C4\end{aligned}$$

The default value for the 13-bit, A1 coefficient is 0x0C52.

0x36—Bits[7:0] Color Space Conversion Coefficient A1 LSBs

See the Register 0x35 section.

0x37—Bits[4:0] CSC A2 MSBs

These five bits form the 5 MSBs of the Color Space Conversion Coefficient A2. Combined with the 8 LSBs of the following register, they form a 13-bit, two's complement coefficient that is user programmable. The equation takes the form of:

$$\begin{aligned}R_{OUT} &= (A1 \times R_{IN}) + (A2 \times G_{IN}) + (A3 \times B_{IN}) + A4 \\G_{OUT} &= (B1 \times R_{IN}) + (B2 \times G_{IN}) + (B3 \times B_{IN}) + B4 \\B_{OUT} &= (C1 \times R_{IN}) + (C2 \times G_{IN}) + (C3 \times B_{IN}) + C4\end{aligned}$$

The default value for the 13-bit, A2 coefficient is 0x0800.

0x38—Bits[7:0] CSC A2 LSBs

See the Register 0x37 section.

0x39—Bits[4:0] CSC A3 MSBs

The default value for the 13-bit A3 is 0x0000.

0x3A—Bits[7:0] CSC A3 LSBs

0x3B—Bits[4:0] CSC A4 MSBs

The default value for the 13-bit A4 is 0x19D7.

0x3C—Bits[7:0] CSC A4 LSBs

0x3D—Bits[4:0] CSC B1 MSBs

The default value for the 13-bit B1 is 0x1C54.

0x3E—Bits[7:0] CSC B1 LSBs

0x3F—Bits[4:0] CSC B2 MSB

The default value for the 13-bit B2 is 0x0800.

0x40—Bits[7:0] CSC B2 LSBs**0x41—Bits[4:0] CSC B3 MSBs**

The default value for the 13-bit B3 is 0x1E89.

0x42—Bits[7:0] CSC B3 LSBs**0x43—Bits[4:0] CSC B4 MSBs**

The default value for the 13-bit B4 is 0x0291.

0x44—Bits[7:0] CSC B4 LSBs**0x45—Bits[4:0] CSC C1 MSBs**

The default value for the 13-bit C1 is 0x0000.

0x46—Bits[7:0] CSC C1 LSBs**0x47—Bits[4:0] CSC C2 MSBs**

The default value for the 13-bit C2 is 0x0800.

0x48—Bits[7:0] CSC C2 LSBs**0x49—Bits[4:0] CSC C3 MSBs**

The default value for the 13-bit C3 is 0x0E87.

0x4A—Bits[7:0] CSC C3 LSBs**0x4B—Bits[4:0] CSC C4 MSBs**

The default value for the 13-bit C4 is 0x18BD.

0x4C—Bits[7:0] CSC C4 LSBs**0x57—Bit[7] AV Mute Override****0x57—Bit[6] AV Mute Value****0x57—Bit[3] Disable AV Mute****0x57—Bit[2] Disable Audio Mute****0x58—Bit[7] MCLK PLL Enable**

This bit enables the use of the analog PLL.

0x58—Bits[6:4] MCLK PLL_N

These bits control the division of the MCLK out of the PLL.

Table 18.

| PLL_N [2:0] | MCLK Divide Value |
|-------------|-------------------|
| 0 | /1 |
| 1 | /2 |
| 2 | /3 |
| 3 | /4 |
| 4 | /5 |
| 5 | /6 |
| 6 | /7 |
| 7 | /8 |

0x58—Bit[3] N_CTS_Disable

This bit makes it possible to prevent the N/CTS packet on the link from writing to the N and CTS registers.

0x58—Bits[2:0] MCLK f_s_N

These bits control the multiple of 128 f_s used for MCLK out.

Table 19.

| MCLK f _s _N [2:0] | f _s Multiple |
|------------------------------|-------------------------|
| 0 | 128 |
| 1 | 256 |
| 2 | 384 |
| 3 | 512 |
| 4 | 640 |
| 5 | 768 |
| 6 | 896 |
| 7 | 1024 |

0x59—Bit[6] MDA/MCL PU Disable

This bit disables the inter-MDA/MCL pull-ups.

0x59—Bit[5] CLK Term O/R

This bit allows for overriding during power down.

0 = auto, 1 = manual.

0x59—Bit[4] Manual CLK Term

This bit allows normal clock termination or disconnects this.

0 = normal, 1 = disconnected.

0x59—Bit[2] FIFO Reset UF

This bit resets the audio FIFO if underflow is detected.

0x59—Bit[1] FIFO Reset OF

This bit resets the audio FIFO if overflow is detected.

0x59—Bit[0] MDA/MCL Three-State

This bit three-states the MDA/MCL lines to allow in-circuit programming of the EEPROM.

0x5A—Bits[6:0] Packet Detect

This register indicates if a data packet in specific sections has been detected. These seven bits are updated if any specific packet has been received since last reset or loss of clock detect. Normal is 0x00.

Table 20.

| Packet Detect Bit | Packet Detected |
|-------------------|-----------------------|
| 0 | AVI infoframe |
| 1 | Audio infoframe |
| 2 | SPD infoframe |
| 3 | MPEG source infoframe |
| 4 | ACP packets |
| 5 | ISRC1 packets |
| 6 | ISRC2 packets |

0x5B—Bit[3] HDMI Mode

0 = DVI, 1 = HDMI.

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0x5E—Bits[7:6] Channel Status Mode

0x5E—Bits[5:3] PCM Audio Data

0x5E—Bit[2] Copyright Information

0x5E—Bit[1] Linear PCM Identification

0x5E—Bit[0] Use of Channel Status Block

0x5F—Bits[7:0] Channel Status Category Code

0x60—Bits[7:4] Channel Number

0x60—Bits[3:0] Source Number

0x61—Bits[5:4] Clock Accuracy

0x61—Bits[3:0] Sampling Frequency

Table 21.

| Code | Frequency (kHz) |
|------|-----------------|
| 0x0 | 44.1 |
| 0x2 | 48 |
| 0x3 | 32 |
| 0x8 | 88.2 |
| 0xA | 96 |
| 0xC | 176.4 |
| 0xE | 192 |

0x62—Bits[3:0] Word Length

0x7B—Bits[7:0] CTS (Cycle Time Stamp) (19:12)

These are the most significant 8 bits of a 20-bit word used in the 20-bit N term in the regeneration of the audio clock.

0x7C—Bits[7:0] CTS (11:4)

0x7D—Bits[7:4] CTS (3:0)

0x7D—Bits[3:0] N (19:16)

These are the most significant 4 bits of a 20-bit word used along with the 20-bit CTS term to regenerate the audio clock.

0x80 AVI Inframe Version

0x81—Bits[6:5] Y [1:0]

This register indicates whether data is RGB, 4:4:4, or 4:2:2.

Table 22.

| Y | Video Data |
|----|-------------|
| 00 | RGB |
| 01 | YCbCr 4:2:2 |
| 10 | YCbCr 4:4:4 |

0x81—Bit[4] Active Format Information Present

0 = no data. 1 = active format information valid.

0x81—Bits[3:2] Bar Information

Table 23.

| B | Bar Type |
|----|---|
| 00 | No bar information |
| 01 | Horizontal bar information valid |
| 10 | Vertical bar information valid |
| 11 | Horizontal and vertical bar information valid |

0x81—Bits[1:0] Scan Information

Table 24.

| S [1:0] | Scan Type |
|---------|--------------------------|
| 00 | No information |
| 01 | Overscanned (television) |
| 10 | Underscanned (computer) |

0x82—Bits[7:6] Colorimetry

Table 25.

| C [1:0] | Colorimetry |
|---------|--------------------|
| 00 | No data |
| 01 | SMPTE 170M, ITU601 |
| 10 | ITU 709 |

0x82—Bits[5:4] Picture Aspect Ratio

Table 26.

| M [1:0] | Aspect Ratio |
|---------|--------------|
| 00 | No data |
| 01 | 4:3 |
| 10 | 16:9 |

0x82—Bits[3:0] Active Format Aspect Ratio

Table 27.

| R [3:0] | Active Format A/R |
|---------|--|
| 0x8 | Same as picture aspect ratio (M [1:0]) |
| 0x9 | 4:3 (center) |
| 0xA | 16:9 (center) |
| 0xB | 14:9 (center) |

0x83—Bits[1:0] Nonuniform Picture Scaling

Table 28.

| SC [1:0] | Picture Scaling |
|----------|--|
| 00 | No known nonuniform scaling |
| 01 | Has been scaled horizontally |
| 10 | Has been scaled vertically |
| 11 | Has been scaled both horizontally and vertically |

0x84—Bits[6:0] Video ID Code

See CEA EDID short video descriptors.

0x85—Bits[3:0] Pixel Repeat

This value indicates how many times the pixel was repeated. 0x0 = no repeats, sent once; 0x8 = 8 repeats, sent 9 times; and so on.

0x86—Bits[7:0] Active Line Start LSB

Combined with the MSB in Register 0x88, these bits indicate the beginning line of active video. All lines before this comprise a top horizontal bar. This is used in letter box modes. If the 2-byte value is 0x00, there is no horizontal bar.

0x87—Bits[6:0] New Data Flags (NDF)

This register indicates whether data in specific sections has changed. In the address space from 0x80 to 0xFF, each register address ending in 0b111 (for example, 0x87, 0x8F, 0x97, 0xAF) is an NDF register. They all have the same data and all are reset upon reading any one of them.

Table 29.

| NDF Bit number | Changes Occurred |
|----------------|-----------------------|
| 0 | AVI infoframe |
| 1 | Audio infoframe |
| 2 | SPD infoframe |
| 3 | MPEG source infoframe |
| 4 | ACP packets |
| 5 | ISRC1 packets |
| 6 | ISRC2 packets |

0x88—Bits[7:0] Active Line Start MSB

See Register 0x86.

0x89—Bits[7:0] Active Line End LSB

Combined with the MSB in Register 0x8A, these bits indicate the last line of active video. All lines past this comprise a lower horizontal bar. This is used in letter-box modes. If the 2-byte value is greater than the number of lines in the display, there is no lower horizontal bar.

0x8A—Bits[7:0] Active Line End MSB

See Register 0x89.

0x8B—Bits[7:0] Active Pixel Start LSB

Combined with the MSB in Register 0x8C, these bits indicate the first pixel in the display that is active video. All pixels before this comprise a left vertical bar. If the 2-byte value is 0x00, there is no left bar.

0x8C—Bits[7:0] Active Pixel Start MSB

See Register 0x8B.

0x8D—Bits[7:0] Active Pixel End LSB

Combined with the MSB in Register 0x8E, these bits indicate the last active video pixel in the display. All pixels past this comprise a right vertical bar. If the 2-byte value is greater than the number of pixels in the display, there is no vertical bar.

0x8E—Bits[7:0] Active Pixel End MSB

See Register 0x8D.

0x8F—Bits[6:0] NDF

See Register 0x87.

0x90—Bits[7:0] Audio Infoframe Version**0x91—Bits[7:4] Audio Coding Type**

These bits identify the audio coding so that the receiver may process audio properly.

Table 30.

| CT [3:0] | Audio Coding |
|----------|-----------------------------|
| 0x0 | Refer to stream header |
| 0x1 | IEC60958 PCM |
| 0x2 | AC-3 |
| 0x3 | MPEG1 (Layer 1 and Layer 2) |
| 0x4 | MP3 (MPEG1 Layer 3) |
| 0x5 | MPEG2 (multichannel) |
| 0x6 | AAC |
| 0x7 | DTS |
| 0x8 | ATRAC |

0x91—Bits[2:0] Audio Channel Count

These bits specify how many audio channels are being sent—2 channels to 8 channels.

Table 31.

| CC [2:0] | Channel Count |
|----------|------------------------|
| 000 | Refer to stream header |
| 001 | 2 |
| 010 | 3 |
| 011 | 4 |
| 100 | 5 |
| 101 | 6 |
| 110 | 7 |
| 111 | 8 |

0x92—Bits[4:2] Sampling Frequency**0x92—Bits[1:0] Ample Size****0x93—Bits[7:0] Max Bit Rate**

For compressed audio only, when this value is multiplied by 8 kHz represents the maximum bit rate. A value of 0x08 in this field yields a maximum bit rate of (8 kHz × 8 kHz = 64 kHz).

0x94—Bits[7:0] Speaker Mapping

These bits define the suggested placement of speakers.

Table 32.

| Abbreviation | Speaker Placement |
|--------------|----------------------|
| FL | Front left |
| FC | Front center |
| FR | Front right |
| FCL | Front center left |
| FCR | Front center right |
| RL | Rear left |
| RC | Rear center |
| RR | Rear right |
| RCL | Rear center left |
| RCR | Rear center right |
| LFE | Low frequency effect |

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Table 33.

| CA | | | | | Channel Number | | | | | | | |
|-------|-------|-------|-------|-------|----------------|-------|-------|-------|-------|-------|-------|-------|
| Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 |
| 0 | 0 | 0 | 0 | 0 | | | | | - | - | FR | FL |
| 0 | 0 | 0 | 0 | 1 | | | | | - | LFE | FR | FL |
| 0 | 0 | 0 | 1 | 0 | | | | | FC | - | FR | FL |
| 0 | 0 | 0 | 1 | 1 | | | | | FC | LFE | FR | FL |
| 0 | 0 | 1 | 0 | 0 | | | | RC | - | - | FR | FL |
| 0 | 0 | 1 | 0 | 1 | | | | RC | - | LFE | FR | FL |
| 0 | 0 | 1 | 1 | 0 | | | | RC | FC | - | FR | FL |
| 0 | 0 | 1 | 1 | 1 | | | | RC | FC | LFE | FR | FL |
| 0 | 1 | 0 | 0 | 0 | | | RR | RL | - | - | FR | FL |
| 0 | 1 | 0 | 0 | 1 | | | RR | RL | - | LFE | FR | FL |
| 0 | 1 | 0 | 1 | 0 | | | RR | RL | FC | - | FR | FL |
| 0 | 1 | 0 | 1 | 1 | - | - | RR | RL | FC | LFE | FR | FL |
| 0 | 1 | 1 | 0 | 0 | - | RC | RR | RL | - | - | FR | FL |
| 0 | 1 | 1 | 0 | 1 | - | RC | RR | RL | - | LFE | FR | FL |
| 0 | 1 | 1 | 1 | 0 | - | RC | RR | RL | FC | - | FR | FL |
| 0 | 1 | 1 | 1 | 1 | - | RC | RR | RL | FC | LFE | FR | FL |
| 1 | 0 | 0 | 0 | 0 | RRC | RLC | RR | RL | - | - | FR | FL |
| 1 | 0 | 0 | 0 | 1 | RRC | RLC | RR | RL | - | LFE | FR | FL |
| 1 | 0 | 0 | 1 | 0 | RRC | RLC | RR | RL | FC | - | FR | FL |
| 1 | 0 | 0 | 1 | 1 | RRC | RLC | RR | RL | FC | LFE | FR | FL |
| 1 | 0 | 1 | 0 | 0 | FRC | FLC | - | - | - | v | FR | FL |
| 1 | 0 | 1 | 0 | 1 | FRC | FLC | - | - | v | LFE | FR | FL |
| 1 | 0 | 1 | 1 | 0 | FRC | FLC | - | - | FC | - | FR | FL |
| 1 | 0 | 1 | 1 | 1 | FRC | FLC | - | - | FC | LFE | FR | FL |
| 1 | 1 | 0 | 0 | 0 | FRC | FLC | - | RC | - | - | FR | FL |
| 1 | 1 | 0 | 0 | 1 | FRC | FLC | - | RC | - | LFE | FR | FL |
| 1 | 1 | 0 | 1 | 0 | FRC | FLC | - | RC | FC | - | FR | FL |
| 1 | 1 | 0 | 1 | 1 | FRC | FLC | - | RC | FC | LFE | FR | FL |
| 1 | 1 | 1 | 0 | 0 | FRC | FLC | RR | RL | - | v | FR | FL |
| 1 | 1 | 1 | 0 | 1 | FRC | FLC | RR | RL | - | LFE | FR | FL |
| 1 | 1 | 1 | 1 | 0 | FRC | FLC | RR | RL | FC | - | FR | FL |
| 1 | 1 | 1 | 1 | 1 | FRC | FLC | RR | RL | FC | LFE | FR | FL |

0x95—Bit[7] Down-Mix Inhibit

0x95—Bits[6:3] Level Shift Values

These bits define the amount of attenuation. The value directly corresponds to the amount of attenuation: for example, 0000 = 0 dB, 0001 = 1 dB to 1111 = 15 dB attenuation.

0x96—Bits[7:0] Reserved

0x97—Bits[6:0] New Data Flags

See Register 0x87 for a description.

0x98—Bits[7:0] Source Product Description (SPD) Inframe Version

0x99—Bits[7:0] Vender Name Character 1 (VN1)

This is the first character in eight that is the name of the company that appears on the product. The data characters are 7-bit ASCII code.

0x9A—Bits[7:0] VN2

0x9B—Bits[7:0] VN3

0x9C—Bits[7:0] VN4

0x9D—Bits[7:0] VN5

0x9E—Bits[7:0] VN6

0x9F—Bits[6:0] New Data Flags

See Register 0x87 for a description.

0xA0—Bits[7:0] VN7

0xA1—Bits[7:0] VN8

0xA2—Bits[7:0] Product Description Character 1 (PD1)

This is the first character of 16 that contains the model number and a short description of the product. The data characters are 7-bit ASCII code.

0xA3—Bits[7:0] PD2**0xA4—Bits[7:0] PD3****0xA5—Bits[7:0] PD4****0xA6—Bits[7:0] PD5****0xA7—Bits[6:0] New Data Flags**

See Register 0x87 for a description.

0xA8—Bits[7:0] PD6**0xA9—Bits[7:0] PD7****0xAA—Bits[7:0] PD8****0xAB—Bits[7:0] PD9****0xAC—Bits[7:0] PD10****0xAD—Bits[7:0] PD11****0xAE—Bits[7:0] PD12****0xAF—Bits[6:0] New Data Flags**

See Register 0x87 for a description.

0xB0—Bits[7:0] PD13**0xB1—Bits[7:0] PD14****0xB2—Bits[7:0] PD15****0xB3—Bits[7:0] PD16****0xB4—Bits[7:0] Source Device Information Code**

These bytes classify the source device.

Table 34.

| SDI Code | Source |
|----------|-------------|
| 0x00 | Unknown |
| 0x01 | Digital STB |
| 0x02 | DVD |
| 0x03 | D-VHS |
| 0x04 | HDD video |
| 0x05 | DVC |
| 0x06 | DSC |
| 0x07 | Video CD |
| 0x08 | Game |
| 0x09 | PC general |

0xB7—Bits[6:0] New Data Flags

See Register 0x87 for a description.

0xB8—Bits[7:0] MPEG Source Inframe Version**0xB9—Bits[7:0] MPEG Bit Rate Byte 0 (MB0)**

The lower 8 of 32 bits that specify the MPEG bit rate in Hz.

0xBA—Bits[7:0] MB1**0xBB—Bits[7:0] MB2****0xBC—Bits[7:0] MB3—Upper Byte****0xBD—Bit[4] Field Repeat**

This defines whether the field is new or repeated. 0 = new field or picture. 1 = repeated field.

0xBD—Bits[1:0] MPEG Frame

This identifies the frame as I, B, or P.

Table 35.

| MF [1-0] | Frame Type |
|----------|------------|
| 00 | Unknown |
| 01 | I—picture |
| 10 | B—picture |
| 11 | P—picture |

0xBE—Bits[7:0] Reserved**0xBF—Bits[6:0] New Data Flags**

See Register 0x87 for a description.

0xC0—Bits[7:0] Audio Content Protection Packet (ACP Type)

These bits define which audio content protection is used.

Table 36.

| Code | ACP Type |
|-----------|------------------------------------|
| 0x00 | Generic audio |
| 0x01 | IEC 60958-identified audio |
| 0x02 | DVD-audio |
| 0x03 | Reserved for super audio CD (SACD) |
| 0x04—0xFF | Reserved |

0xC1—ACP Packet Byte 0 (ACP_PB0)**0xC2—Bits[7:0] ACP_PB1****0xC3—Bits[7:0] ACP_PB2****0xC4—Bits[7:0] ACP_PB3****0xC5—Bits[7:0] ACP_PB4****0xC7—Bits[6:0] New Data Flags**

See Register 0x87 for a description.

0xC8—Bit[7] International Standard Recording Code (ISRC1) Continued

This bit indicates that a continuation of the 16 ISRC1 packet bytes (an ISRC2 packet) is being transmitted.

0xC8—Bit[6] ISRC1 Valid

This bit is an indication of the whether ISRC1 packet bytes are valid. 0 = ISRC1 status bits and PBs not valid. 1 = ISRC1 status bits and PBs valid.

0xC8—Bits[2:0] ISRC Status

These bits define where in the ISRC track the samples are: at least two transmissions of 001 occur at the beginning of the track, while continuous transmission of 010 occurs in the middle of the track, followed by at least two transmissions of 100 near the end of the track.

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0xC9—Bits[7:0] ISRC1 Packet Byte 0 (ISRC1_PB0)

0xCA—Bits[7:0] ISRC1_PB1

0xCB—Bits[7:0] ISRC1_PB2

0xCC—Bits[7:0] ISRC1_PB3

0xCD—Bits[7:0] ISRC1_PB4

0xCE—Bits[7:0] ISRC1_PB5

0xCF—Bits[6:0] New Data Flags

See Register 0x87 for a description.

0xD0—Bits[7:0] ISRC1_PB6

0xD1—Bits[7:0] ISRC1_PB7

0xD2—Bits[7:0] ISRC1_PB8

0xD3—Bits[7:0] ISRC1_PB9

0xD4—Bits[7:0] ISRC1_PB10

0xD5—Bits[7:0] ISRC1_PB11

0xD6—Bits[7:0] ISRC1_PB12

0xD7—Bits[6:0] New Data Flags

See Register 0x87 for a description.

0xD8—Bits[7:0] ISRC1_PB13

0xD9—Bits[7:0] ISRC1_PB14

0xDA—Bits[7:0] ISRC1_PB15

0xDB—Bits[7:0] ISRC1_PB16

0xDC—Bits[7:0] ISRC2 Packet Byte 0 (ISRC2_PB0)

This is transmitted only when the ISRC continue bit (Register 0xC8 Bit 7) is set to 1.

0xDD—Bits[7:0] ISRC2_PB1

0xDE—Bits[7:0] ISRC2_PB2

0xDF—Bits[6:0] New Data Flags

See Register 0x87 for a description.

0xE0—Bits[7:0] ISRC2_PB3

0xE1—Bits[7:0] ISRC2_PB4

0xE2—Bits[7:0] ISRC2_PB5

0xE3—Bits[7:0] ISRC2_PB6

0xE4—Bits[7:0] ISRC2_PB7

0xE5—Bits[7:0] ISRC2_PB8

0xE6—Bits[7:0] ISRC2_PB9

0xE7—Bits[6:0] New Data Flags

See Register 0x87 for a description.

0xE8—Bits[7:0] ISRC2_PB10

0xE9—Bits[7:0] ISRC2_PB11

0xEA—Bits[7:0] ISRC2_PB12

0xEB—Bits[7:0] ISRC2_PB13

0xEC—Bits[7:0] ISRC2_PB14

0xED—Bits[7:0] ISRC2_PB15

0xEE—Bits[7:0] ISRC2_PB16

2-WIRE SERIAL CONTROL PORT

A 2-wire serial interface control is provided in the AD9381. Up to two AD9381 devices can be connected to the 2-wire serial interface, with a unique address for each device.

The 2-wire serial interface comprises a clock (SCL) and a bidirectional data (SDA) pin. The analog flat panel interface acts as a slave for receiving and transmitting data over the serial interface. When the serial interface is not active, the logic levels on SCL and SDA are pulled high by external pull-up resistors.

Data received or transmitted on the SDA line must be stable for the duration of the positive-going SCL pulse. Data on SDA must change only when SCL is low. If SDA changes state while SCL is high, the serial interface interprets that action as a start or stop sequence.

There are six components to serial bus operation:

- Start signal
- Slave address byte
- Base register address byte
- Data byte to read or write
- Stop signal
- Acknowledge (Ack)

When the serial interface is inactive (SCL and SDA are high), communications are initiated by sending a start signal. The start signal is a high-to-low transition on SDA while SCL is high. This signal alerts all slave devices that a data transfer sequence is coming.

The first 8 bits of data transferred after a start signal comprise a 7-bit slave address (the first 7 bits) and a single R/W bit (the 8th bit). The R/W bit indicates the direction of data transfer, read from (1) or write to (0) the slave device. If the transmitted slave address matches the address of the device (set by the state of the SA0 input pin as shown in Table 37), the AD9381 acknowledges by bringing SDA low on the 9th SCL pulse. If the addresses do not match, the AD9381 does not acknowledge.

Table 37. Serial Port Addresses

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 |
|----------------------|----------------|----------------|----------------|----------------|----------------|----------------|
| A ₆ (MSB) | A ₅ | A ₄ | A ₃ | A ₂ | A ₁ | A ₀ |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 |

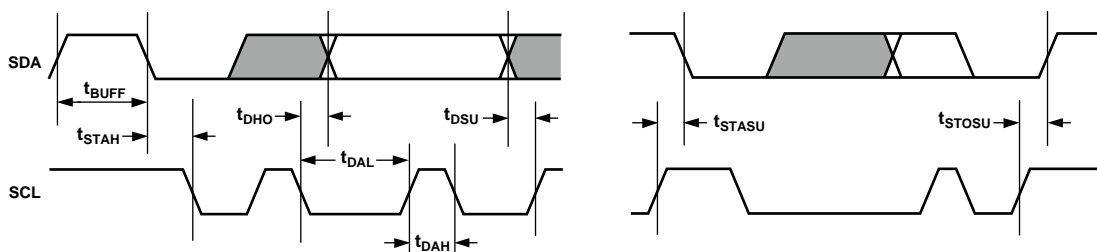


Figure 9. Serial Port Read/Write Timing

DATA TRANSFER VIA SERIAL INTERFACE

For each byte of data read or written, the MSB is the first bit of the sequence. If the AD9381 does not acknowledge the master device during a write sequence, the SDA remains high so the master can generate a stop signal. If the master device does not acknowledge the AD9381 during a read sequence, the AD9381 interprets this as the end of data. The SDA remains high so the master can generate a stop signal.

To write data to specific control registers of the AD9381, the 8-bit address of the control register of interest must be written after the slave address has been established. This control register address is the base address for subsequent write operations. The base address auto-increments by 1 for each byte of data written after the data byte intended for the base address. If more bytes are transferred than there are available addresses, the address does not increment and remains at its maximum value. Any base address higher than the maximum value does not produce an acknowledge signal.

Data are read from the control registers of the AD9381 in a similar manner. Reading requires two data transfer operations:

- The base address must be written with the R/W bit of the slave address byte low to set up a sequential read operation.
- Reading (the R/W bit of the slave address byte high) begins at the previously established base address. The address of the read register auto-increments after each byte is transferred.

To terminate a read/write sequence to the AD9381, a stop signal must be sent. A stop signal comprises a low-to-high transition of SDA while SCL is high.

A repeated start signal occurs when the master device driving the serial interface generates a start signal without first generating a stop signal to terminate the current communication. This is used to change the mode of communication (read, write) between the slave and master without releasing the serial interface lines.

SERIAL INTERFACE READ/WRITE EXAMPLES

Write to one control register:

- Start signal
- Slave address byte ($\overline{R/\overline{W}}$ bit = low)
- Base address byte
- Data byte to base address
- Stop signal

Write to four consecutive control registers:

- Start signal
- Slave address byte ($\overline{R/\overline{W}}$ bit = low)
- Base address byte
- Data byte to base address
- Data byte to (base address + 1)
- Data byte to (base address + 2)
- Data byte to (base address + 3)
- Stop signal

Read from one control register:

- Start signal
- Slave address byte ($\overline{R/\overline{W}}$ bit = low)
- Base address byte
- Start signal
- Slave address byte ($\overline{R/\overline{W}}$ bit = high)
- Data byte from base address
- Stop signal

Read from four consecutive control registers:

- Start signal
- Slave address byte ($\overline{R/\overline{W}}$ bit = low)
- Base address byte
- Start signal
- Slave address byte ($\overline{R/\overline{W}}$ bit = high)
- Data byte from base address
- Data byte from (base address + 1)
- Data byte from (base address + 2)
- Data byte from (base address + 3)
- Stop signal

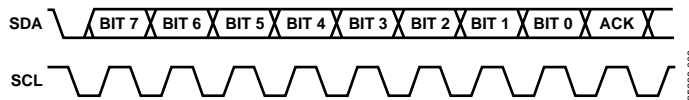


Figure 10. Serial Interface—Typical Byte Transfer

PCB LAYOUT RECOMMENDATIONS

The AD9381 is a high precision, high speed digital device. To achieve the maximum performance from the part, it is important to have a well laid-out board. The following is a guide for designing a board using the AD9381.

POWER SUPPLY BYPASSING

It is recommended to bypass each power supply pin with a 0.1 μ F capacitor. The exception is in the case where two or more supply pins are adjacent to each other. For these groupings of powers/grounds, it is only necessary to have one bypass capacitor. The fundamental idea is to have a bypass capacitor within about 0.5 cm of each power pin. Also, avoid placing the capacitor on the opposite side of the PC board from the AD9381, because that interposes resistive vias in the path.

The bypass capacitors should be physically located between the power plane and the power pin. Current should flow from the power plane to the capacitor to the power pin. Do not make the power connection between the capacitor and the power pin. Placing a via underneath the capacitor pads down to the power plane is generally the best approach.

It is particularly important to maintain low noise and good stability of PV_{DD} (the clock generator supply). Abrupt changes in PV_{DD} can result in similarly abrupt changes in sampling clock phase and frequency. This can be avoided by careful attention to regulation, filtering, and bypassing. It is highly desirable to provide separate regulated supplies for each of the analog circuitry groups (V_D and PV_{DD}).

Some graphic controllers use substantially different levels of power when active (during active picture time) and when idle (during HSYNC and VSYNC periods). This can result in a measurable change in the voltage supplied to the analog supply regulator, which can in turn produce changes in the regulated analog supply voltage. This can be mitigated by regulating the analog supply, or at least PV_{DD} , from a different, cleaner power source (for example, from a 12 V supply).

It is recommended to use a single ground plane for the entire board. Experience has shown repeatedly that the noise performance is the same or better with a single ground plane. Using multiple ground planes can be detrimental because each separate ground plane is smaller and long ground loops can result.

In some cases, using separate ground planes is unavoidable, so it is recommend to place a single ground plane under the AD9381. The location of the split should be at the receiver of the digital outputs. In this case, it is even more important to place components wisely because the current loops are much longer, (current takes the path of least resistance). An example of a current loop is power plane to AD9381 to digital output trace to digital data receiver to digital ground plane to analog ground plane.

OUTPUTS (BOTH DATA AND CLOCKS)

Try to minimize the trace length that the digital outputs have to drive. Longer traces have higher capacitance, which require more current that causes more internal digital noise.

Shorter traces reduce the possibility of reflections.

Adding a series resistor of value 50 Ω to 200 Ω can suppress reflections, reduce EMI, and reduce the current spikes inside the AD9381. If series resistors are used, place them as close as possible to the AD9381 pins (although try not to add vias or extra length to the output trace to move the resistors closer).

If possible, limit the capacitance that each of the digital outputs drives to less than 10 pF. This can be accomplished easily by keeping traces short and by connecting the outputs to only one device. Loading the outputs with excessive capacitance increases the current transients inside of the AD9381 and creates more digital noise on its power supplies.

DIGITAL INPUTS

The digital inputs on the AD9381 were designed to work with 3.3 V signals, but are tolerant of 5.0 V signals. Therefore, no extra components need to be added if using 5.0 V logic.

Any noise that enters the HSYNC input trace can add jitter to the system. Therefore, minimize the trace length and do not run any digital or other high frequency traces near it.

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COLOR SPACE CONVERTER (CSC) COMMON SETTINGS

Table 38. HDTV YCrCb (0 to 255) to RGB (0 to 255) (Default Setting for AD9381)

| Register | Red/Cr Coeff 1 | | Red/Cr Coeff 2 | | Red/Cr Coeff 3 | | Red/Cr Offset | |
|----------|-----------------|------|-----------------|------|-----------------|------|----------------|------|
| Address | 0x35 | 0x36 | 0x37 | 0x38 | 0x39 | 0x3A | 0x3B | 0x3C |
| Value | 0x0C | 0x52 | 0x08 | 0x00 | 0x00 | 0x00 | 0x19 | 0xD7 |
| Register | Green/Y Coeff 1 | | Green/Y Coeff 2 | | Green/Y Coeff 3 | | Green/Y Offset | |
| Address | 0x3D | 0x3E | 0x3F | 0x40 | 0x41 | 0x42 | 0x43 | 0x44 |
| Value | 0x1C | 0x54 | 0x08 | 0x00 | 0x3E | 0x89 | 0x02 | 0x91 |
| Register | Blue/Cb Coeff 1 | | Blue/Cb Coeff 2 | | Blue/Cb Coeff 3 | | Blue/Cb Offset | |
| Address | 0x45 | 0x46 | 0x47 | 0x48 | 0x49 | 0x4A | 0x4B | 0x4C |
| Value | 0x00 | 0x00 | 0x08 | 0x00 | 0x0E | 0x87 | 0x18 | 0xBD |

Table 39. HDTV YCrCb (16 to 235) to RGB (0 to 255)

| Register | Red/Cr Coeff 1 | | Red/Cr Coeff 2 | | Red/Cr Coeff 3 | | Red/Cr Offset | |
|----------|-----------------|------|-----------------|------|-----------------|------|----------------|------|
| Address | 0x35 | 0x36 | 0x37 | 0x38 | 0x39 | 0x3A | 0x3B | 0x3C |
| Value | 0x47 | 0x2C | 0x04 | 0xA8 | 0x00 | 0x00 | 0x1C | 0x1F |
| Register | Green/Y Coeff 1 | | Green/Y Coeff 2 | | Green/Y Coeff 3 | | Green/Y Offset | |
| Address | 0x3D | 0x3E | 0x3F | 0x40 | 0x41 | 0x42 | 0x43 | 0x44 |
| Value | 0x1D | 0xDD | 0x04 | 0xA8 | 0x1F | 0x26 | 0x01 | 0x34 |
| Register | Blue/Cb Coeff 1 | | Blue/Cb Coeff 2 | | Blue/Cb Coeff 3 | | Blue/Cb Offset | |
| Address | 0x45 | 0x46 | 0x47 | 0x48 | 0x49 | 0x4A | 0x4B | 0x4C |
| Value | 0x00 | 0x00 | 0x04 | 0xA8 | 0x08 | 0x75 | 0x1B | 0x7B |

Table 40. SDTV YCrCb (0 to 255) to RGB (0 to 255)

| Register | Red/Cr Coeff 1 | | Red/Cr Coeff 2 | | Red/Cr Coeff 3 | | Red/Cr Offset | |
|----------|-----------------|------|-----------------|------|-----------------|------|----------------|------|
| Address | 0x35 | 0x36 | 0x37 | 0x38 | 0x39 | 0x3A | 0x3B | 0x3C |
| Value | 0x2A | 0xF8 | 0x08 | 0x00 | 0x00 | 0x00 | 0x1A | 0x84 |
| Register | Green/Y Coeff 1 | | Green/Y Coeff 2 | | Green/Y Coeff 3 | | Green/Y Offset | |
| Address | 0x3D | 0x3E | 0x3F | 0x40 | 0x41 | 0x42 | 0x43 | 0x44 |
| Value | 0x1A | 0x6A | 0x08 | 0x00 | 0x1D | 0x50 | 0x04 | 0x23 |
| Register | Blue/Cb Coeff 1 | | Blue/Cb Coeff 2 | | Blue/Cb Coeff 3 | | Blue/Cb Offset | |
| Address | 0x45 | 0x46 | 0x47 | 0x48 | 0x49 | 0x4A | 0x4B | 0x4C |
| Value | 0x00 | 0x00 | 0x08 | 0x00 | 0x0D | 0xDB | 0x19 | 0x12 |

Table 41. SDTV YCrCb (16 to 235) to RGB (0 to 255)

| Register | Red/Cr Coeff 1 | | Red/Cr Coeff 2 | | Red/Cr Coeff 3 | | Red/Cr Offset | |
|----------|-----------------|------|-----------------|------|-----------------|------|----------------|------|
| Address | 0x35 | 0x36 | 0x37 | 0x38 | 0x39 | 0x3A | 0x3B | 0x3C |
| Value | 0x46 | 0x63 | 0x04 | 0xA8 | 0x00 | 0x00 | 0x1C | 0x84 |
| Register | Green/Y Coeff 1 | | Green/Y Coeff 2 | | Green/Y Coeff 3 | | Green/Y Offset | |
| Address | 0x3D | 0x3E | 0x3F | 0x40 | 0x41 | 0x42 | 0x43 | 0x44 |
| Value | 0x1C | 0xC0 | 0x04 | 0xA8 | 0x1E | 0x6F | 0x02 | 0x1E |
| Register | Blue/Cb Coeff 1 | | Blue/Cb Coeff 2 | | Blue/Cb Coeff 3 | | Blue/Cb Offset | |
| Address | 0x45 | 0x46 | 0x47 | 0x48 | 0x49 | 0x4A | 0x4B | 0x4C |
| Value | 0x00 | 0x00 | 0x04 | 0xA8 | 0x08 | 0x11 | 0x1B | 0xAD |

Table 42. RGB (0 to 255) to HDTV YCrCb (0 to 255)

| Register | Red/Cr Coeff 1 | | Red/Cr Coeff 2 | | Red/Cr Coeff 3 | | Red/Cr Offset | |
|----------|-----------------|------|-----------------|------|-----------------|------|----------------|------|
| Address | 0x35 | 0x36 | 0x37 | 0x38 | 0x39 | 0x3A | 0x3B | 0x3C |
| Value | 0x08 | 0x2D | 0x18 | 0x93 | 0x1F | 0x3F | 0x08 | 0x00 |
| Register | Green/Y Coeff 1 | | Green/Y Coeff 2 | | Green/Y Coeff 3 | | Green/Y Offset | |
| Address | 0x3D | 0x3E | 0x3F | 0x40 | 0x41 | 0x42 | 0x43 | 0x44 |
| Value | 0x03 | 0x68 | 0x0B | 0x71 | 0x01 | 0x27 | 0x00 | 0x00 |
| Register | Blue/Cb Coeff 1 | | Blue/Cb Coeff 2 | | Blue/Cb Coeff 3 | | Blue/Cb Offset | |
| Address | 0x45 | 0x46 | 0x47 | 0x48 | 0x49 | 0x4A | 0x4B | 0x4C |
| Value | 0x1E | 0x21 | 0x19 | 0xB2 | 0x08 | 0x2D | 0x08 | 0x00 |

Table 43. RGB (0 to 255) to HDTV YCrCb (16 to 235)

| Register | Red/Cr Coeff 1 | | Red/Cr Coeff 2 | | Red/Cr Coeff 3 | | Red/Cr Offset | |
|----------|-----------------|------|-----------------|------|-----------------|------|----------------|------|
| Address | 0x35 | 0x36 | 0x37 | 0x38 | 0x39 | 0x3A | 0x3B | 0x3C |
| Value | 0x07 | 0x06 | 0x19 | 0xA0 | 0x1F | 0x5B | 0x08 | 0x00 |
| Register | Green/Y Coeff 1 | | Green/Y Coeff 2 | | Green/Y Coeff 3 | | Green/Y Offset | |
| Address | 0x3D | 0x3E | 0x3F | 0x40 | 0x41 | 0x42 | 0x43 | 0x44 |
| Value | 0x02 | 0xED | 0x09 | 0xD3 | 0x00 | 0xFD | 0x01 | 0x00 |
| Register | Blue/Cb Coeff 1 | | Blue/Cb Coeff 2 | | Blue/Cb Coeff 3 | | Blue/Cb Offset | |
| Address | 0x45 | 0x46 | 0x47 | 0x48 | 0x49 | 0x4A | 0x4B | 0x4C |
| Value | 0x1E | 0x64 | 0x1A | 0x96 | 0x07 | 0x06 | 0x08 | 0x00 |

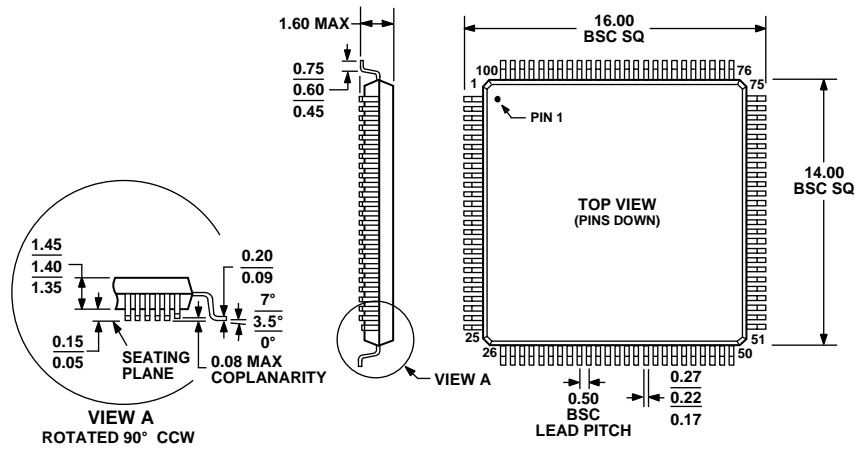
Table 44. RGB (0 to 255) to SDTV YCrCb (0 to 255)

| Register | Red/Cr Coeff 1 | | Red/Cr Coeff 2 | | Red/Cr Coeff 3 | | Red/Cr Offset | |
|----------|-----------------|------|-----------------|------|-----------------|------|----------------|------|
| Address | 0x35 | 0x36 | 0x37 | 0x38 | 0x39 | 0x3A | 0x3B | 0x3C |
| Value | 0x08 | 0x2D | 0x19 | 0x27 | 0x1E | 0xAC | 0x08 | 0x00 |
| Register | Green/Y Coeff 1 | | Green/Y Coeff 2 | | Green/Y Coeff 3 | | Green/Y Offset | |
| Address | 0x3D | 0x3E | 0x3F | 0x40 | 0x41 | 0x42 | 0x43 | 0x44 |
| Value | 0x04 | 0xC9 | 0x09 | 0x64 | 0x01 | 0xD3 | 0x00 | 0x00 |
| Register | Blue/Cb Coeff 1 | | Blue/Cb Coeff 2 | | Blue/Cb Coeff 3 | | Blue/Cb Offset | |
| Address | 0x45 | 0x46 | 0x47 | 0x48 | 0x49 | 0x4A | 0x4B | 0x4C |
| Value | 0x1D | 0x3F | 0x1A | 0x93 | 0x08 | 0x2D | 0x08 | 0x00 |

Table 45. RGB (0 to 255) to SDTV YCrCb (16 to 235)

| Register | Red/Cr Coeff 1 | | Red/Cr Coeff 2 | | Red/Cr Coeff 3 | | Red/Cr Offset | |
|----------|-----------------|------|-----------------|------|-----------------|------|----------------|------|
| Address | 0x35 | 0x36 | 0x37 | 0x38 | 0x39 | 0x3A | 0x3B | 0x3C |
| Value | 0x07 | 0x06 | 0x1A | 0x1E | 0x1E | 0xDC | 0x08 | 0x00 |
| Register | Green/Y Coeff 1 | | Green/Y Coeff 2 | | Green/Y Coeff 3 | | Green/Y Offset | |
| Address | 0x3D | 0x3E | 0x3F | 0x40 | 0x41 | 0x42 | 0x43 | 0x44 |
| Value | 0x04 | 0x1C | 0x08 | 0x11 | 0x01 | 0x91 | 0x01 | 0x00 |
| Register | Blue/Cb Coeff 1 | | Blue/Cb Coeff 2 | | Blue/Cb Coeff 3 | | Blue/Cb Offset | |
| Address | 0x45 | 0x46 | 0x47 | 0x48 | 0x49 | 0x4A | 0x4B | 0x4C |
| Value | 0x1D | 0xA3 | 0x1B | 0x57 | 0x07 | 0x06 | 0x08 | 0x00 |

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-026-BED

Figure 11. 100-Lead Low Profile Quad Flat Package [LQFP] (ST-100)

Dimensions shown in millimeters

ORDERING GUIDE

| Model | Max Speed (MHz) | | Temperature Range | Package Description | Package Option |
|-----------------------------|-----------------|---------|-------------------|---|----------------|
| | Analog | Digital | | | |
| AD9381KSTZ-100 ¹ | 100 | 100 | 0°C to 70°C | 100-Lead Low Profile Quad Flat Package (LQFP) | ST-100 |
| AD9381KSTZ-150 ¹ | 150 | 150 | 0°C to 70°C | 100-Lead Low Profile Quad Flat Package (LQFP) | ST-100 |
| AD9381/PCB | | | | Evaluation Board | |

¹ Z = Pb-free part.

NOTES

AD9381

NOTES