AKD4955-A

AK4955 Evaluation Board Rev.3

GENERAL DESCRIPTION

The AKD4955-A is an evaluation board for AK4955, 24bit stereo CODEC with a microphone/ speaker/ video amplifiers, DSP and LDO. The AKD4955-A has the Digital Audio I/F and can achieve the interface with digital audio systems via optical connector.

■ Ordering Guide

AKD4955-A --- AK4955 Evaluation Board
(Cable for connecting with USB Port of PC and control software are packed with this.)

FUNCTION

- **DIR/DIT with optical input/output**
- **BNC connector for an external clock input**

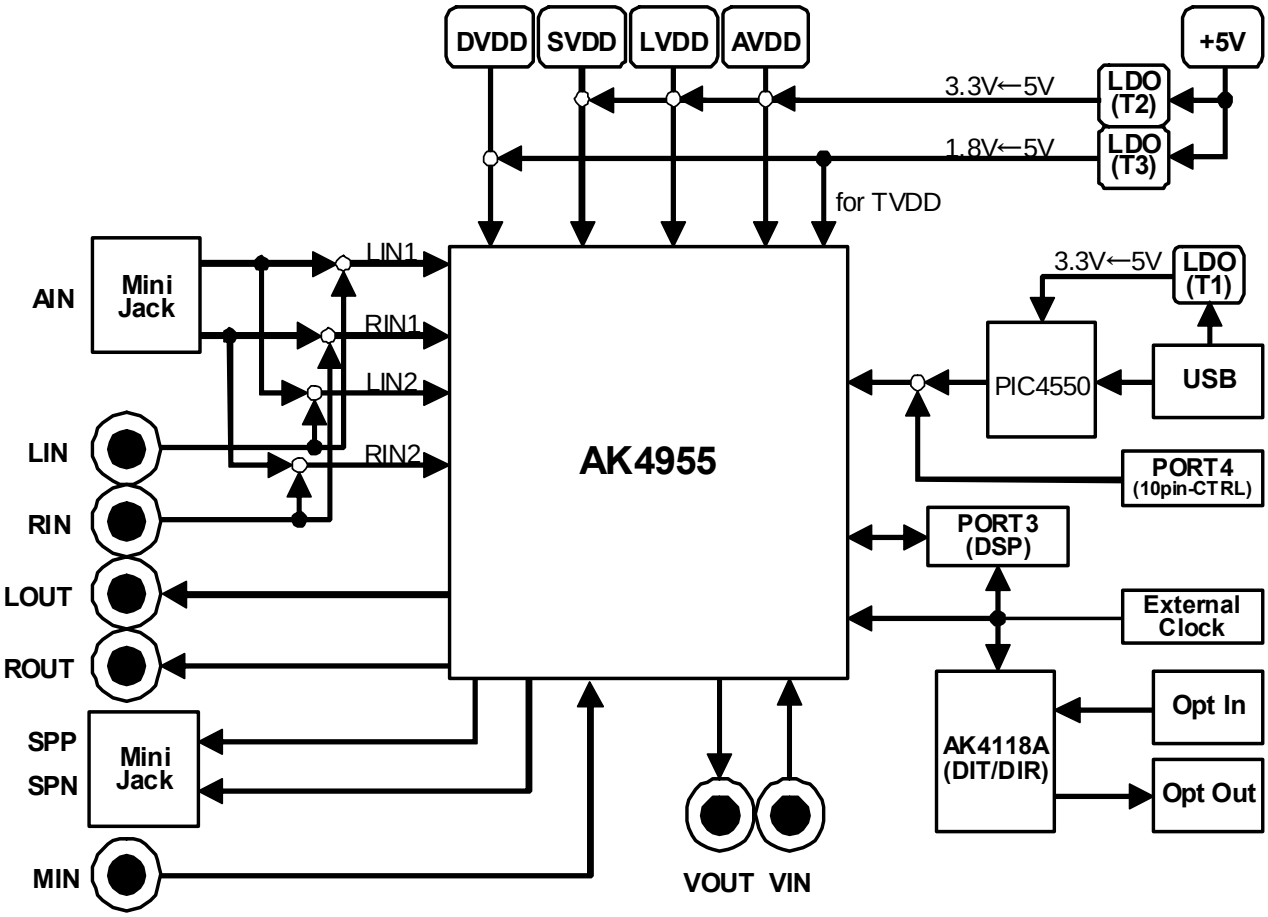


Figure 1.AKD4955-A Block Diagram

■ Operation Sequence

1) Set up the Power Supply Lines.

2) Setup the Audio I/F Evaluation Mode.

(1) Evaluation of A/D using DIT of AK4118A.
  (1-1) Setting with External Slave Mode.
  (1-2) Setting with External Master Mode.

(2) Evaluation of D/A using DIR of AK4118A.
  (2-1) Setting with External Slave Mode. < Default >
  (2-2) Setting with External Master Mode.

(3) Evaluation of A/D, D/A using PORT3 (DSP).
  (3-1) Setting with External Slave Mode.
  (3-2) Setting with External Master Mode.
  (3-3) Setting with PLL Slave Mode.
  (3-4) Setting with PLL Master Mode.

(4) Evaluation of external Loop-back (A/D -> D/A).
  (4-1) Setting with External Slave Mode.
  (4-2) Setting with External Master Mode.
  (4-3) Setting with PLL Slave Mode.
  (4-4) Setting with PLL Master Mode.

3) Jumper pins and SW Setting.

(1) Setting of other jumper pins.

(2) Setting of SW.

4) Power on.

1) Set up the Power Supply Lines.

(1-1) In case of using the regulator. < Default >

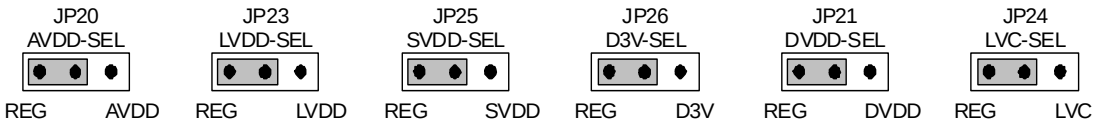


Figure 2.Setting of jumper pins, when using the regulator.

Name of Jack	Color	Default Setting	Using
+5V	red	5V	for regulator.
AVDD	green	Open	for AVDD of AK4955
LVDD	green	Open	for LVDD of AK4955
SVDD	green	Open	for SVDD of AK4955
D3V	green	Open	for AK4118A and digital logic.
DVDD	green	Open	for DVDD of AK4955
LVC	green	Open	for TVDD of AK4955 and digital logic.
AGND	black	0V	for analog ground
DGND	black	0V	for digital ground

Table 1.Set up of power supply lines

(1-2) In case of using the power supply connectors.

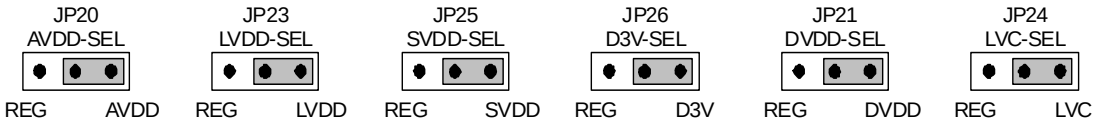


Figure 3.Setting of jumper pins, when using the power supply connectors.

Name of Jack	Color	Default Setting	Using
+5V	red	Open	for regulator.
AVDD	green	+2.8V ~ +3.6V [typ:+3.3V]	for AVDD of AK4955
LVDD	green	+2.7V ~ +5.5V [typ:+3.3V]	for LVDD of AK4955
SVDD	green	+2.7V ~ +5.5V [typ:+3.3V]	for SVDD of AK4955
D3V	green	+2.7V ~ +3.6V [typ:+3.3V]	for AK4118A and digital logic.
DVDD	green	+1.6V ~ +2.0V [typ:+1.8V]	for DVDD of AK4955
LVC	green	+1.6V ~ +3.6V [typ:+1.8V]	for TVDD of AK4955 and digital logic.
AGND	black	0V	for analog ground
DGND	black	0V	for digital ground

Table 2.Set up of power supply lines (Note 1)

Note 1.Each supply line should be distributed from the power supply unit.

2) Setup the Audio I/F Evaluation Mode.

In case of using the AK4118A when evaluating the AK4955, both the AK4955 and AK4118A's audio interface formats must be matched.
Refer to the datasheet for AK4955's audio interface format, and AK4118A's audio interface format (Table 4).
The AK4118A operates at sampling frequency of 32 kHz or more. If the sampling frequency is slower than 32 kHz, please use other mode.
In addition, MCLK of AK4118A supports 256fs and 512fs. When evaluating in a condition except above, please use other mode.
Refer to the datasheet for register setting of the AK4955.

(1) Evaluation of A/D using DIT of AK4118A.

(1-1) Setting with External Slave Mode

X1 (X'tal) and PORT2 (TOTX) are used. Nothing should be connected to PORT1 (TORX) and PORT3 (DSP).
MCKI, BICK and LRCK are supplied from the AK4118A, and SDTO of the AK4955 is output to the AK4118A.
In addition, registers of the AK4955 should be set to "External Slave Mode" and setting of AK4118A should be set to "Master Mode".
SW4 (M/S) should be set to "ON (H)".

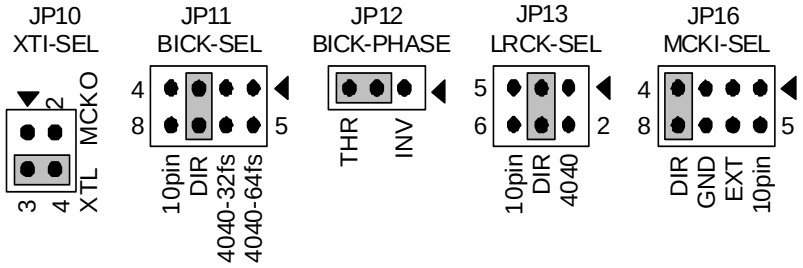


Figure 4.Setting of jumper pins with External Slave Mode

(1-2) Setting with External Master Mode

X1 (X'tal) and PORT2 (TOTX) are used. Nothing should be connected to PORT1 (TORX) and PORT3 (DSP).
MCKI is supplied from the AK4118A, and BICK, LRCK and SDTO of the AK4955 is output to the AK4118A.
In addition, registers of the AK4955 should be set to "External Master Mode" and setting of AK4118A should be set to "Slave Mode".
SW4 (M/S) should be set to "OFF (L)".

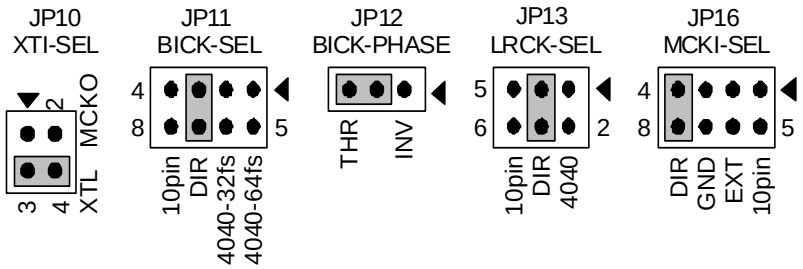


Figure 5.Setting of jumper pins with External Master Mode

(2) Evaluation of D/A using DIR of AK4118A.

(2-1) Setting with External Slave Mode < Default >

PORT1 (TORX) is used. Nothing should be connected to PORT2 (TOTX) and PORT3 (DSP).
MCKI, BICK, LRCK and SDTI are supplied from the AK4118A.
In addition, registers of the AK4955 should be set to “External Slave Mode” and setting of AK4118A should be set to “Master Mode”.
SW4 (M/S) should be set to “ON (H)”.

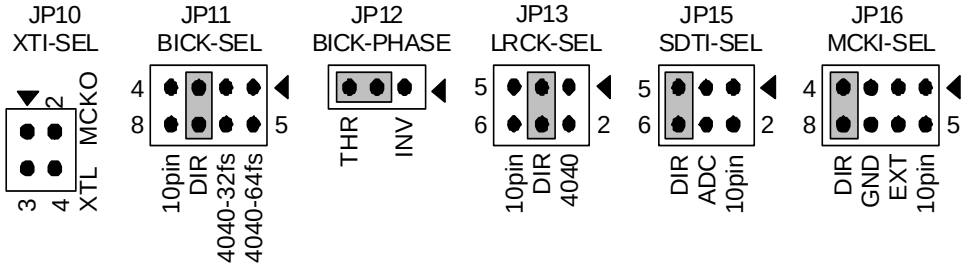


Figure 6.Setting of jumper pins with External Slave Mode

(2-2) Setting with External Master Mode

PORT1 (TORX) is used. Nothing should be connected to PORT2 (TOTX) and PORT3 (DSP).
MCKI and SDTI are supplied from the AK4118A, and BICK and LRCK of the AK4955 is output to the AK4118A.
In addition, registers of the AK4955 should be set to “External Master Mode” and setting of AK4118A should be set to “Slave Mode”.
SW4 (M/S) should be set to “OFF (L)”.

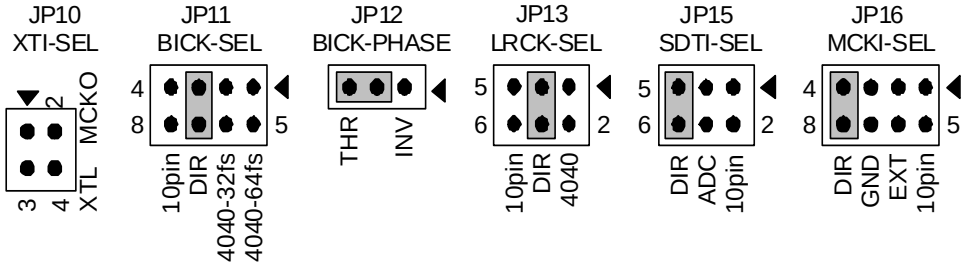


Figure 7.Setting of jumper pins with External Master Mode

(3) Evaluation of A/D, D/A using PORT3 (DSP).

(3-1) Setting with External Slave Mode

Registers of the AK4955 should be set to "External Slave Mode".
SW4 (M/S) should be set to "ON (H)".

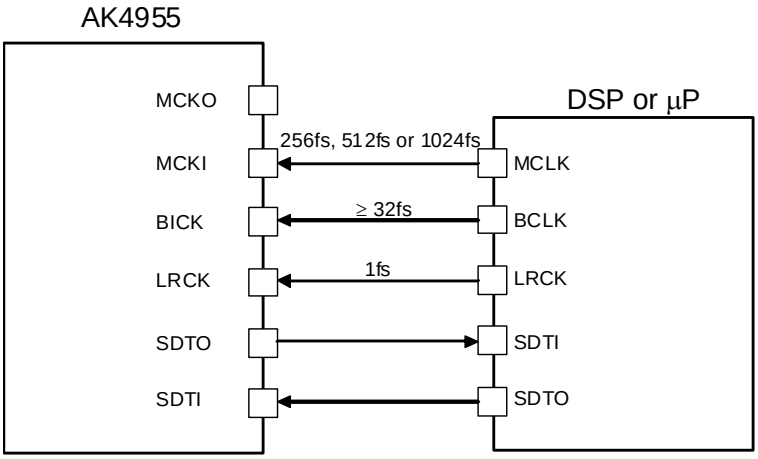


Figure 8.External Slave Mode

PORT3 (DSP) is used. Nothing should be connected to PORT1 (TORX) and PORT2 (TOTX).
MCLK, BICK, LRCK, and SDTI are input from PORT3 (DSP) and SDTO of the AK4955 is output to the PORT3 (DSP).

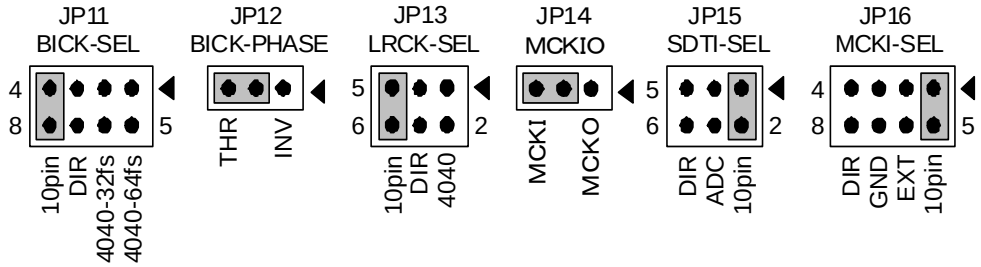


Figure 9.Setting of jumper pins with External Slave Mode (Note 2)

Note 2.JP12 (BICK-PHASE) is jumper which decides polarity of BICK, "THR" or "INV" should be selected according to the Audio I/F format.

(3-2) Setting with External Master Mode

Registers of the AK4955 should be set to “External Master Mode”.
SW4 (M/S) should be set to “OFF (L)”.

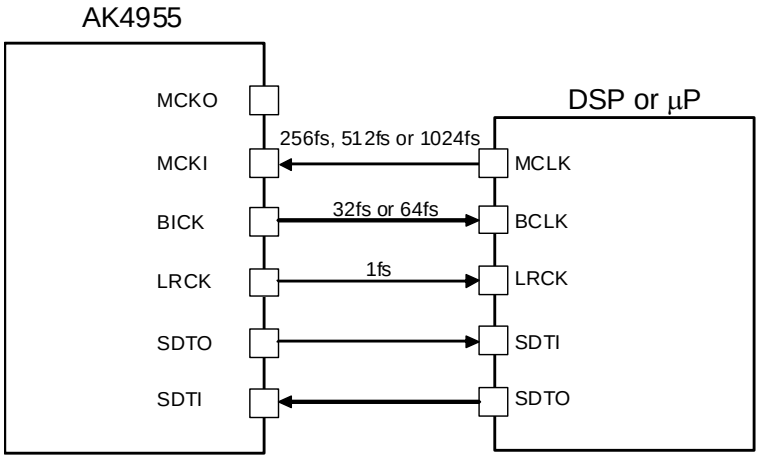


Figure 10.External Master Mode

PORT3 (DSP) is used. Nothing should be connected to PORT1 (TORX) and PORT2 (TOTX).
MCLK and SDTI are input from PORT3 (DSP) and BICK, LRCK and SDTO of the AK4955 is output to the PORT3 (DSP).

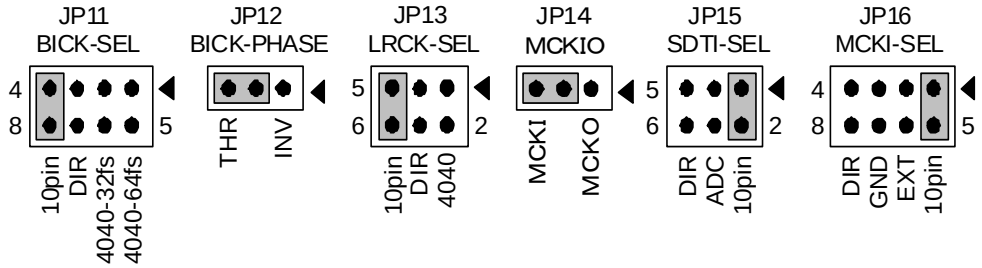


Figure 11.Setting of jumper pins with External Master Mode

(3-3) Setting with PLL Slave Mode

A reference clock of PLL is selected among the input clocks supplied to MCKI pin. The required clock to the AK4955 is generated by an internal PLL circuit.
SW4 (M/S) should be set to "ON (H)".

(a) PLL Reference Clock: MCKI pin

Registers of the AK4955 should be set to "PLL Slave Mode" (Reference Clock: MCKI pin).
BICK and LRCK inputs should be synchronized with MCKO output. However the phase between MCKO and LRCK dose not matter.

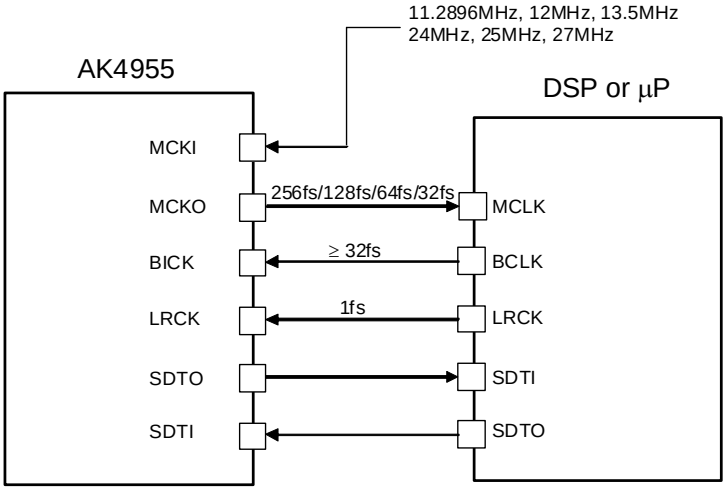


Figure 12.PLL Slave Mode 1 (PLL Reference Clock: MCKI pin)

J10 (EXT) and PORT3 (DSP) are used (Note 3). Nothing should be connected to PORT1 (TORX) and PORT2 (TOTX).
MCKI is input from J10 (EXT). BICK, LRCK and SDTI are input from PORT3 (DSP). MCKO and SDTO of the AK4955 is output to the PORT3 (DSP).

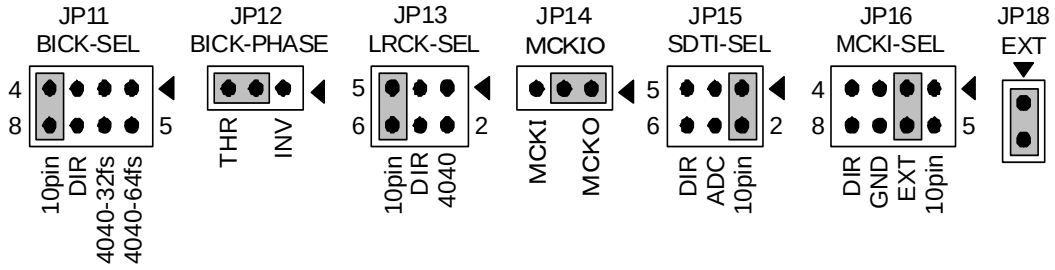


Figure 13.Setting of jumper pins with PLL Slave Mode (Note 4)

Note 3.When a termination (51Ω) of J10 (EXT) is not used, JP18 (EXT) should be open.
Note 4.JP12 (BICK-PHASE) is jumper which decides polarity of BICK, "THR" or "INV" should be selected according to the Audio I/F format.

(b) PLL Reference Clock: BICK pin

Registers of the AK4955 should be set to “PLL Slave Mode” (Reference Clock: BICK pin).

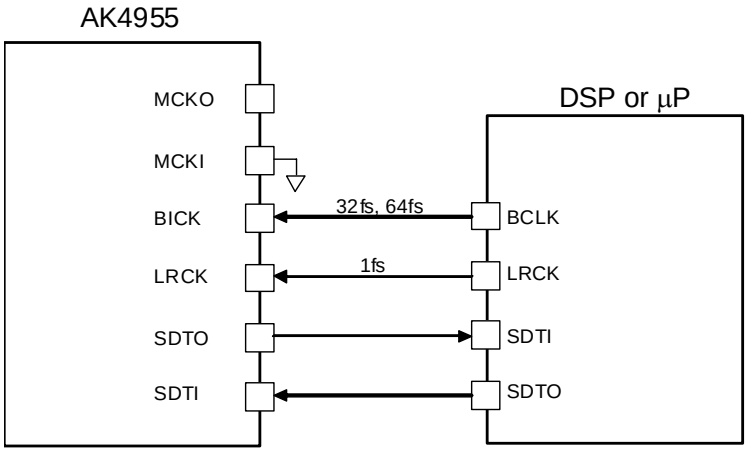


Figure 14.PLL Slave Mode 2 (PLL Reference Clock: BICK pin)

PORT3 (DSP) is used. Nothing should be connected to PORT1 (TORX) and PORT2 (TOTX). BICK, LRCK and SDTI are input from PORT3 (DSP). SDTO of the AK4955 is output to the PORT3 (DSP).

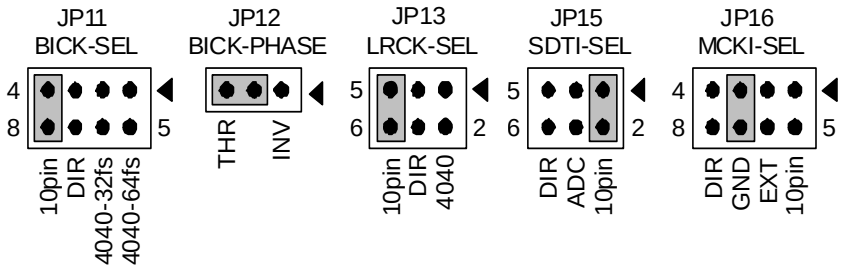


Figure 15.Setting of jumper pins with PLL Slave Mode (Note 5)

Note 5.JP12 (BICK-PHASE) is jumper which decides polarity of BICK, “THR” or “INV” should be selected according to the Audio I/F format.

(3-4) Setting with PLL Master Mode

The master clock is input from MCKI pin of J10 (EXT). An internal PLL circuit generates MCKO, BICK, and LRCK.
In addition, registers of the AK4955 should be set to “PLL Master Mode”.
SW4 (M/S) should be set to “ON (H)”.

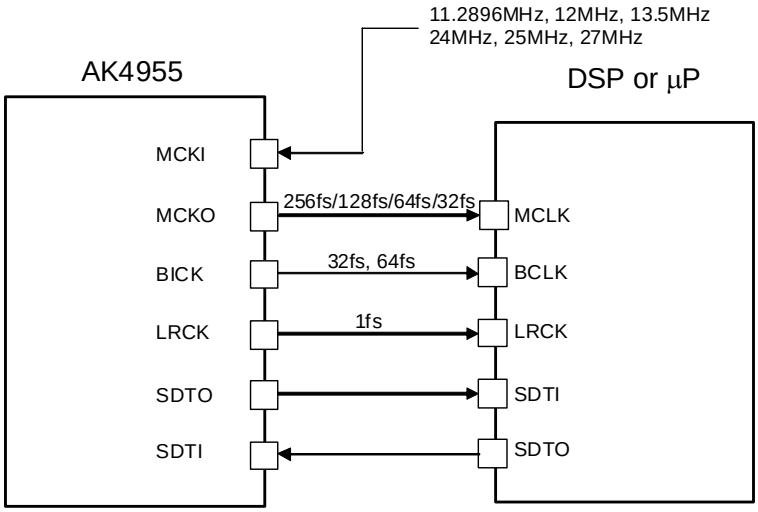


Figure 16.PLL Master Mode

J10 (EXT) and PORT3 (DSP) are used (Note 6). Nothing should be connected to PORT1 (TORX) and PORT2 (TOTX).
MCKI is input from J10 (EXT) and SDTI is input from PORT3 (DSP). BICK, LRCK, MCKO and SDTO of the AK4955 are output to the PORT3 (DSP).

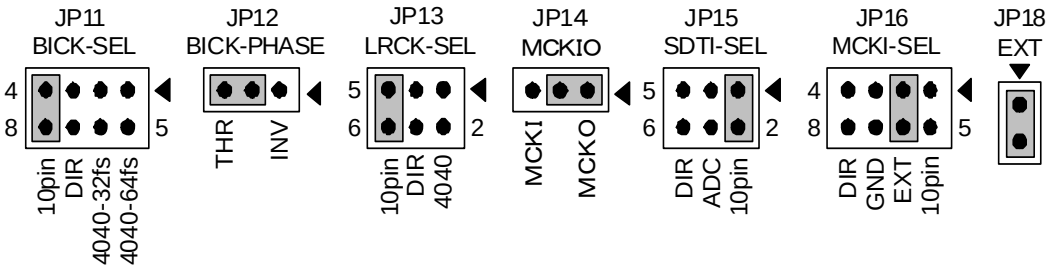


Figure 17.Setting of jumper pins with PLL Slave Mode

Note 6.When a termination (51Ω) of J10 (EXT) is not used, JP18 (EXT) should be open.

(4) Evaluation of external Loop-back (A/D -> D/A).

(4-1) Setting with External Slave Mode.

J10 (EXT) is used (Note 7). Nothing should be connected to PORT1 (TORX), PORT2 (TOTX) and PORT3 (DSP).
MCKI is input from J10 (EXT). BICK and LRCK are generated by on-board divider. SDTI is connected to SDTO of the AK4955 as loopback.
In addition, registers of the AK4955 should be set to "External Slave Mode".
SW4 (M/S) should be set to "ON (H)".

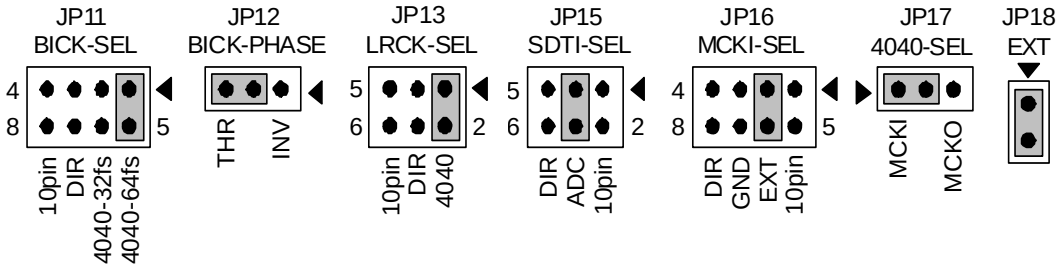


Figure 18.Setting of jumper pins with External Slave Mode (Note 8, Note 9)

Note 7.When a termination (51Ω) of J10 (EXT) is not used, JP18 (EXT) should be open.
Note 8.JP12 (BICK-PHASE) is jumper which decides polarity of BICK, "THR" or "INV" should be selected according to the Audio I/F format.
Note 9.When BICK of 32fs is used, JP11 (BICK-SEL) should be set to "4040-32fs" side.

(4-2) Setting with External Master Mode.

J10 (EXT) is used (Note 10). Nothing should be connected to PORT1 (TORX), PORT2 (TOTX) and PORT3 (DSP).
MCKI is input from J10 (EXT), SDTI is connected to SDTO of the AK4955 as loopback.
In addition, registers of the AK4955 should be set to "External Master Mode".
SW4 (M/S) should be set to "OFF (L)".

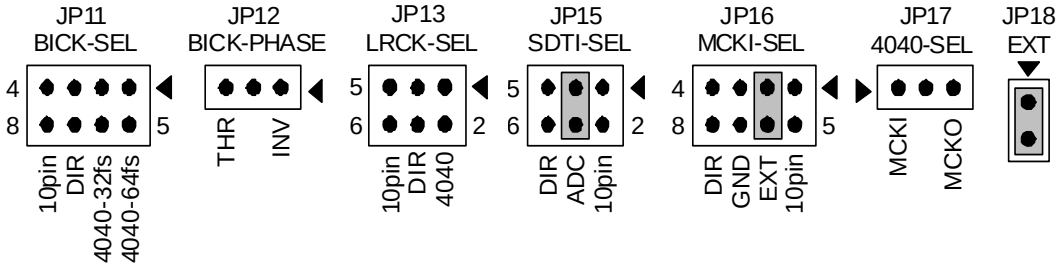


Figure 19.Setting of jumper pins with External Master Mode

Note 10.When a termination (51Ω) of J10 (EXT) is not used, JP18 (EXT) should be open.

(4-3) Setting with PLL Slave Mode.

SW4 (M/S) should be set to “ON (H)”.

(a) PLL Reference Clock: MCKI pin

J10 (EXT) is used (Note 11). Nothing should be connected to PORT1 (TORX), PORT2 (TOTX) and PORT3 (DSP).
MCKI is input from J10 (EXT). BICK and LRCK are generated by using on-board divider and MCKO of the AK4955. SDTI is connected to SDTO of the AK4955 as loopback.
In addition, registers of the AK4955 should be set to “PLL Slave Mode” (Reference Clock: MCKI pin).

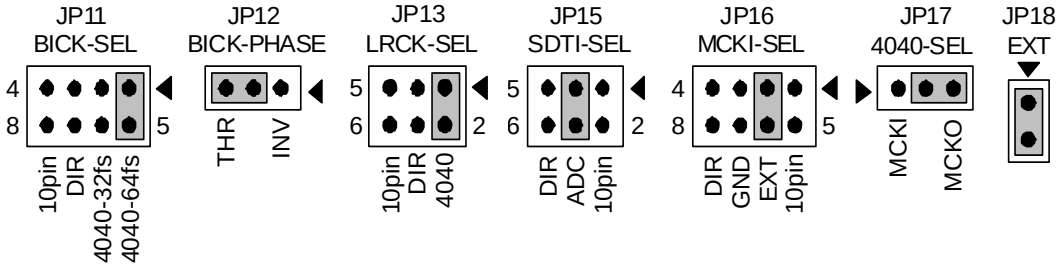


Figure 20.Setting of jumper pins with PLL Slave Mode (Note 12, Note 13)

Note 11.When a termination (51Ω) of J10 (EXT) is not used, JP18 (EXT) should be open.
Note 12.JP12 (BICK-PHASE) is jumper which decides polarity of BICK, “THR” or “INV” should be selected according to the Audio I/F format.
Note 13.When BICK of 32fs is used, JP11 (BICK-SEL) should be set to “4040-32fs” side.

(b) PLL Reference Clock: BICK pin

PORT3 (DSP) is used. Nothing should be connected to PORT1 (TORX), PORT2 (TOTX) and J10 (EXT).
BICK and LRCK are generated by on-board divider which used MCLK from PORT3 (DSP). SDTI is connected to SDTO of the AK4955 as loopback.
In addition, registers of the AK4955 should be set to “PLL Slave Mode” (Reference Clock: BICKI pin).

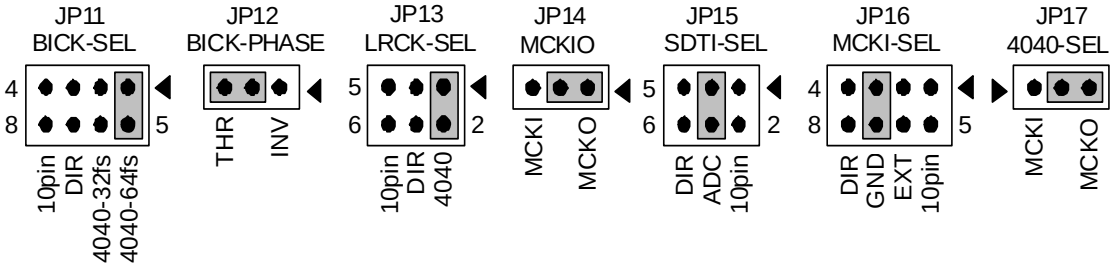


Figure 21.Setting of jumper pins with PLL Slave Mode (Note 14, Note 15)

Note 14.JP12 (BICK-PHASE) is jumper which decides polarity of BICK, “THR” or “INV” should be selected according to the Audio I/F format.
Note 15.When BICK of 32fs is used, JP11(BICK-SEL) should be set to “4040-32fs” side.

(4-4) Setting with PLL Master Mode.

J10 (EXT) is used (Note 16). Nothing should be connected to PORT1 (TORX), PORT2 (TOTX) and PORT3 (DSP).
MCKI is input from J10 (EXT), SDTI is connected to SDTO of the AK4955 as loopback.
SW4 (M/S) should be set to “OFF (L)”.

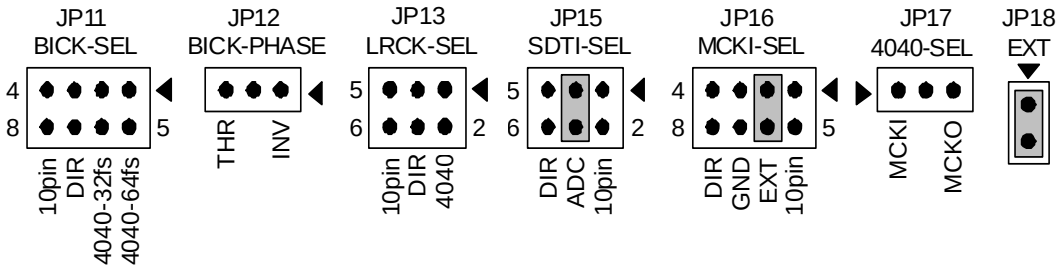


Figure 22.Setting of jumper pins with PLL Master Mode

Note 16.When a termination (51Ω) of J10 (EXT) is not used, JP18 (EXT) should be open.

3) Jumper pins and SW Setting.

(1) Setting of other jumper pins.

[JP6 (LIN-SEL)]: The selection of input signal to LIN1 pin and LIN2 pin.
- L1-mini : Input signal of LIN1 pin is supplied from J1 (AIN). < Default >
- L1-BNC : Input signal of LIN1 pin is supplied from J3 (LIN).
- L2-mini : Input signal of LIN2 pin is supplied from J1 (AIN).
- L2-BNC : Input signal of LIN2 pin is supplied from J3 (LIN). < Default >

[JP7 (RIN-SEL)]: The selection of input signal to RIN1 pin and RIN2 pin.
- R1-mini : Input signal of RIN1 pin is supplied from J1 (AIN). < Default >
- R1-BNC : Input signal of RIN1 pin is supplied from J5 (RIN).
- R2-mini : Input signal of RIN2 pin is supplied from J1 (AIN).
- R2-BNC : Input signal of RIN2 pin is supplied from J5 (RIN). < Default >

[JP8 (MIN-SEL)]: The selection of input mode of MIN pin.
- EXT : "External Resistance Mode".
- INT : "Internal Resistance Mode". < Default >

[JP9 (SPK-GND)]: The selection of condition for GND of J9 (SPK-OUT) connector.
- Short : Connect to GND. < Default >
- Open : None connect to GND.

[JP19 (GND)]: Analog ground and Digital ground
- Short : Common. (The connector "DGND" can be open.) < Default >
- Open : Separated.

[JP28 (CTRL-SEL)]: The selection of Serial Control I/F.
- USB : Use U10 (USB) connector. < Default >
- 10pin : Use PORT4 (10pin-CTRL).

[JP29 (PIC)]: Not to Use.

[JP100 (MPWR-SEL)]：The selection of MIC-power.
- OPEN : MIC-power is not supplied. < Default >
- SHORT : MIC-power is supplied.

[JP101 (RIN1-SEL)]：The selection of input signal to RIN1 pin.
- RIN1 : Connect to analog signal from JP7 (RIN-SEL). < Default >
- DMCLK : Connect to digital microphone clock supply input.

[JP102 (LIN1-SEL)]：The selection of input signal to LIN1 pin.
- LIN1 : Connect to analog signal from JP6 (LIN-SEL). < Default >
- DMDAT : Connect to digital microphone data input.

[JP103 (CDTIO/CAD0)]：The selection of input signal to CDTIO/CAD0 pin.
- CDTIO : When I2C pin = "L", CDTIO is selected. < Default >
- CAD0 : When I2C pin = "H", CAD0 is selected.

[JP104 (CSN/SDA)]：The selection of input signal to CSN/SDA pin.
- CSN : When I2C pin = "L", CSN is selected. < Default >
- SDA : When I2C pin = "H", SDA is selected.

(2) Setting of SW.

Upper-side is “ON(H)” and lower-side is “OFF(L)”.

[SW1] (SW DIP-4): Mode setting for AK4118A.

No.	Name	ON (“H”)	OFF (“L”)	Default
1	DIF2	See Table 4		ON
2	DIF1			OFF
3	DIF0			OFF
4	OCKS1	See Table 5		OFF

Table 3.Mode setting for AK4118A

Mode	DIF2	DIF1	DIF0	DAUX	SDTO	LRCK		BICK		
							I/O		I/O	
0	L	L	L	24bit, Left justified	16bit, Right justified	H/L	O	64fs	O	
1	L	L	H	24bit, Left justified	18bit, Right justified	H/L	O	64fs	O	
2	L	H	L	24bit, Left justified	20bit, Right justified	H/L	O	64fs	O	
3	L	H	H	24bit, Left justified	24bit, Right justified	H/L	O	64fs	O	
4	H	L	L	24bit, Left justified	24bit, Left justified	H/L	O	64fs	O	Default
5	H	L	H	24bit, I^2S	24bit, I^2S	L/H	O	64fs	O	
6	H	H	L	24bit, Left justified	24bit, Left justified	H/L	I	64 -128fs	I	
7	H	H	H	24bit, I^2S	24bit, I^2S	L/H	I	64 -128fs	I	

Table 4.Audio I/F Format Setting for AK4118A

OCKS1	MCKO1	
L	256fs	Default
H	512fs	

Table 5.Master Clock setting for AK4118A

[SW4] (SW DIP-3): Mode setting for AK4955.

No.	Name	ON (“H”)	OFF (“L”)	Default
1	I2C	I^2C Bus	3-Wire Serial	OFF
2	CAD0	CAD0 pin = “1”	CAD0 pin = “0”	OFF
3	M/S	When the AK4955 is in “Slave Mode”.	When the AK4955 is in “Master Mode”.	ON

Table 6.Mode setting for AK4955

4) Power on.

Upper-side is “H” and lower-side is “L”.

[SW2] (DIO-PDN) : Resets the AK4118A. Keep “H” during normal operation.
The AK4118A should be resets once bringing “L” upon power-up.

[SW3] (PDN) : Resets the AK4955. Keep “H” during normal operation.
The AK4955 should be resets once bringing “L” upon power-up.

■ Indication for LED

[LED1] (INT0) : Monitor INT0 pin of the AK4118A.
LED turns on when some error has occurred to AK4118A.

■ Control Port

It is possible to control AKD4955-A via general USB port. Connect cable with the U10 (USB) on board and PC. Control software is packed with this board. The software operation sequence is included in the evaluation board manual.

■ Analog Input / Output Circuits

1) Input circuit

(1-1) MIC/LINE1, 2 input circuit (except for Digital-MIC circuit).

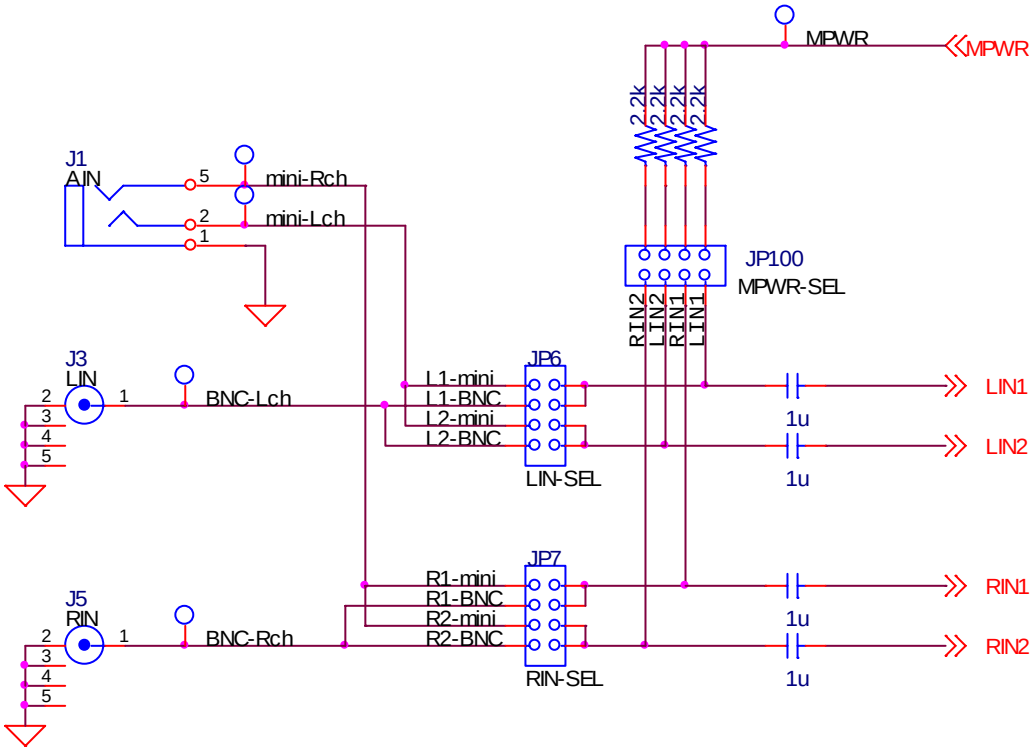


Figure 23.Circuit diagram of MIC/LIN1, 2 input

The MIC/LINE1, 2 inputs are shared with J1, J3 and J5.
Please select the input to be used with JP6 (LIN-SEL) and JP7 (RIN-SEL).

(1-2) Video input circuit.

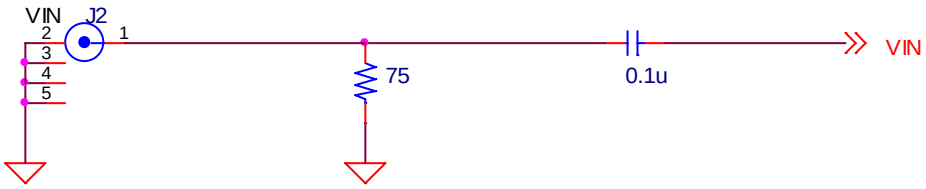


Figure 24.Circuit diagram of Video input

(1-3) Monaural input circuit.

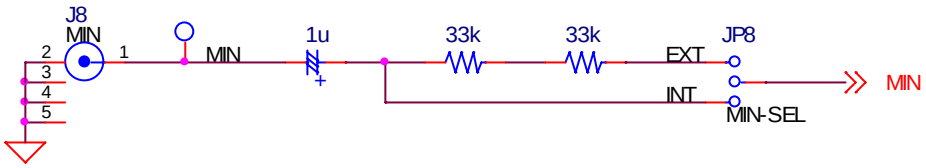


Figure 25.Circuit diagram of Monaural input

2) Output circuit

(2-1) LINE output circuit.

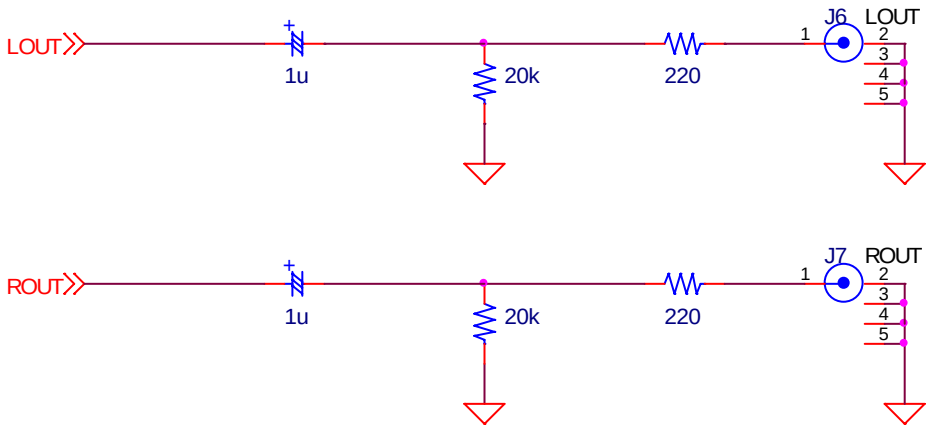


Figure 26.Circuit diagram of LINE output

(2-2) Video output circuit.

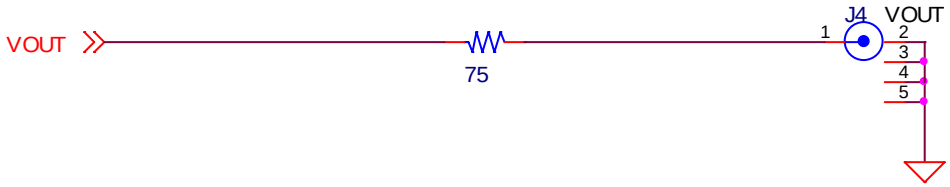


Figure 27.Circuit diagram of Video output

(2-3) Speaker output circuit.

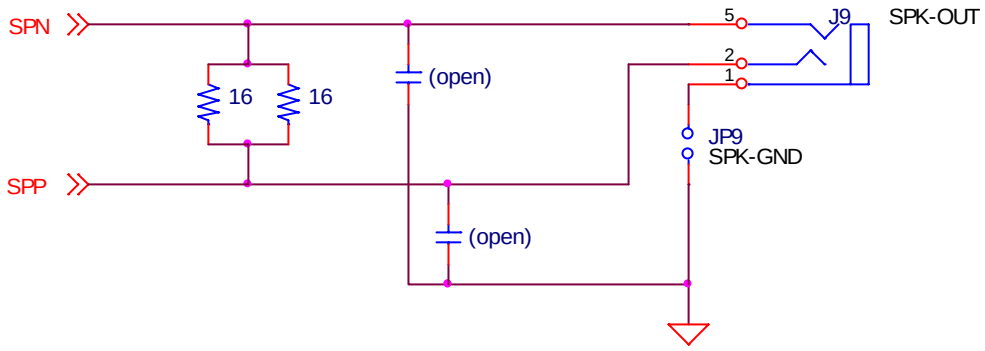


Figure 28.Circuit diagram of Speaker output

Control Soft Manual

■ Evaluation Board and Control Soft Settings

1. Set an evaluation board properly.
2. Connect a PC and an evaluation board.
3. The USB control is recognized as HID (Human Interface Device) on the PC.
   It is not necessary to install a new driver.
4. Start up the control program. (Note 17)

Note 17. **The AK4955 should be reset by the PDN pin after the power supplies are applied.**
After that, "Dummy Command" should be executed.

5. Proceed evaluation by following the process below.

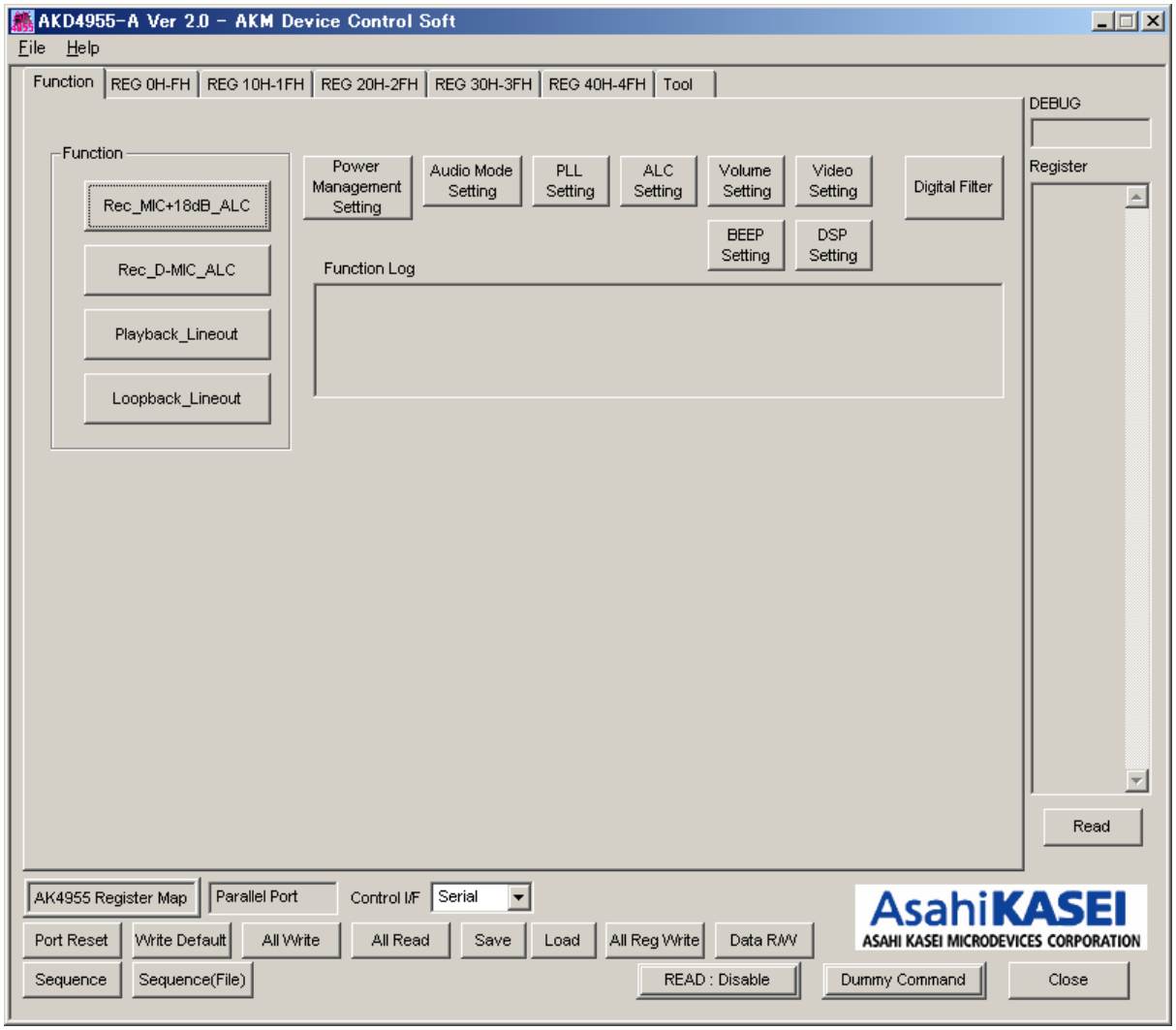


Figure 29. Window of Control Soft

■ Operation Overview

Function, register map and testing tool can be controlled by this control soft. These controls are selected by upper tabs.

Buttons which are frequently used such as register initializing button “Write Default”, are located outside of the switching tab window. Refer to the “■ Dialog Boxes” for details of each dialog box setting.

1. [Port Reset]: Click this button after the control soft starts up.

2. [Write Default]: Initializes Registers
   When the device is reset by a hardware reset, use this button to initialize the registers.

3. [All Write]: Executes write commands for all registers displayed.

4. [All Read]: Executes read commands for all registers displayed.

5. [Save]: Saves current register settings to a file.

6. [Load]: Executes data write from a saved file.

7. [All Req Write]: Opens “All Req Write” dialog box.

8. [Data R/W]: Opens “Data R/W” dialog box

9. [Sequence]: Opens “Sequence” dialog box.

10. [Sequence(File)]: Opens “Sequence(File)” dialog box.

11. [Read]: Reads current register settings and displays on to the register area (on the right of the main window). This is different from [All Read] button, it does not reflect to a register map, only displaying register settings in hexadecimal.

12. [READ:Disable/Enable]: The register setting of [READ].

    READ: Read function enable.
    0: Disable < Default >
    1: Enable

13. [Dummy Command]: The dummy command is written (Note 18).

Note 18. **The AK4955 should be reset by the PDN pin after the power supplies are applied. After that, “Dummy Command” should be executed.**

■ Tab Functions

1. [Function]: Function control

This tab is for function.
Each operation is executed by [Function] buttons on the left side of the screen (Note 19, Note 20).

Note 19. Please refer to the following setting when you use the "Function" function.

Mode= "External Slave Mode", fs= "7.35kHz～48kHz", Audio I/F Format= "24bit MSB justified"

Note 20. **The AK4955 should be reset by the PDN pin after the power supplies are applied.**
After that, "Dummy Command" should be executed.

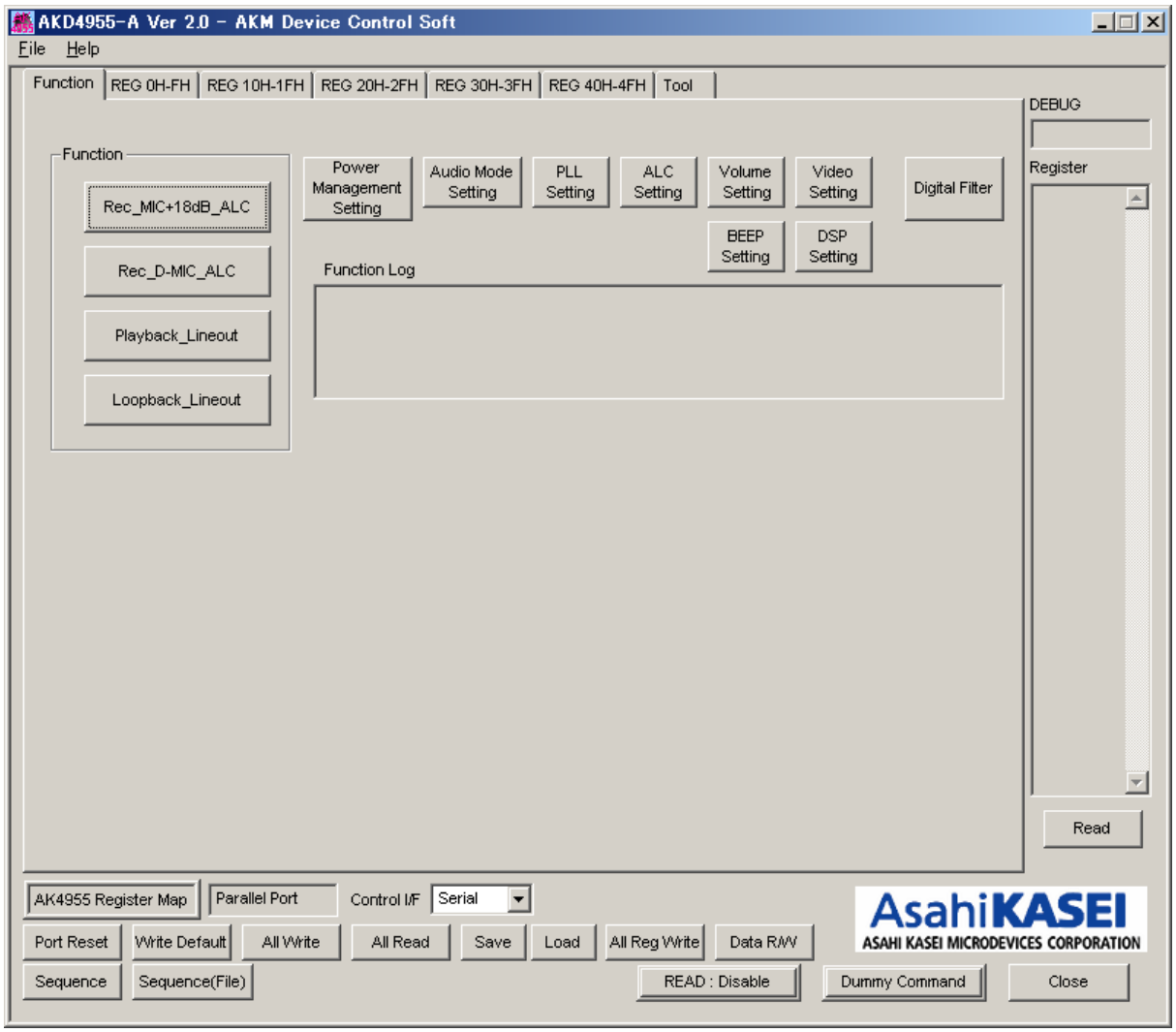


Figure 30.Window of [Function]

2. [REG]: Register Map

This tab is for a register writing and reading.

Each bit on the register map is a push-button switch.
Button Down indicates “H” or “1” and the bit name is in red (when read only it is in deep red).
Button Up indicates “L” or “0” and the bit name is in blue (when read only it is in gray).

Gray-out registers are Read only registers. They can not be controlled.

The registers which is not defined in the datasheet are indicated as “---”.

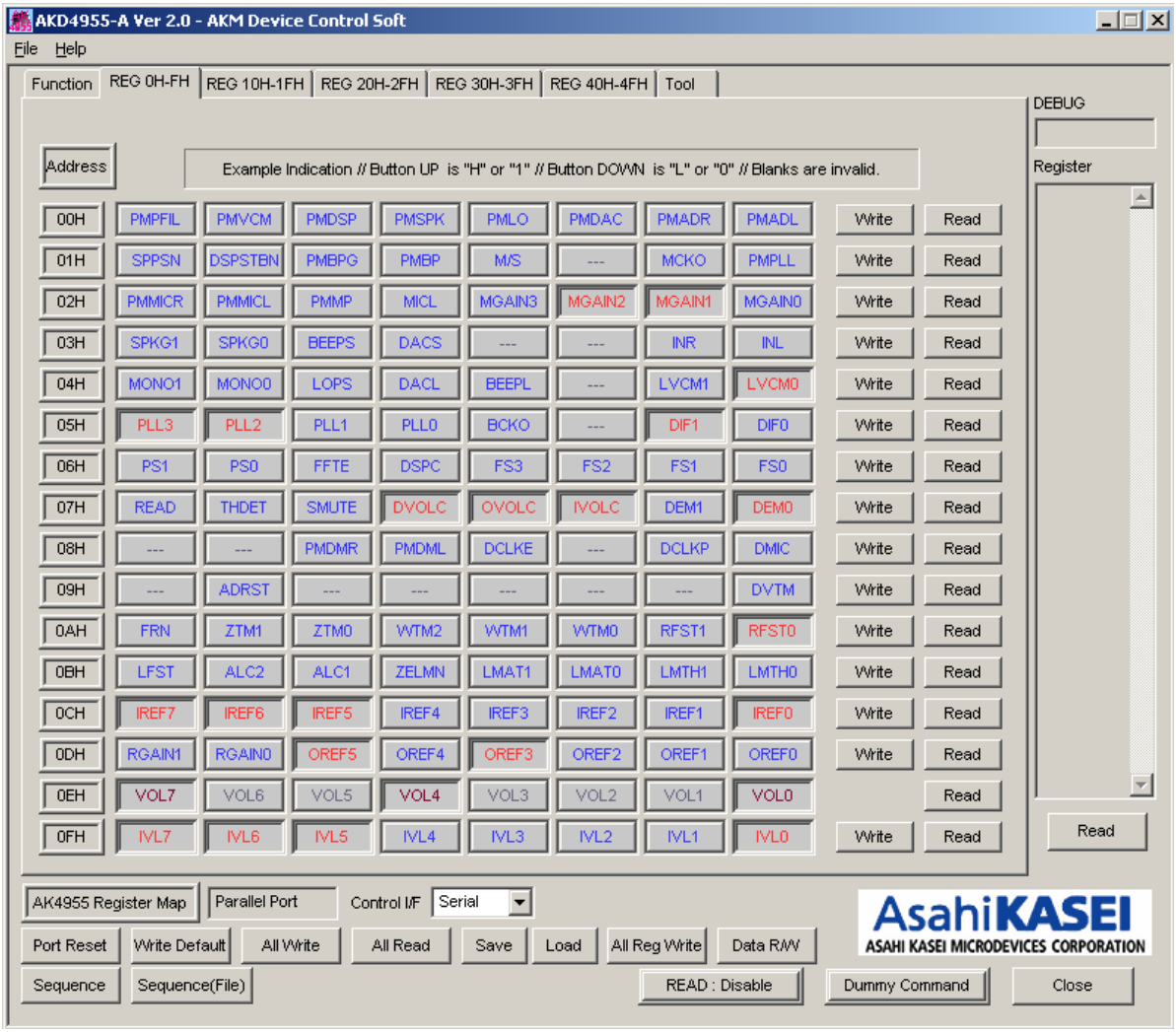


Figure 31.Window of [REG]

2-1. [Write]: Data Writing Dialog

It is for when changing two or more bits on the same address at the same time.
Click [Write] button located on the right of the each corresponded address for a pop-up dialog box.
When the checkbox is checked, the data will be “H” or “1”. When the checkbox is not checked, the data will be “L” or “0”. Click [OK] to write setting values to the registers, or click [Cancel] to cancel this setting.

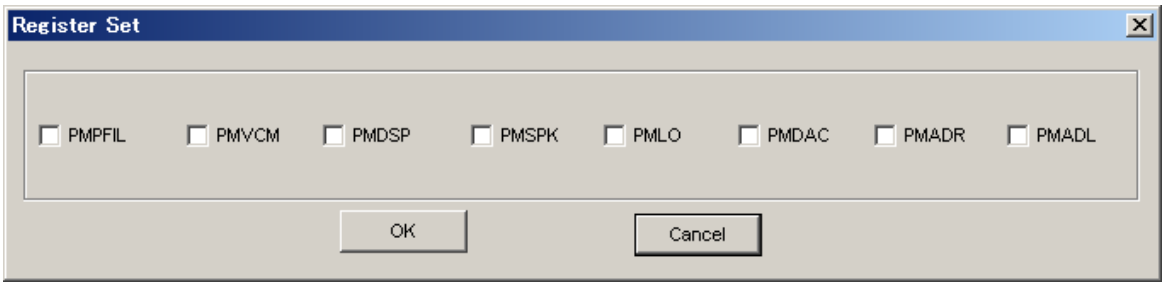


Figure 32.Window of [Register Set]

2-2. [Read]: Data Read

Click [Read] button located on the right of the each corresponded address to execute a register read.
After register reading, the display will be updated regarding to the register status.
Button Down indicates “H” or “1” and the bit name is in red (when read only it is in deep red).
Button Up indicates “L” or “0” and the bit name is in blue (when read only it is in gray).
Please be aware that button statuses will be changed by a Read command.

3. [Tool]: Testing Tools

Evaluation testing tools are available in this tab.
Click buttons for each testing tool.

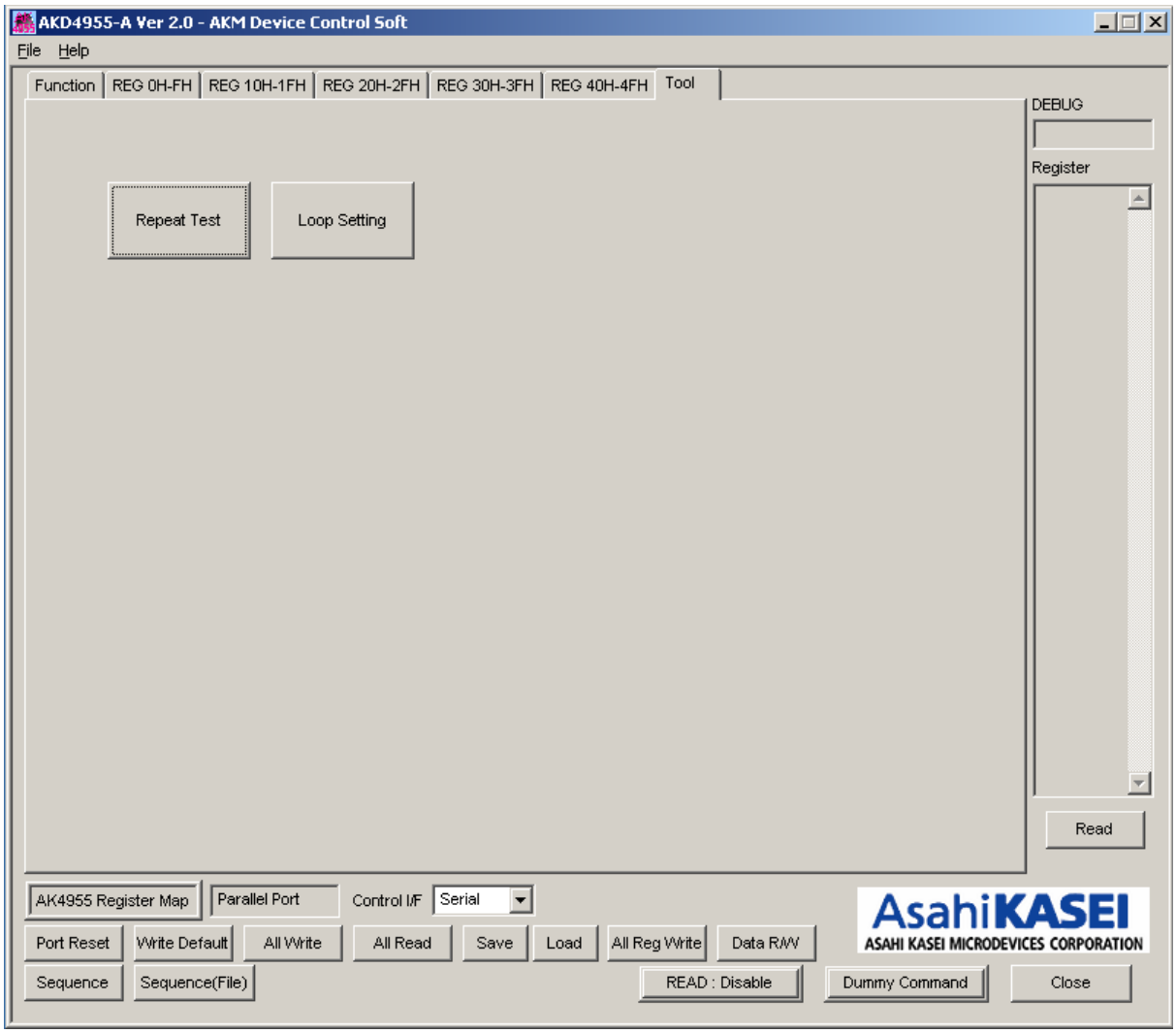


Figure 33.Window of [Tool]

3-1. [Repeat Test]: Repeat Test Dialog

Click [Repeat Test] button in the Test tab to open a repeat test dialog shown below.
Repeat writing test can be executed by this dialog.

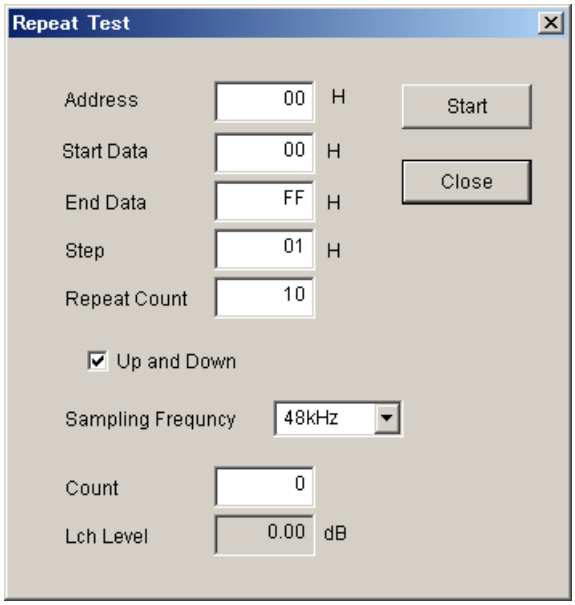


Figure 34.Window of [Repeat Test]

[Start] Button : Starts the repeat test.
A dialog for saving a file of the test result will open when clicking this button.
Name the file.
Test will start after specifying a saving file.
[Close] Button : Closes this dialog and finishes the process.
[Address] Box : Data writing address in hexadecimal numbers.
[Start Data] Box : Start data in hexadecimal numbers.
[End Data] Box : End data in hexadecimal numbers.
[Step] Box : Data write step interval.
[Repeat Count] Box : Repeat count of the test writing.
[Up and Down] Box : Data write flow is changed as below.

- Checked : Writes in step interval from the start data to the end data and turn back from the end data to the start data.
  [Example] Start Data = 00, End Data = 05, Step = 1, [ ]…for 1 count.
  Data flow : [00→01→02→03→04→05→05→04→03→02→01→00] x Repeat Count Number

- Not checked : Writes in step interval from the start data to the end data and finishes writing.
  [Example] Start Data = 00, End Data = 05, Step = 1, [ ]…for 1 count.
  Data flow : [00→01→02→03→04→05] x Repeat Count Number

[Sampling Frequency] Box : Selects sampling frequency 44.1 kHz/48 kHz
[Count] Box : Indicates the count number during a repeat test.
[Lch Level] Box : Indicates the Lch Level during a repeat test.

3-2. [Loop Setting]: Loop Dialog

Click [Loop Setting] button in the Tool tab to open loop setting dialog as shown below.
Writing test can be executed.

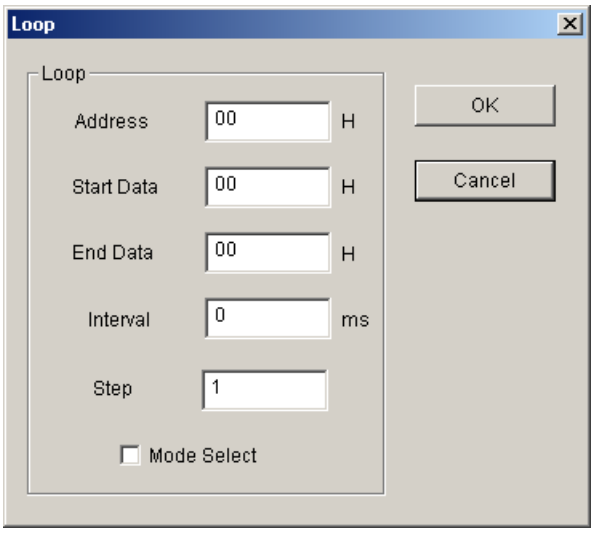


Figure 35.Window of [Loop]

[OK] Button : Starts the test.
[Cancel] Button : Closes the dialog and finishes the process.
[Address] Box : Data writing address in hexadecimal numbers.
[Start Data] Box : Start data in hexadecimal numbers.
[End Data] Box : End data in hexadecimal numbers.
[Interval] Box : Data write interval time.
[Step] Box : Data write step interval.
[Mode Select] Box : Mode select check box.

• Checked : Writes in step interval from the start data to the end data and turn back from the end data to the start data.
[Example] Start Data = 00, End Data = 05, Step = 1
Data flow : 00→01→02→03→04→05→05→04→03→02→01→00

• Not Checked : Writes in step interval from the start data to the end data and finishes writing.
[Example] Start Data = 00, End Data = 05, Step = 1
Data flow : 00→01→02→03→04→05

■ Dialog Boxes

1. [All Req Write]: All Reg Write dialog box

Click [All Reg Write] button in the main window to open register setting files.
Register setting files saved by [SAVE] button can be applied.

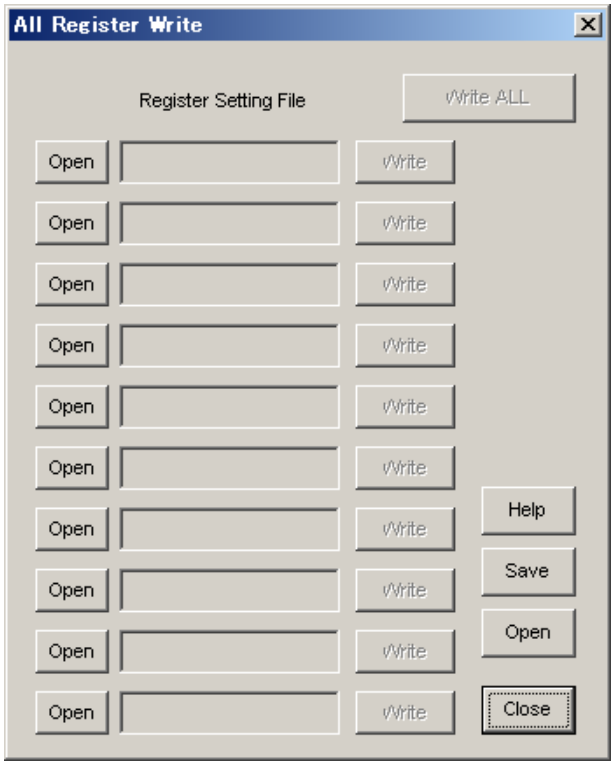


Figure 36.Window of [All Reg Write]

[Open (left)] : Selects a register setting file (*.akr).
[Write] : Executes register writing by the setting of selected file.
[Write All] : Executes all register writings.
Selected files are executed in descending order.

[Help] : Opens a help window.
[Save] : Saves a register setting file assignment. The file name is "*.mar".
[Open (right)]: Opens a saved register setting file assignment "*. mar".
[Close] : Closes the dialog box and finish the process.

~ Operating Suggestions ~

1. Those files saved by [Save] button and opened by [Open] button on the right of the dialog "*.mar" should be stored in the same folder.
2. When register settings are changed by [Save] button in the main window, re-read the file to reflect new register settings.

2. [Data R/W]: Data R/W Dialog Box

Click the [Data R/W] button in the main window for data read/write dialog box.
Data write is available to specified address.

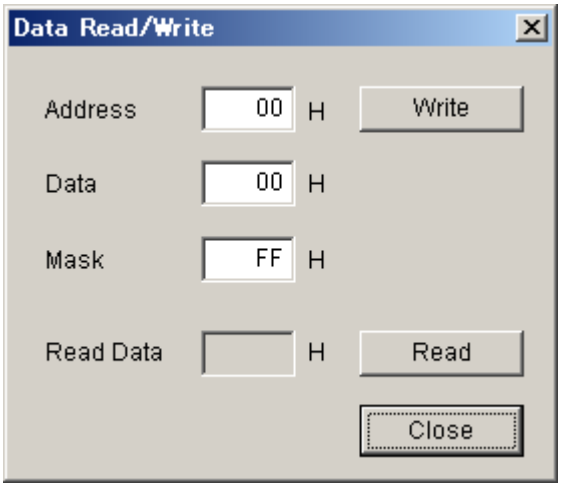


Figure 37.Window of [Data R/W]

[Address] Box : Input data address in hexadecimal numbers for data writing.
[Data] Box : Input data in hexadecimal numbers.
[Mask] Box : Input masks data in hexadecimal numbers.
This is "AND" processed input data.
[Write] : Writs the data generated from Data and Mask values to the address specified by "Address" box (Note 21).
[Read] : Reads data from the address specified by "Address" box (Note 21).
The result will be shown in the Read Data Box in hexadecimal numbers.
[Close] : Closes the dialog box and finishes the process.
Data writing can be cancelled by this button instead of executing a write command.

Note 21.The register map will be updated after executing [Write] or [Read] commands.

3. [Sequence]: Sequence Dialog Box

Click [Sequence] button to open register sequence setting dialog box.
Register sequence can be set in this dialog box.

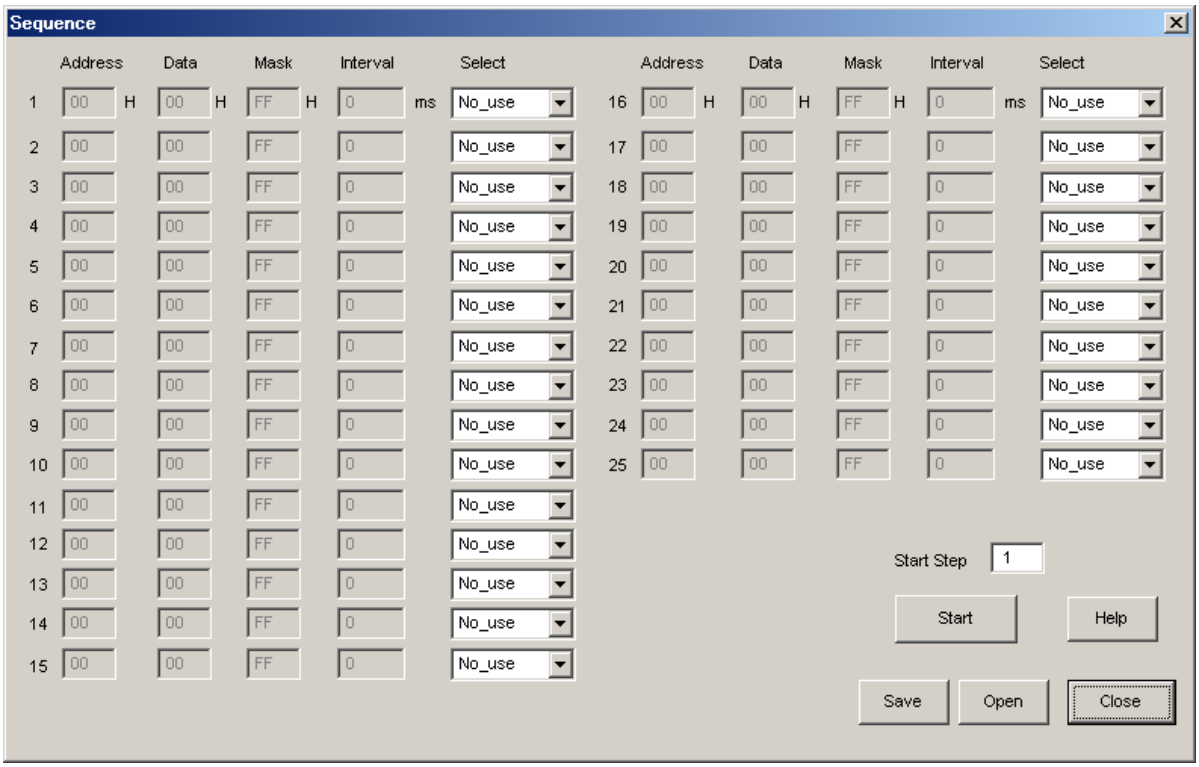


Figure 38.Window of [Sequence]

~ Sequence Setting ~

Set register sequence by following process bellow.

1. Select a command
   Use [Select] pull-down box to choose commands.
   Corresponding boxes will be valid.

   < Select Pull-down menu >
   - · No_use: Not using this address
   - · Register: Register writing
   - · Reg(Mask): Register writing (Masked)
   - · Interval: Taking an interval
   - · Stop: Pausing the sequence
   - · End: Finishing the sequence

2. Input sequence
   [Address] : Data address
   [Data] : Writing data
   [Mask] : Mask
   [Data] box data is ANDed with [Mask] box data. This is the actual writing data.
   When Mask = 0x00, current setting is hold.
   When Mask = 0xFF, the 8bit data which is set in the [Data] box is written.
   When Mask =0x0F, lower 4bit data which is set in the [Data] box is written.
   Upper 4bit is hold to current setting.
   [Interval] : Interval time

   Valid boxes for each process command are shown bellow.

   · No_use : None
   · Register : [Address], [Data], [Interval]
   · Reg(Mask) : [Address], [Data], [Mask], [Interval]
   · Interval : [Interval]
   · Stop : None
   · End : None

~ Control Buttons~

The function of Control Button is shown bellow.

[Start] : Executes the sequence
[Help] : Opens a help window
[Save] : Saves sequence settings as a file. The file name is "*.aks".
[Open] : Opens a sequence setting file "*.aks".
[Close] : Closes the dialog box and finishes the process.

~ Stop of the sequence~

When "Stop" is selected in the sequence, the process is paused and it starts again when [Start] button is clicked Restarting step number is shown in the "Start Step" box. When finishing the process at the end of sequence, "Start Step" will return to "1".

The sequence can be started from any step by writing the step number to the "Start Step" box.
Write "1" to the "Start Step" box and click [Start] button, when restarting the process from the beginning.

4. [Sequence(File)]: Sequence Setting File Dialog Box

Click [Sequence(File)] button to open sequence setting file dialog box.
Those files saved in the "Sequence setting dialog" can be applied in this dialog.

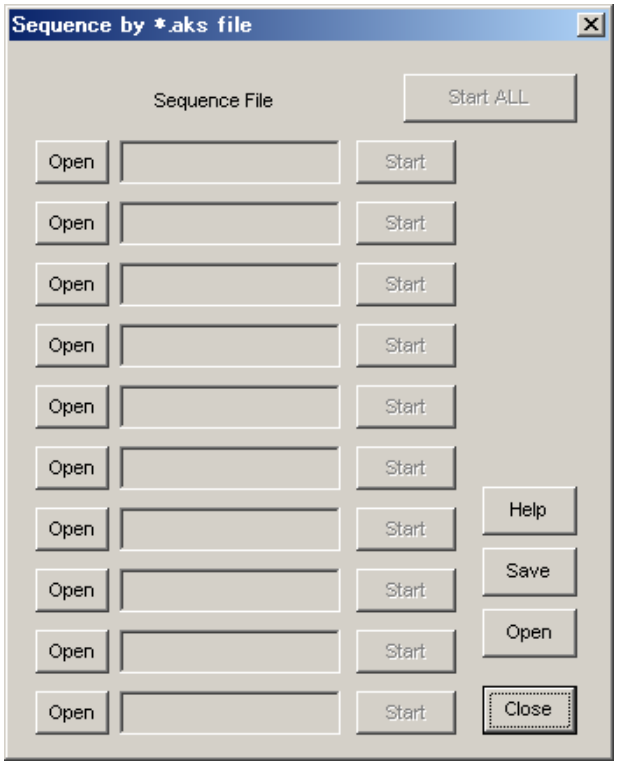


Figure 39.Window of [Sequence(File)]

[Open (left)] : Opens a sequence setting file (*.aks).
[Start] : Executes the sequence by the setting of selected file.
[Start All] : Executing all sequence settings.
Selected files are executed in descending order.
[Help] : Opens a help window.
[Save] : Saves a sequence setting file assignment. The file name is "*.mas".
[Open(right)] : Opens a saved sequence setting file assignment "*. mas".
[Close] : Closes the dialog box and finishes the process.

~ Operating Suggestions ~

1. Those files saved by [Save] button and opened by [Open] button on the right of the dialog "*.mas" should be stored in the same folder.
2. When "Stop" is selected in the sequence the process will be paused and a pop-up message will appear. Click "OK" to continue the process.

Figure 40.Window of [Sequence Pause]

5. [Power Management Setting]: Power Management Setting Dialog Box

When [Power Management Setting] button is clicked, the window as shown in Figure 41 opens.
Refer to the datasheet for register settings of the AK4955.

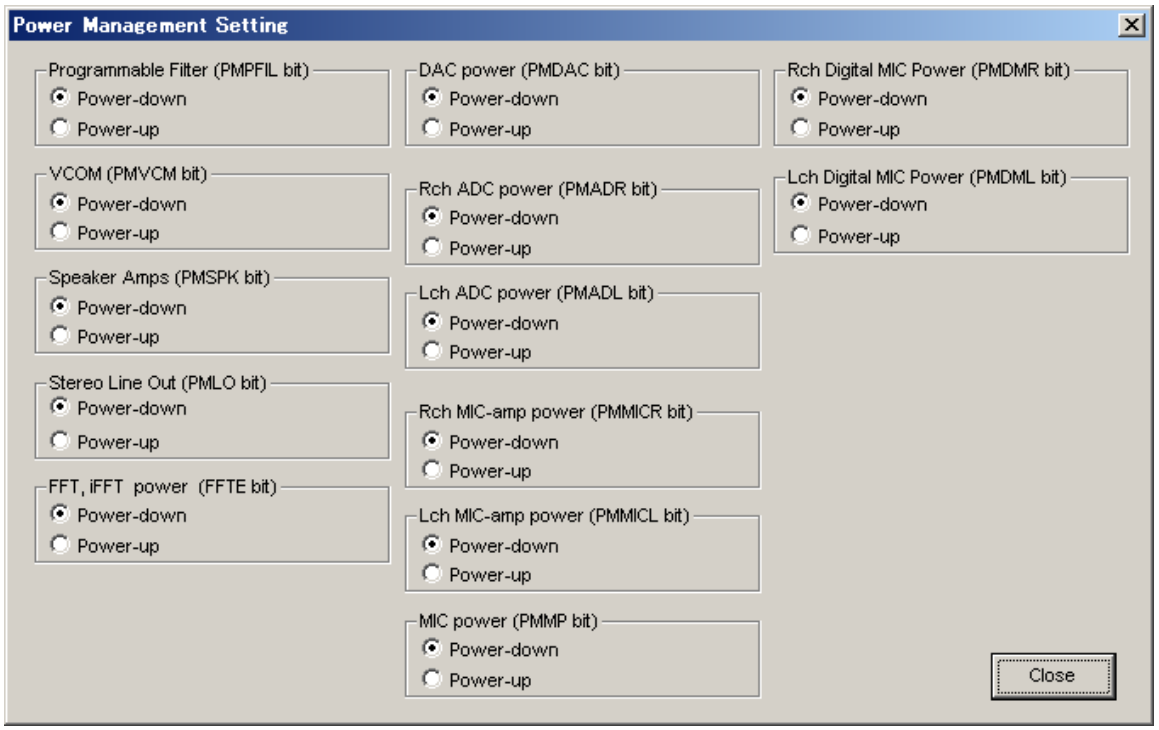


Figure 41.Window of [Power Management Setting]

6. [Audio Mode Setting]: Audio Mode Setting Dialog Box

When [Audio Mode Setting] button is clicked, the window as shown in Figure 42 opens.
Refer to the datasheet for register settings of the AK4955.

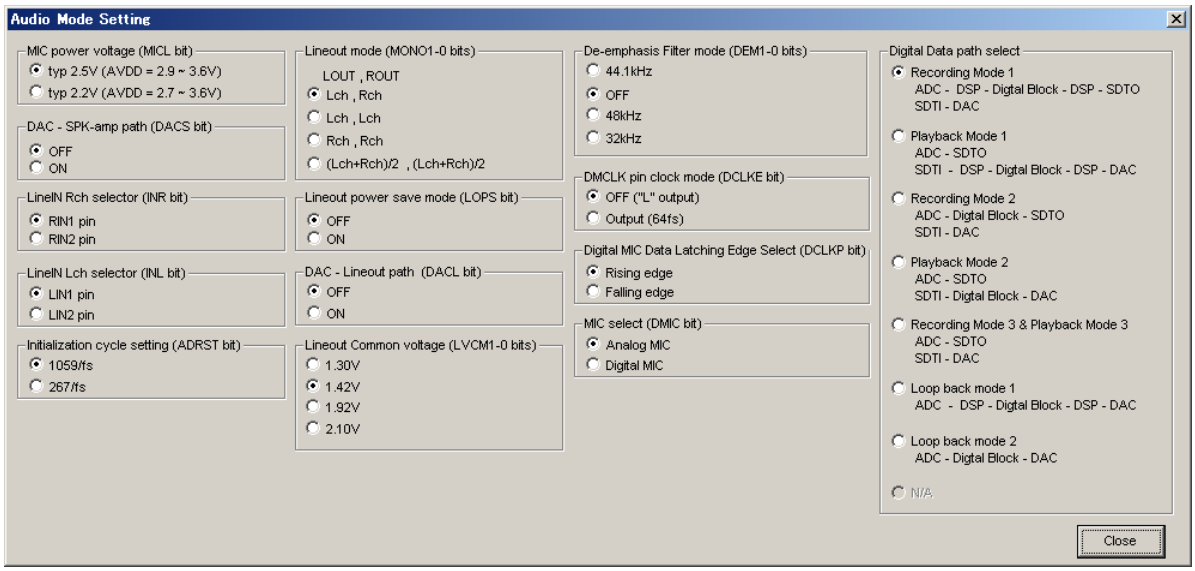


Figure 42.Window of [Audio Mode Setting]

7. [PLL Setting]: PLL Setting Dialog Box

When [PLL Setting] button is clicked, the window as shown in Figure 43 opens.
Refer to the datasheet for register settings of the AK4955.

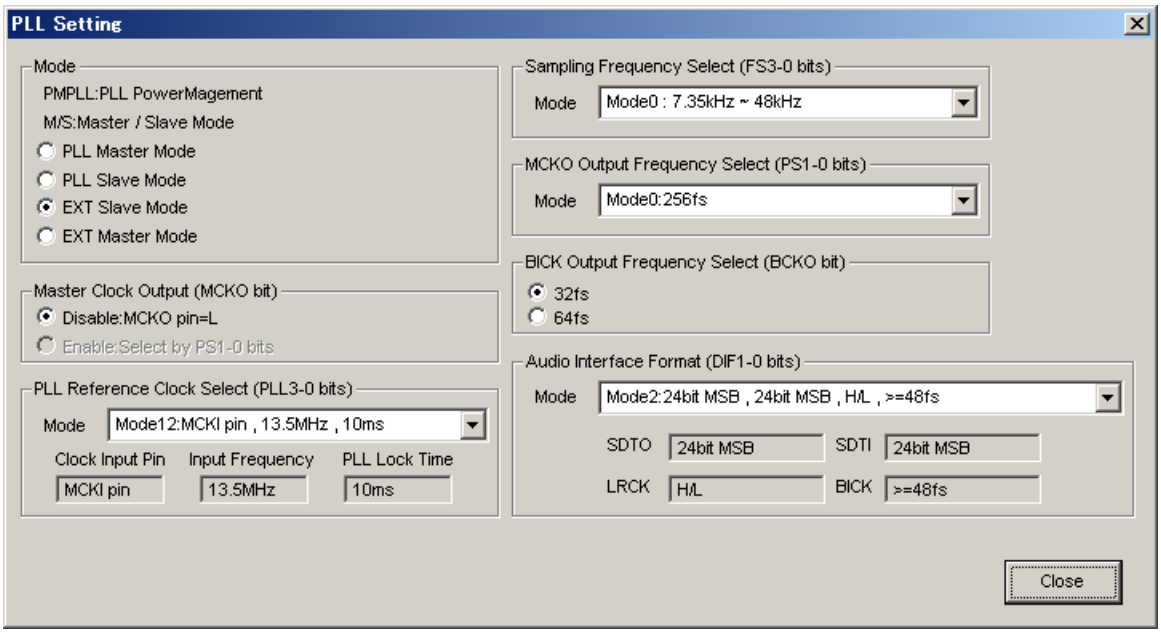


Figure 43.Window of [PLL Setting]

8. [ALC Setting]: ALC Setting Dialog Box

When [ALC Setting] button is clicked, the window as shown in Figure 44 opens.
Refer to the datasheet for register settings of the AK4955.

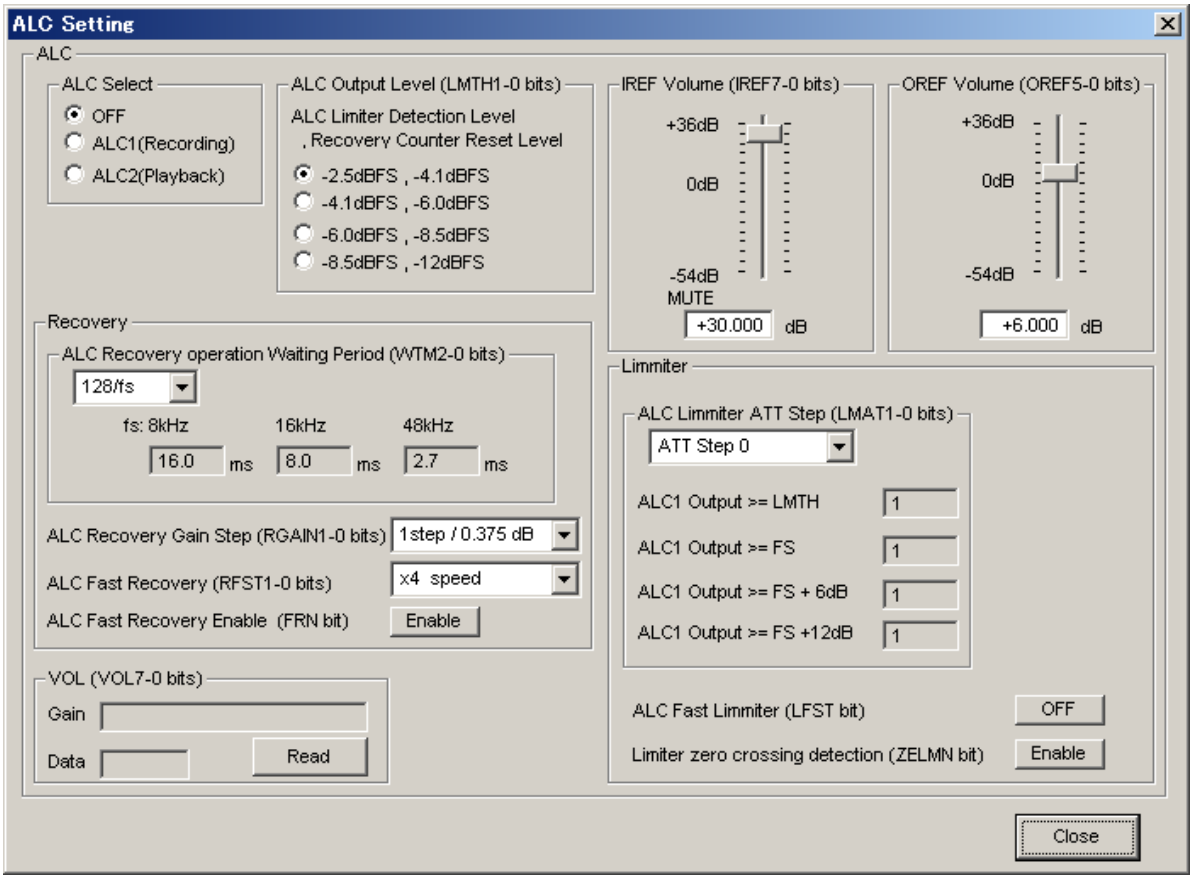


Figure 44.Window of [ALC Setting]

[VOL Read]: When the button is pushed, reading “VOL” register is executed.

Gain: Current volume is displayed in 1.5dB step based on the reading result of the VOL register value.
Data: The VOL register value is displayed. (HEX)

9. [Volume Setting]: Volume Setting Dialog Box

When [Volume Setting] button is clicked, the window as shown in Figure 45 opens.
Refer to the datasheet for register settings of the AK4955.

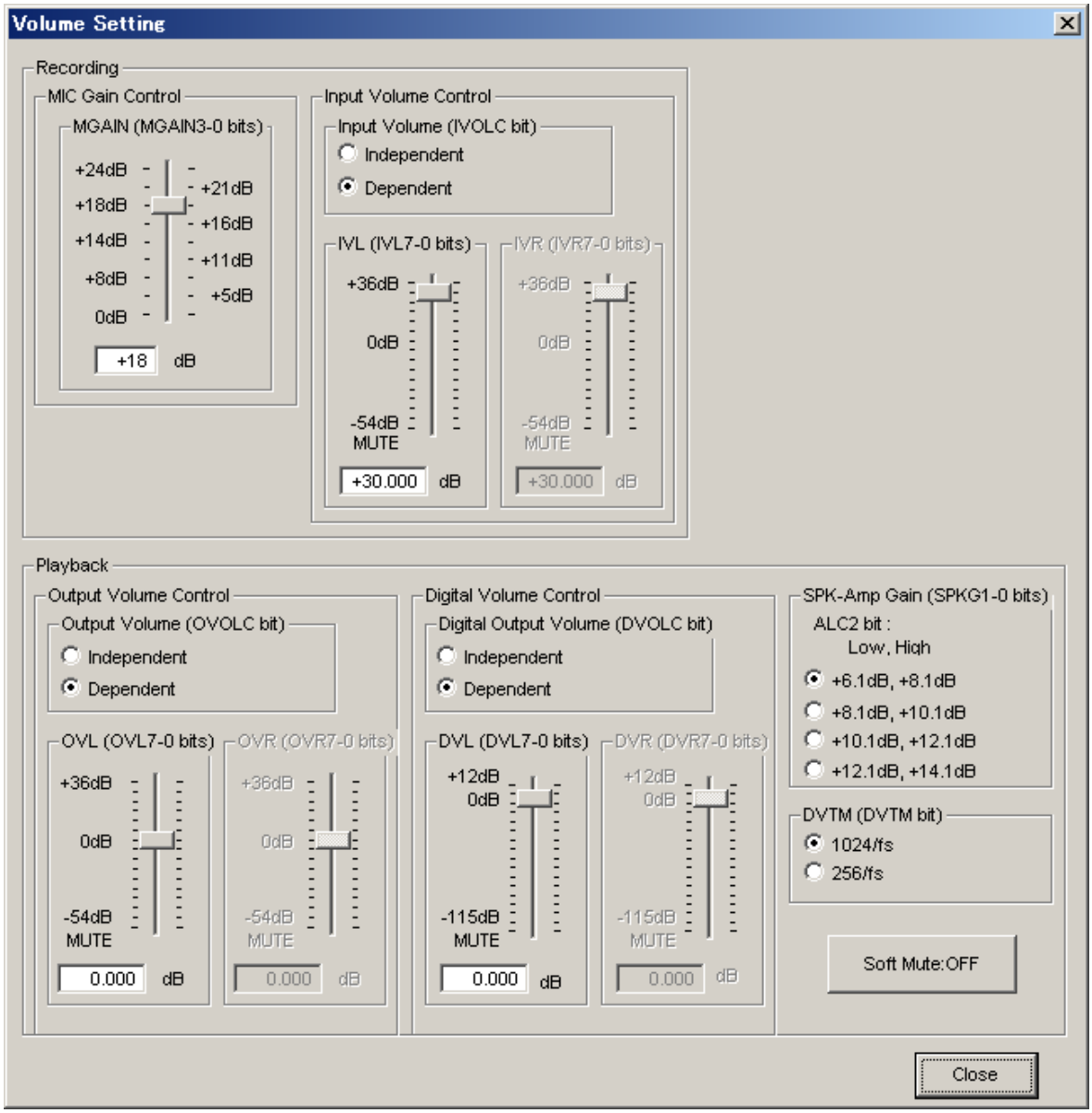


Figure 45.Window of [Volume Setting]

Volume Control by Slider Menu

The volume can also be changed by writing a value in a dialog box.
The slide bar is moved to the value that written in the dialog box.
The up and down arrow keys to mouse or keyboard to adjust the settings.

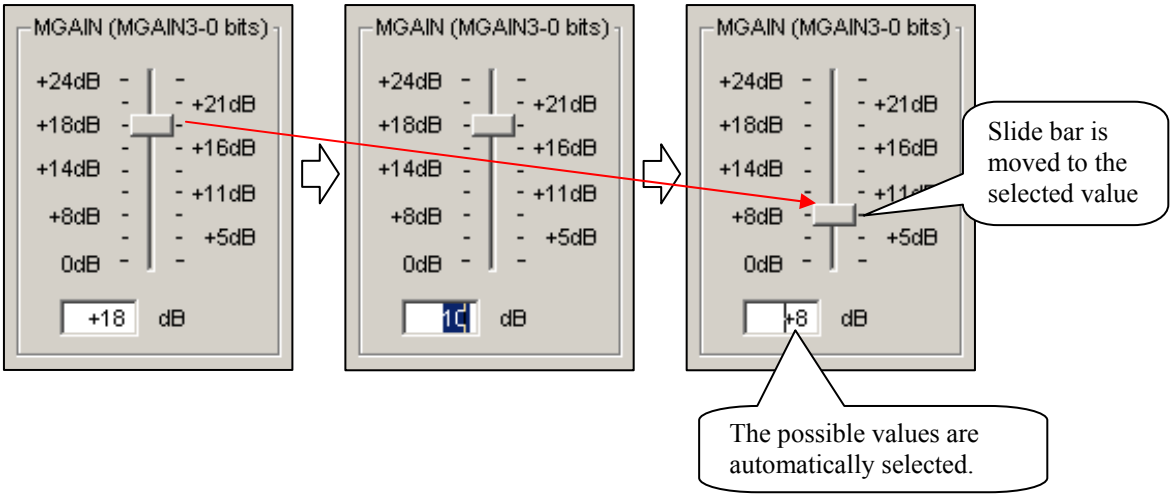


Figure 46.Volume Slider

10. [Video Setting]: Video Setting Dialog Box

When [Video Setting] button is clicked, the window as shown in Figure 47 opens.
Refer to the datasheet for register settings of the AK4955.

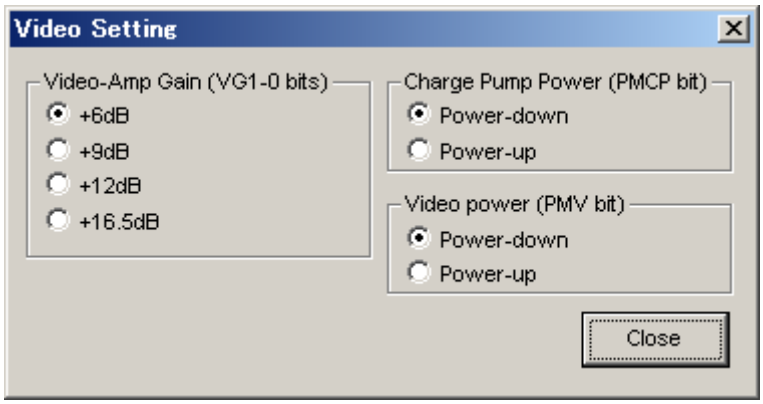


Figure 47.Window of [Video Setting]

11. [BEEP Setting]: BEEP Setting Dialog Box

When [BEEP Setting] button is clicked, the window as shown in Figure 48 opens.
Refer to the datasheet for register settings of the AK4955.

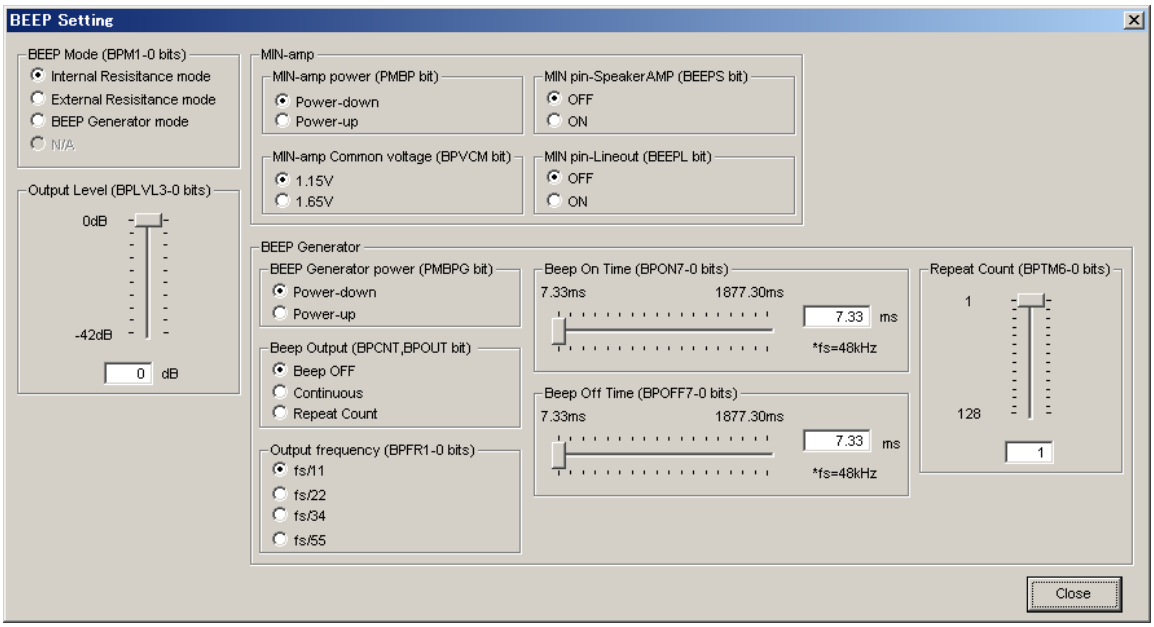


Figure 48.Window of [BEEP Setting]

12. [DSP Setting]: DSP Setting Dialog Box

When [DSP Setting] button is clicked, the window as shown in Figure 49 opens.
Refer to the datasheet for register settings of the AK4955.

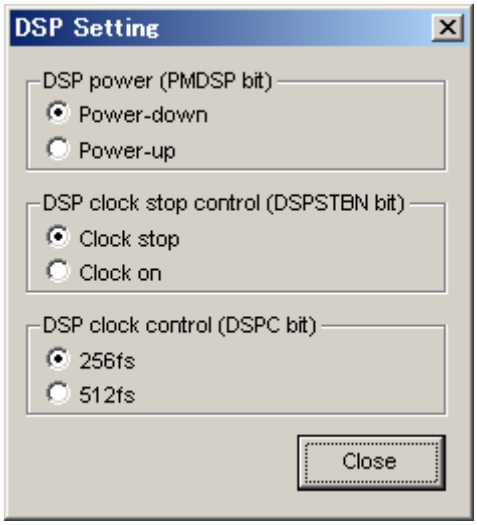


Figure 49.Window of [DSP Setting]

13. [Digital Filter]: Filter Setting Dialog Box

When [Digital Filter] button is clicked, the window as shown in Figure 50 opens.
Refer to the datasheet for register settings of the AK4955.

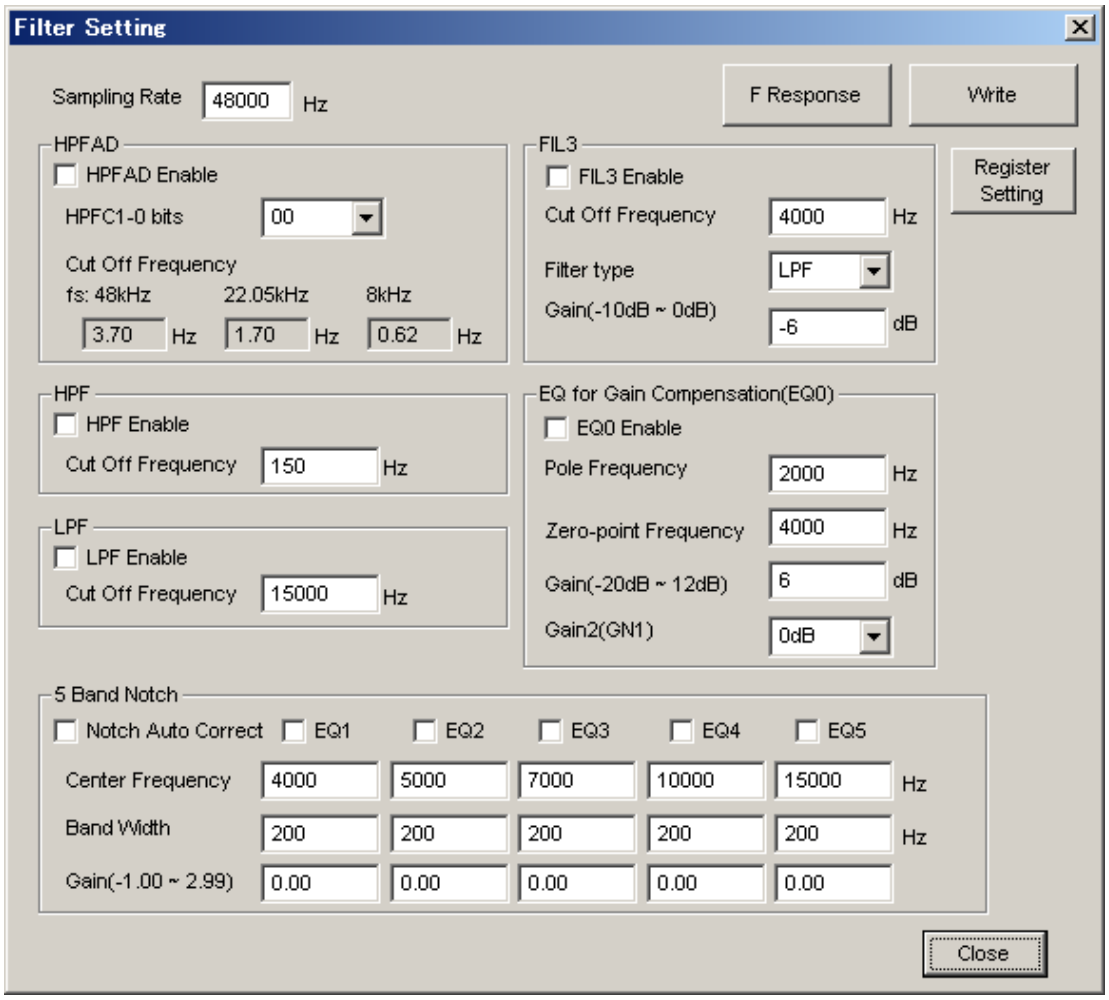


Figure 50.Window of [Filter Setting]

[F Response] : The filter characteristic dialog is displayed.
[Write] : The calculation of all filters and writing the coefficient are executed.
[Register Setting] : "Register Setting for Filter" dialog box is popped up.
[Close] : Closing the dialog box and finish the process.

13-1. Parameter Setting

(1) Please set a parameter of each Filter.

Parameter	Function	Setting Range
Sampling Rate	Sampling frequency (fs)	7350Hz ≤ fs ≤ 48000Hz
HPF		
Cut Off Frequency	High pass filter cut off frequency	fs/10000 ≤ Cut Off Frequency ≤ (0.497 * fs)
LPF		
Cut Off Frequency	Low pass filter cut off frequency	fs/20 ≤ Cut Off Frequency ≤ (0.497 * fs)
FIL3		
Cut Off Frequency	FIL3 cut off frequency	fs/10000 ≤ Cut Off Frequency ≤ (0.497 * fs)
Filter type	The selection of filter type	LPF or HPF
Gain	Gain	-10 ≤ Gain < 0 dB
EQ0		
Pole Frequency	EQ0 Pole Frequency	fs/10000 ≤ Cut Off Frequency ≤ (0.497 * fs)
Zero-point Frequency	EQ0 Zero-point Frequency	fs/10000 ≤ Cut Off Frequency ≤ (0.497 * fs)
Gain	Gain	-20 ≤ Gain < +12 dB
Gain2	Gain2	0 / +12 / +24 dB
5 Band Equalizer		
EQ1-5 Center Frequency	EQ1-5 Center Frequency	0Hz ≤ Center Frequency < (0.497 * fs)
EQ1-5 Band Width	EQ1-5 Band Width (Note 22)	1Hz ≤ Band Width < (0.497 * fs)
EQ1-5 Gain	EQ1-5 Gain (Note 23)	-1 ≤ Gain < 3

Table 7.Parameter setting of [Filter Setting]

Note 22.A gain difference is a bandwidth of 3dB from center frequency.
Note 23.When a gain is "-1", EQ becomes a notch filter.

(2) "LPF Enable", "HPF Enable", "HPFAD Enable", "FIL3 Enable", "EQ0 Enable", "EQ1", "EQ2", "EQ3", "EQ4", "EQ5" Please set ON/OFF of Filter with a check button. When checked it, Filter becomes ON. When "Notch Filter Auto Correction" is checked, perform automatic correction of the center frequency of the notch filter is executed.

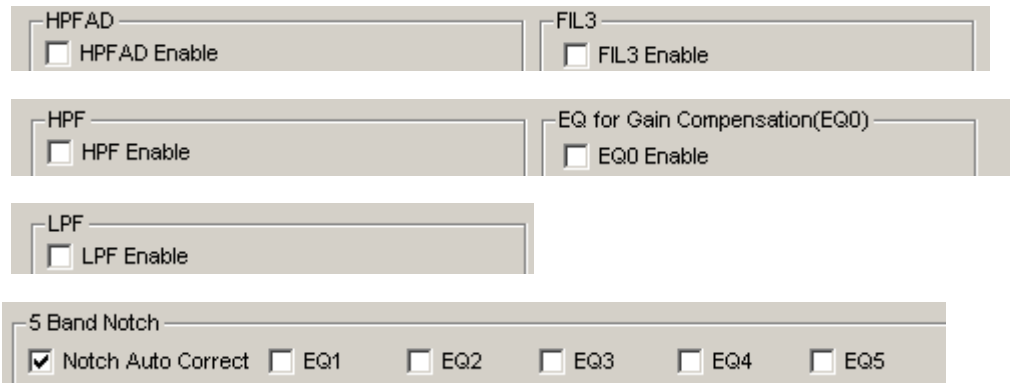


Figure 51.Filter ON/OFF setting button

13-2. [Register Setting]: Register Setting for Filter Dialog Box

A register set value is displayed when push a [Register Setting] button. When a value out of a setting range is set, error message is displayed, and a calculation of register setting is not carried out.

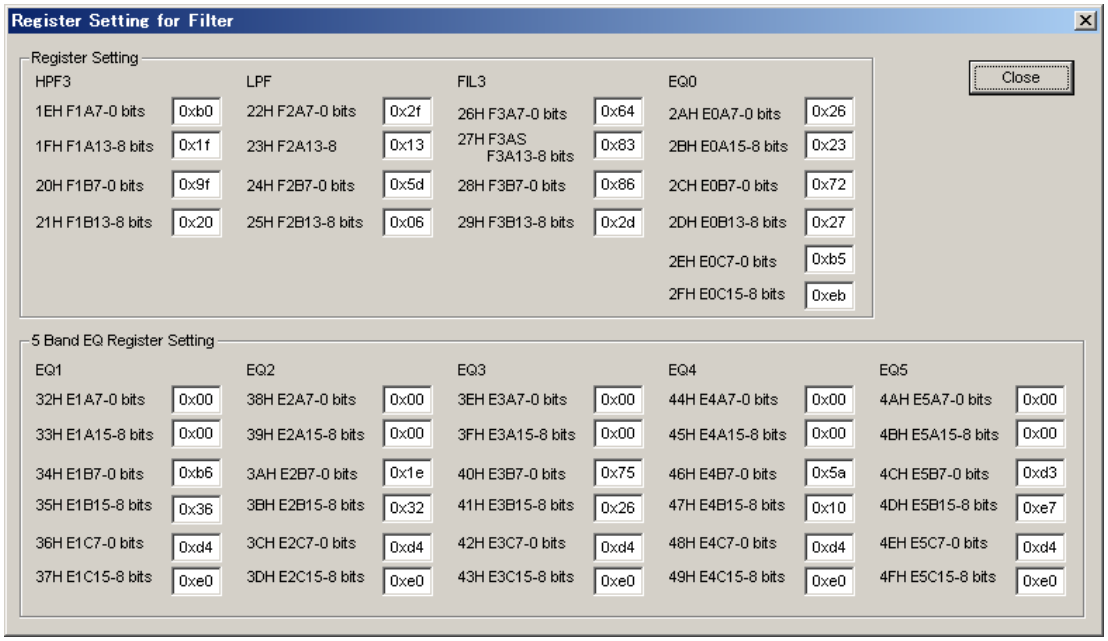


Figure 52.A register setting calculation result

Followings are the cases when a register set value is updated.
(1) When [Register Setting] button was pushed.
(2) When [Frequency Response] button was pushed.
(3) When [UpDate] button was pushed on a frequency characteristic indication window.
(4) When set ON/OFF of a check button “Notch Filter Auto Correction”

13-3. [F Response]: Filter Plot Dialog Box

A frequency characteristic is displayed when push a [F Response] button. Then, a register set point is also updated.
Change Frequency Range, and indication of a frequency characteristic is updated when push a [UpDate] button.

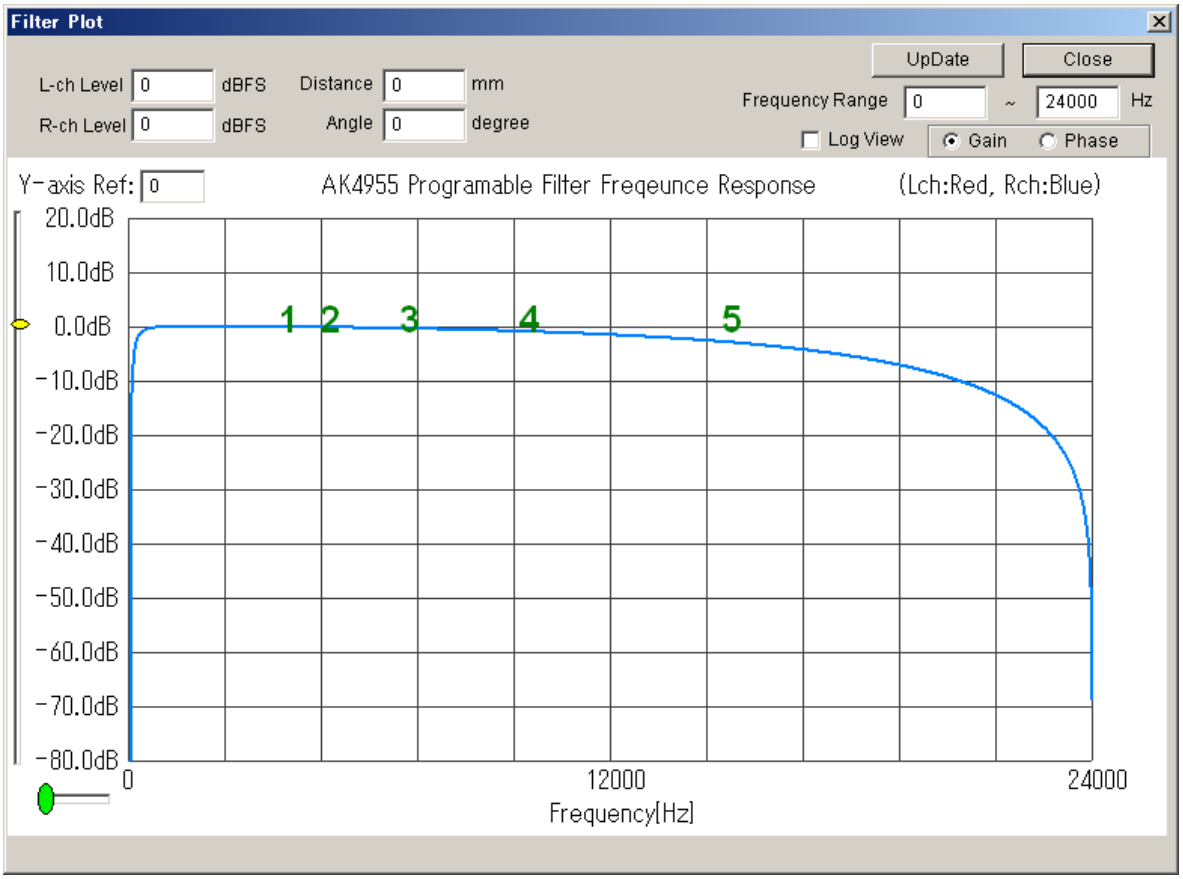


Figure 53.Window of [F Response]

[Frequency Range] : The width of the frequency display is specified.
[Update] : It draws in the graph again.
[Gain/Phase] : Switch of "Gain/Phase" display.
[Log View] : Switch of "Linear/Log" display.
[Close] : Closing the dialog box and finish the process.

~ Adjustment of vertical range ~

[Y-axis Ref] : Display setting of center value.
[Vertical slider] : Movement of vertical display.
[Horizontal slider] : Adjustment of the horizontal display.
(The left side reduces, and the right side expands.)

13-4. 5-BandEQ operation on Filter Plot screen

When EQ (1~5) is turning on, a green number is displayed on the Filter Plot dialog box.
This number shows the setting of the center frequency and the gain of each EQ.
The number under the display is operated with the mouse, and it is possible to set the filter characteristic on this screen.
The center frequency and the gain setting are changed by moving the mouse while left-clicking.
The setting of the bandwidth is changed by moving the mouse while right-clicking.

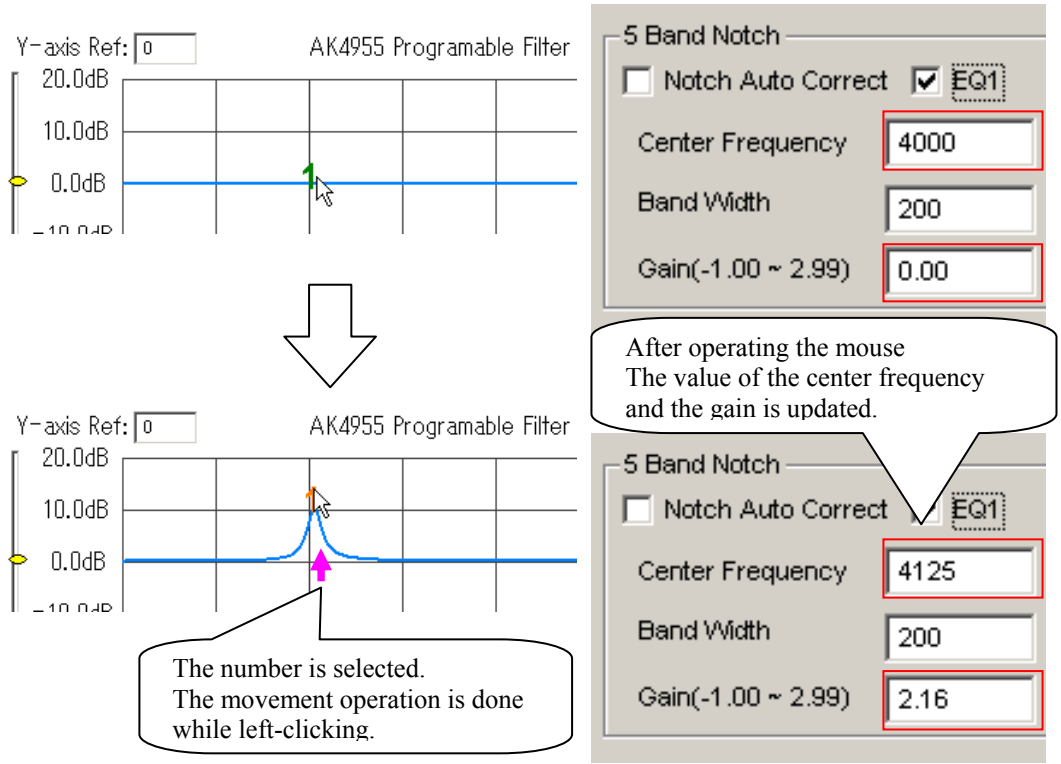


Figure 54.Filter Setting (Left-clicking operation)

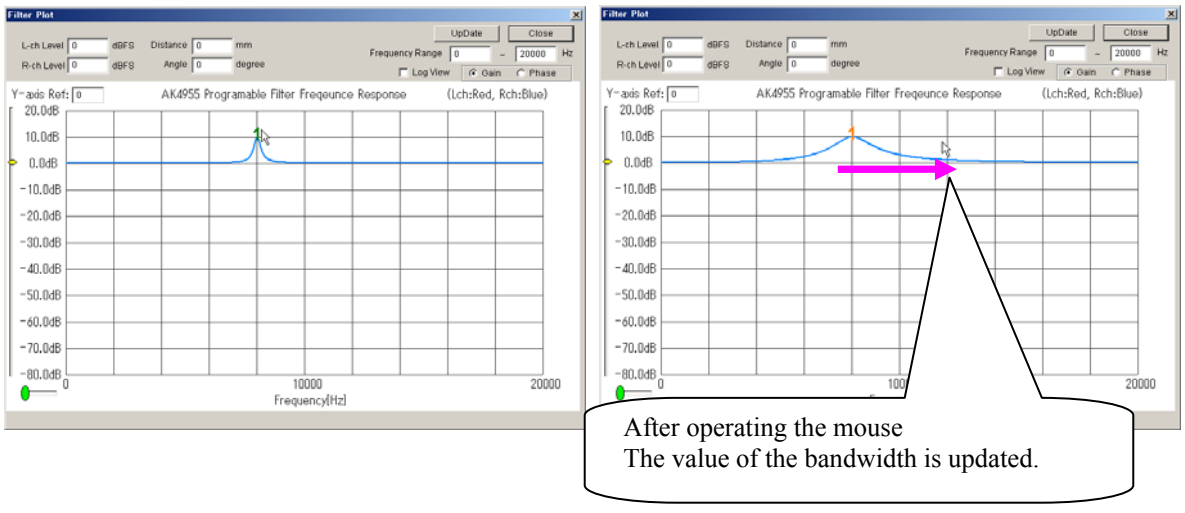


Figure 55.Filter Setting (Right-clicking operation)

13-5. Simulation of Fil3 Filter

Setting of Stereo-MIC
[L-ch Level]/[R-ch Level] : The level of the MIC input is input.
[Distance] : The distance between the sound source and the MIC is set.
[Angle] : The angle between the sound source and the MIC is set.

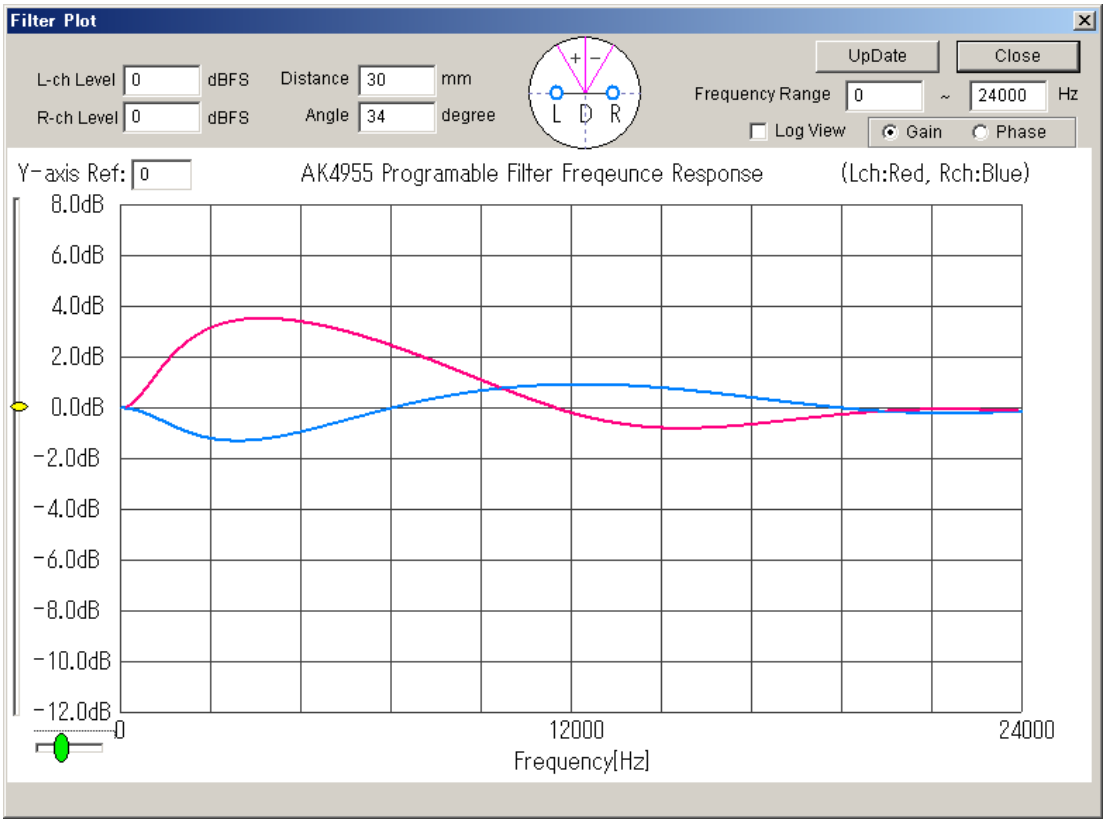
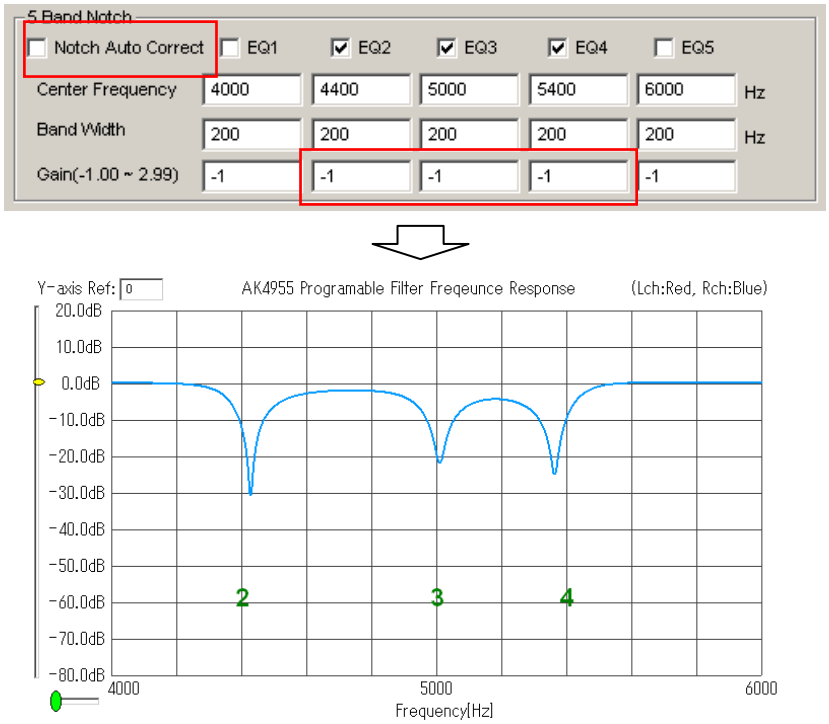


Figure 56.Simulation of Fil3 Filter

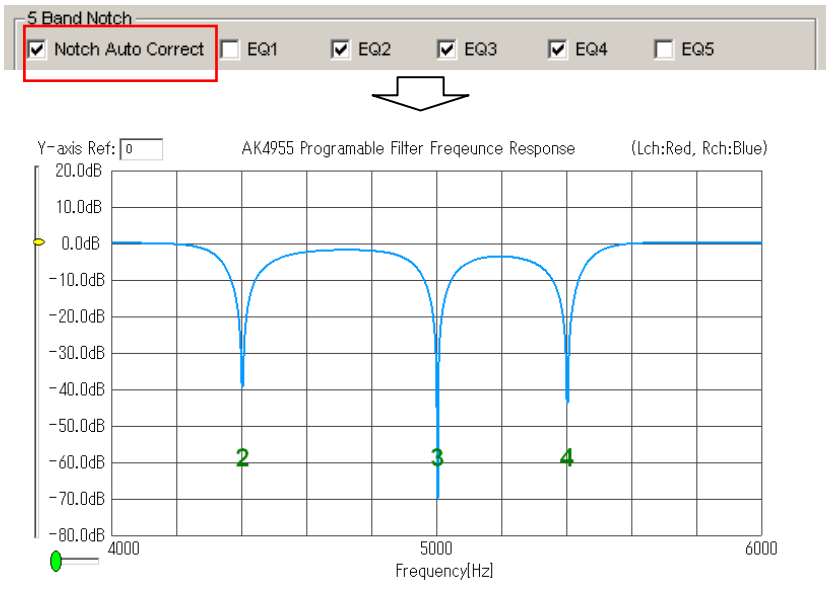
13-6. about “Notch Auto Correct”

If the gain of 5-Band EQ is set to “-1”, Equalizer becomes a notch filter.
When the center frequency of two or more notch filters is adjacent, the gap is generated in the center frequency. When “Notch Auto Correct” button is checked, the center frequency of the notch filter is automatically corrected. The gain setting of the automatic correction function is effective and only EQ of “-1” is effective. (Note 24)

Note 24.There is a possibility that the automatic compensation is not correctly done when the width of the center frequency is smaller than that of the bandwidth setting.



Setting of center frequency: 4400Hz, 5000Hz, 5400Hz / Bandwidth: 200Hz (EQ2~4)
Figure 57. “Notch Auto Correct” function is “OFF”



Setting of center frequency: 4400Hz, 5000Hz, 5400Hz / Bandwidth: 200Hz (EQ2~4)
Figure 58. “Notch Auto Correct” function is “ON”

Measurement Result

[Measurement condition]

- Measurement Unit : Audio Precession System Two Cascade
- MCLK : 12.2880MHz
- BICK : 64fs
- fs : 48 kHz
- Bit : 24bit
- Power Supply : AVDD = LVDD = SVDD = 3.3V, DVDD = TVDD = 1.8V
- Band Width : 20 Hz ~ 20 kHz
- Measurement Mode : External Slave Mode
- Temperature : Room Temperature

[Measurement Result]

1. ADC

a). LIN1/RIN1 pins, MGAIN bits = "+18dB"

Parameter	Result Lch / Rch	Unit
S/(N+D) (-1dBFS Input)	81.0 / 81.5	dB
D-Range (-60dB Input, A-weighted)	88.8 / 88.7	dB
S/N (No Signal, A-weighted)	88.7 / 88.7	dB

b). LIN2/RIN2 pins, MGAIN bits = "0dB"

Parameter	Result Lch / Rch	Unit
S/(N+D) (-1dBFS Input)	81.7 / 82.2	dB
D-Range (-60dB Input, A-weighted)	97.7 / 97.8	dB
S/N (No Signal, A-weighted)	98.0 / 97.8	dB

2. DAC

a). LOUT/ROUT pins, LVCM bits = "01", R_L=10kΩ

Parameter	Result Lch / Rch	Unit
S/(N+D) (-3dBFS Input)	87.5 / 87.6	dB
S/N (No Signal, A-weighted)	92.6 / 92.5	dB

b). SPP/SPN pins, SPKG bits = "01", R_L=8Ω

Parameter	Result	Unit
S/(N+D) (-0.5dBFS Input)	80.5	dB
S/N (No Signal, A-weighted)	96.7	dB

PLOT DATA

1-a). ADC [LIN1/RIN1 pins, MGAIN = “+18dB”]

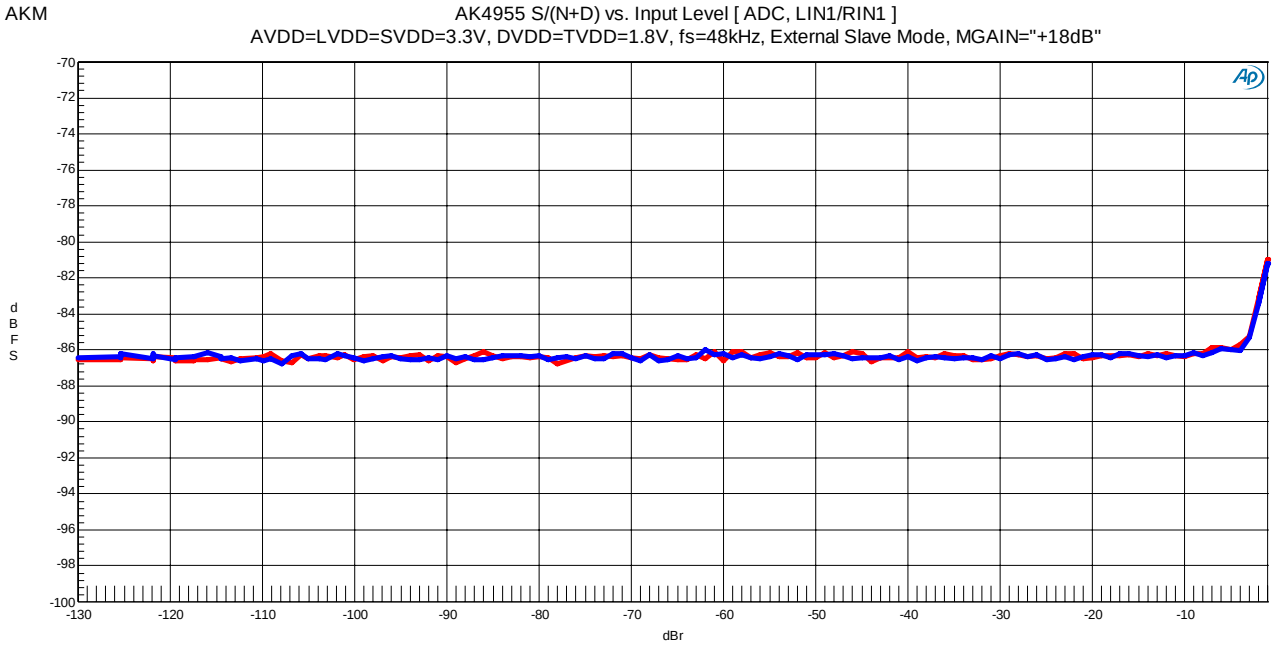


Figure 59.S/(N+D) vs. Input Level

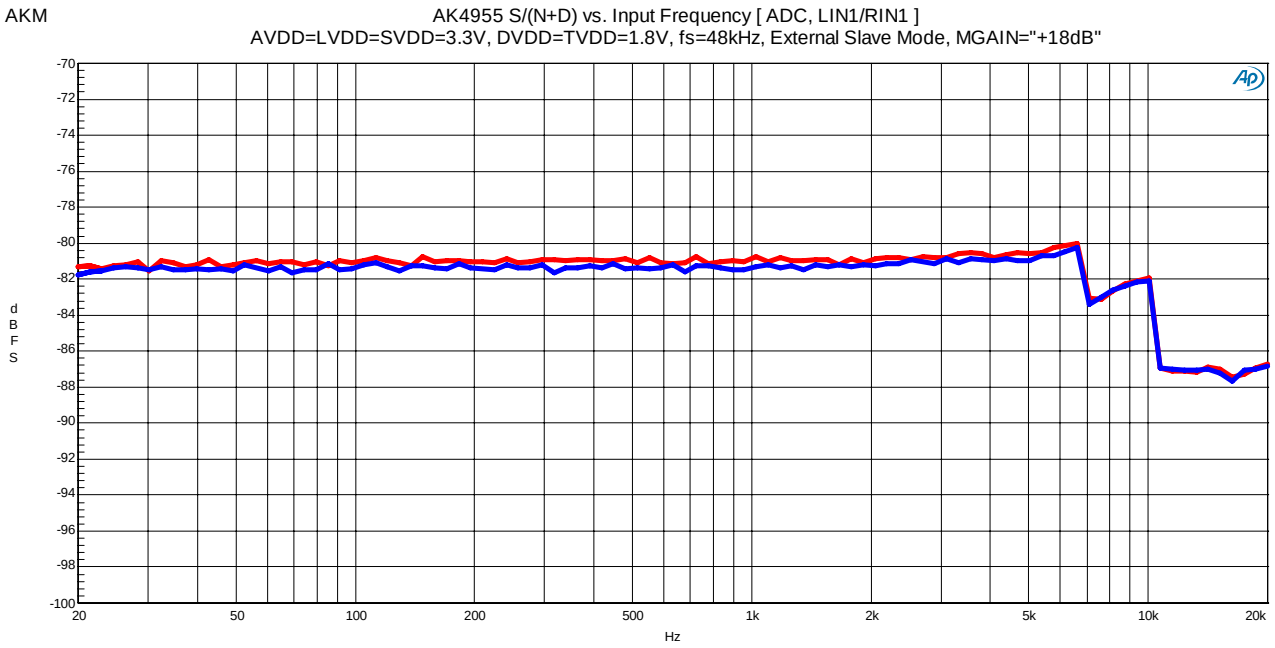


Figure 60.S/(N+D) vs. Input Frequency

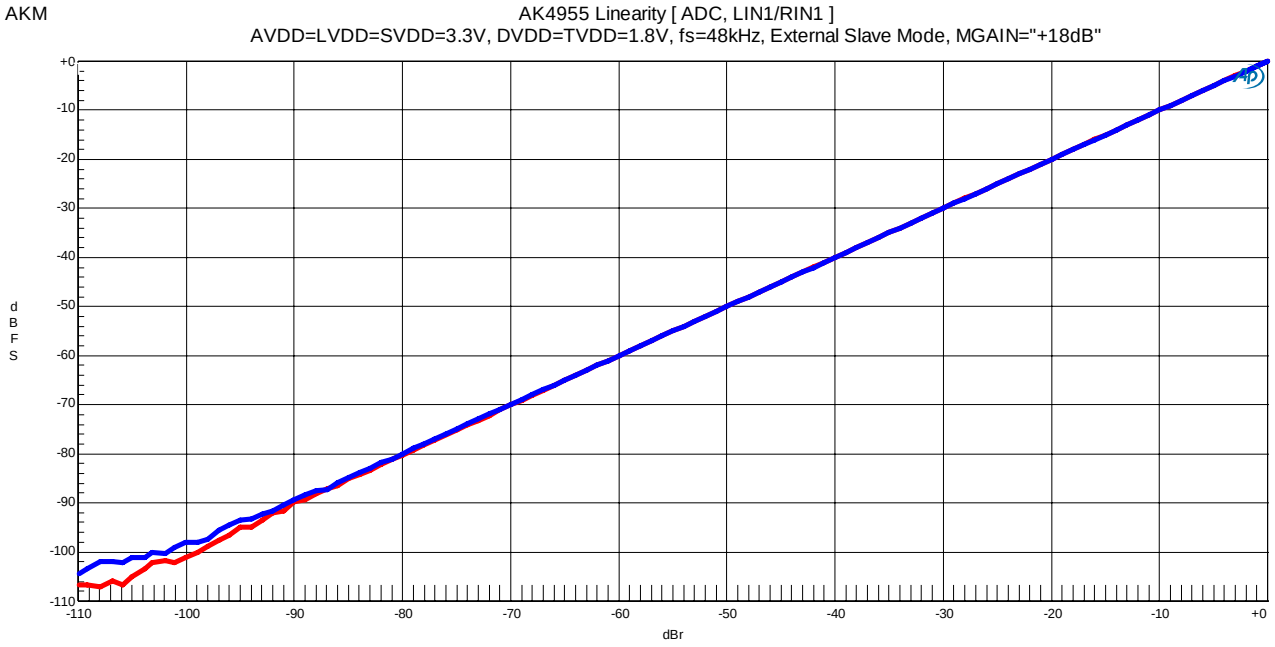


Figure 61.Linearity

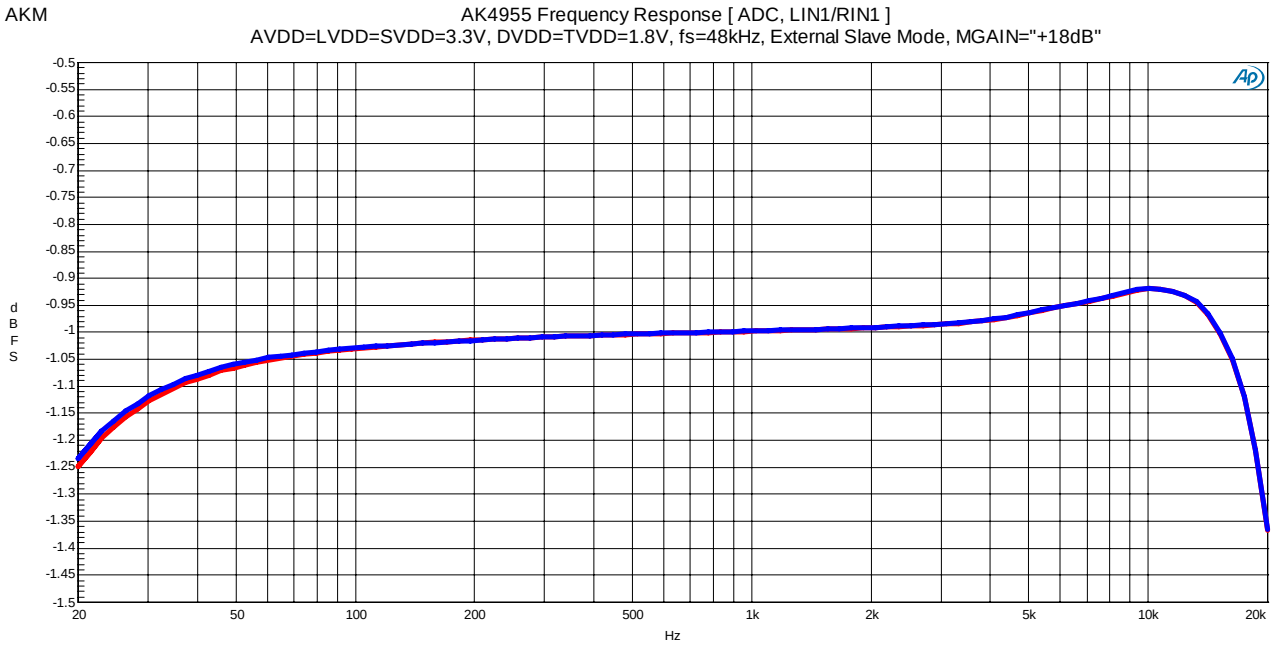


Figure 62.Frequency Response

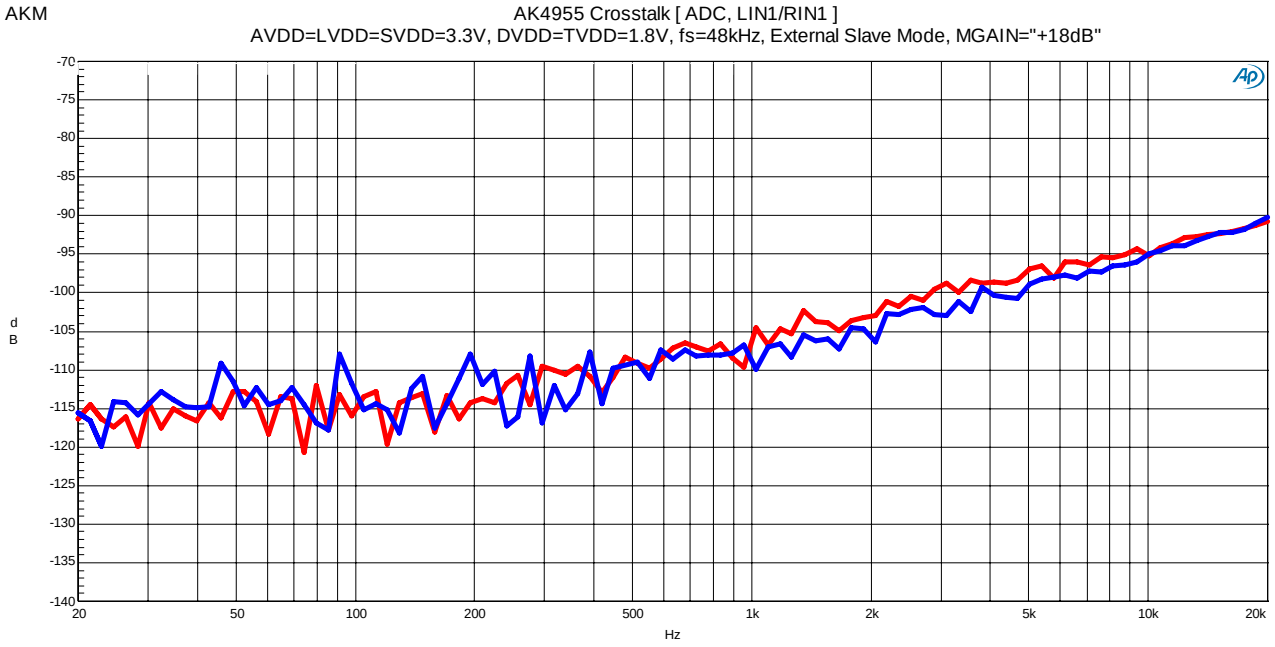


Figure 63.Crosstalk

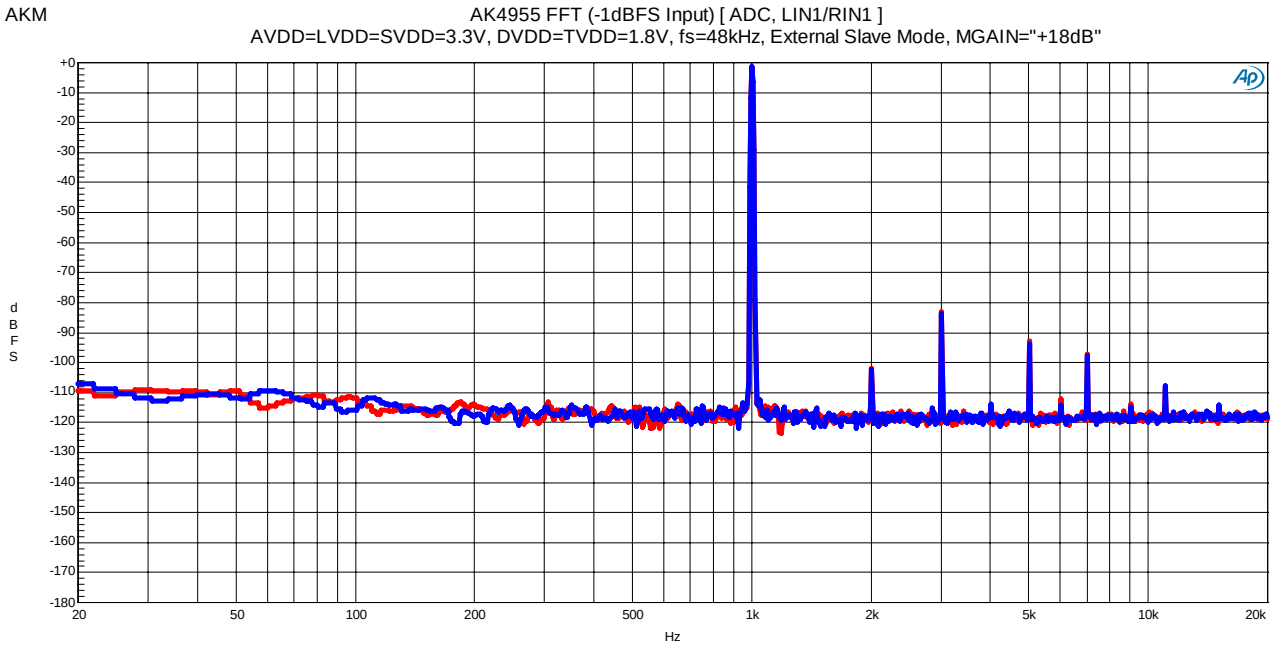


Figure 64.FFT (-1dBFS Input)

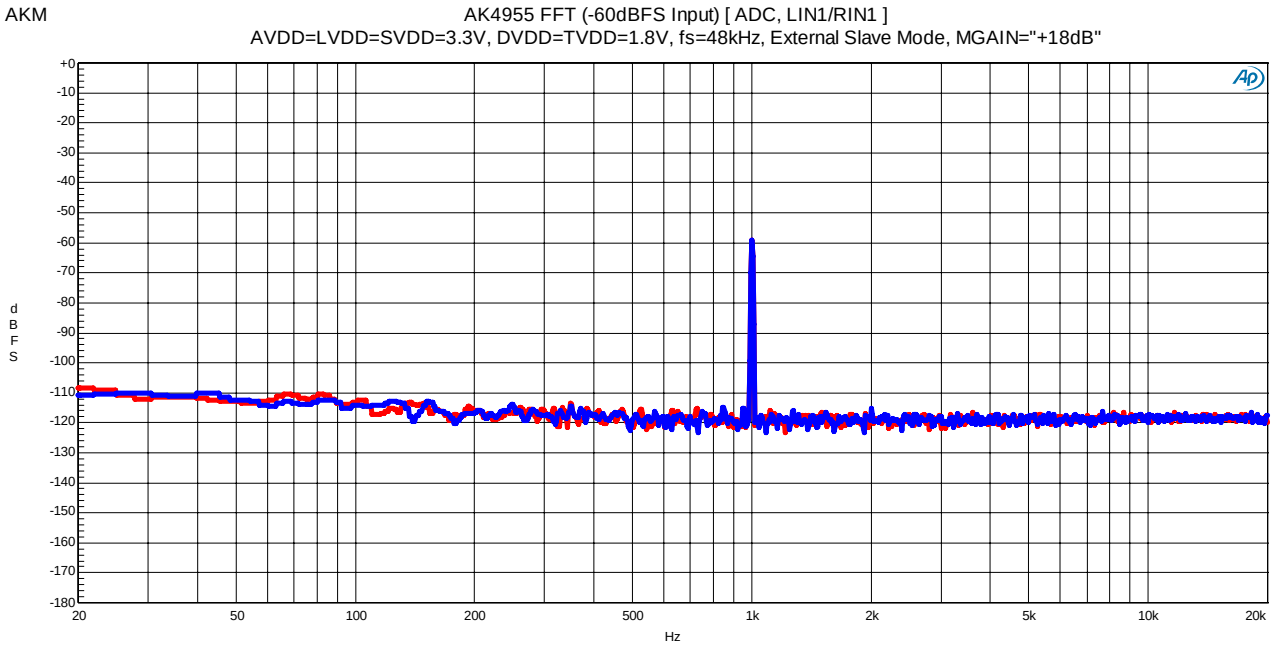


Figure 65.FFT (-60dBFS Input)

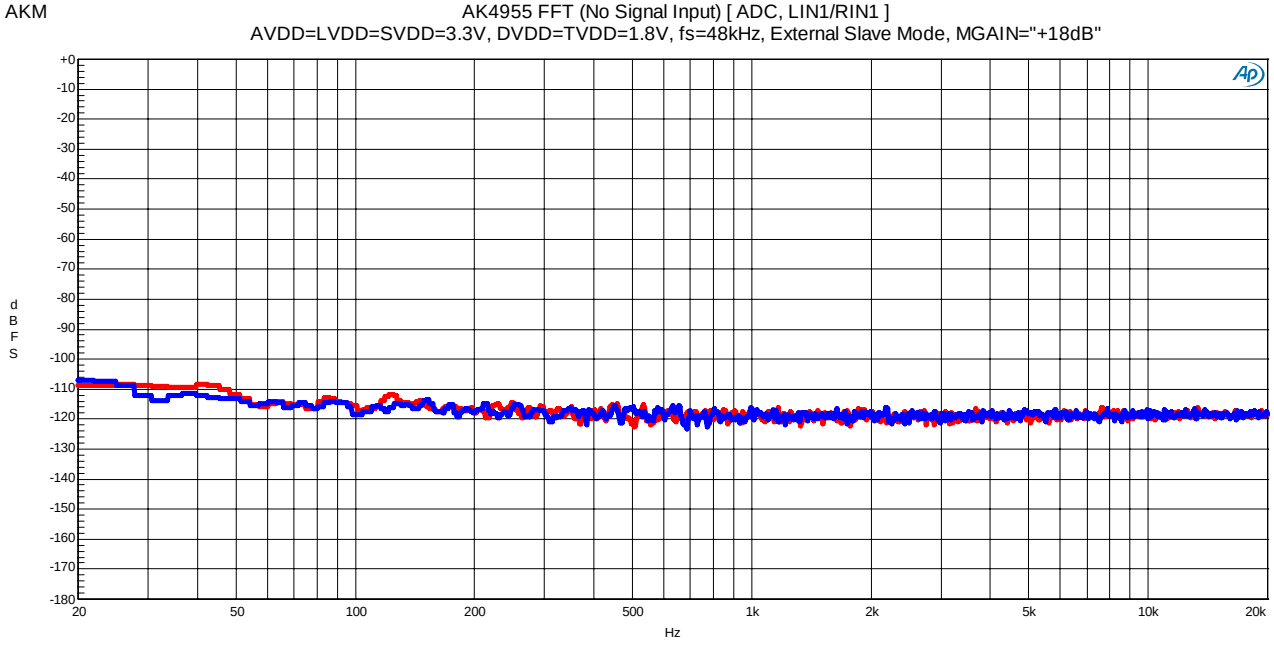


Figure 66.FFT (No Signal Input)

1-b). ADC [LIN2/RIN2 pins, MGAIN = “0dB”]

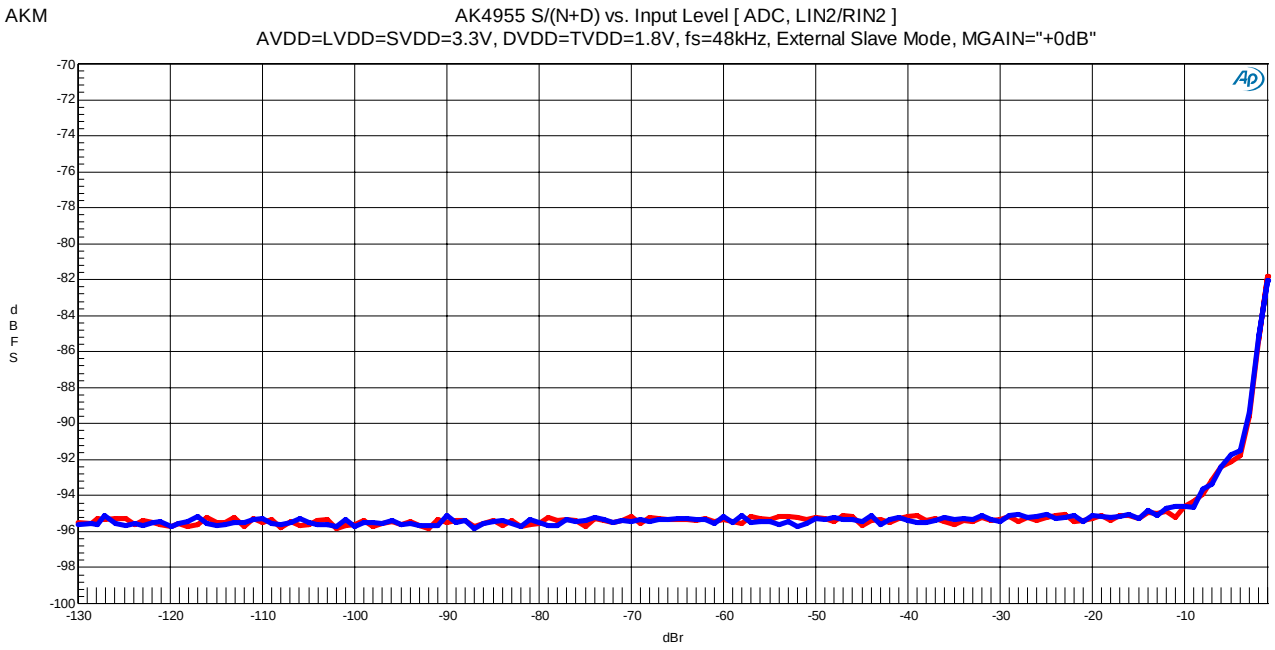


Figure 67.S/(N+D) vs. Input Level

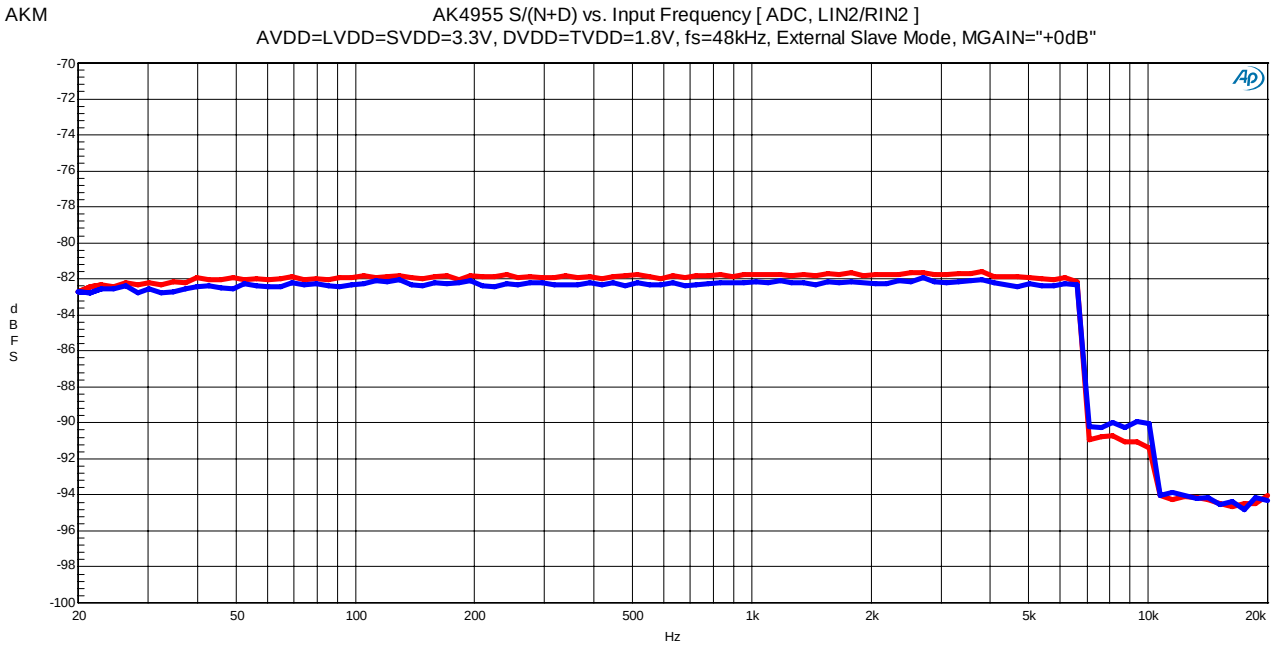


Figure 68.S/(N+D) vs. Input Frequency

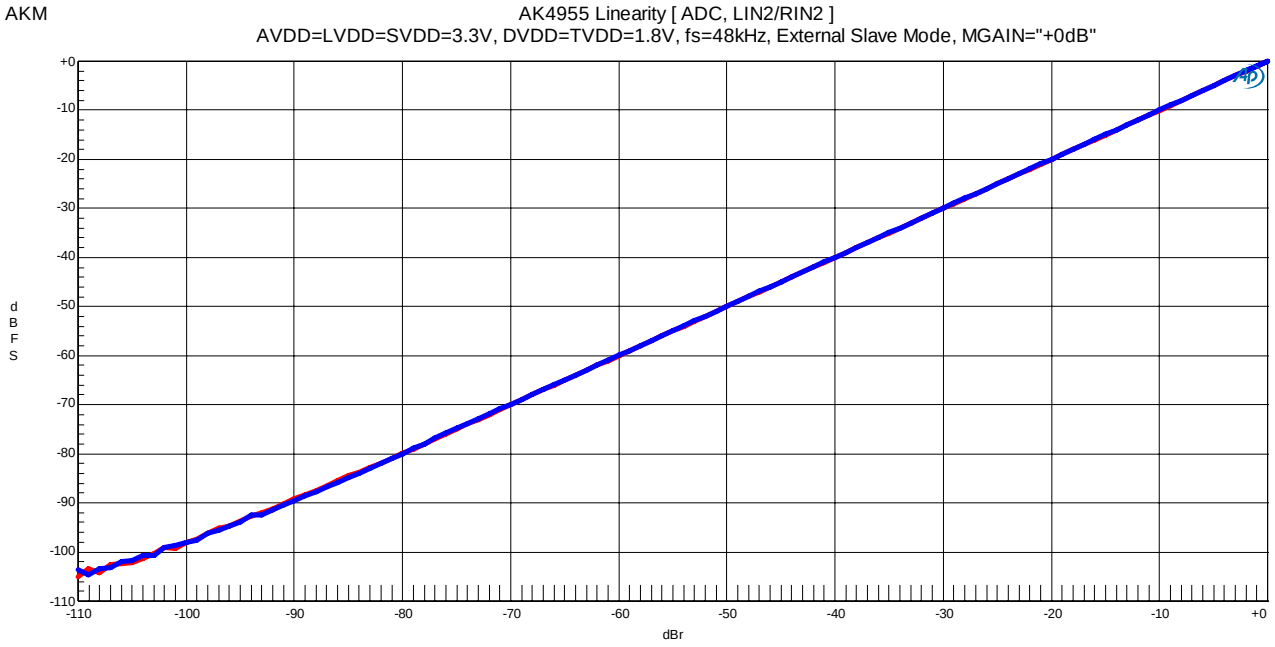


Figure 69.Linearity

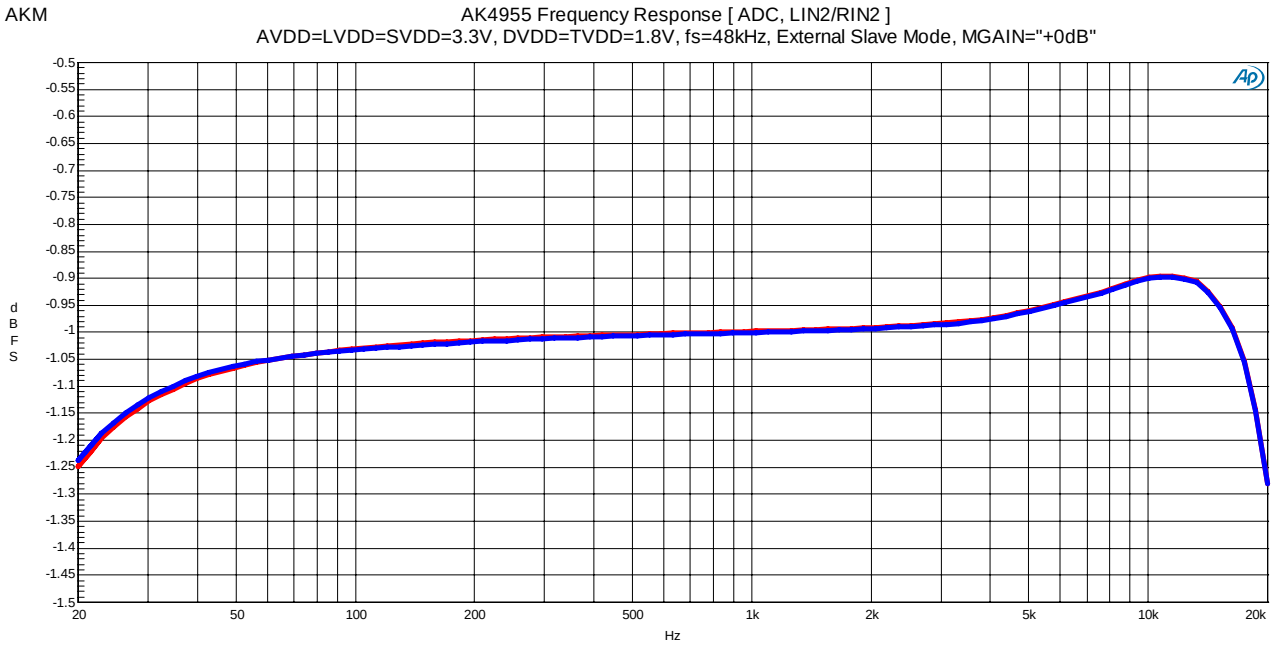


Figure 70.Frequency Response

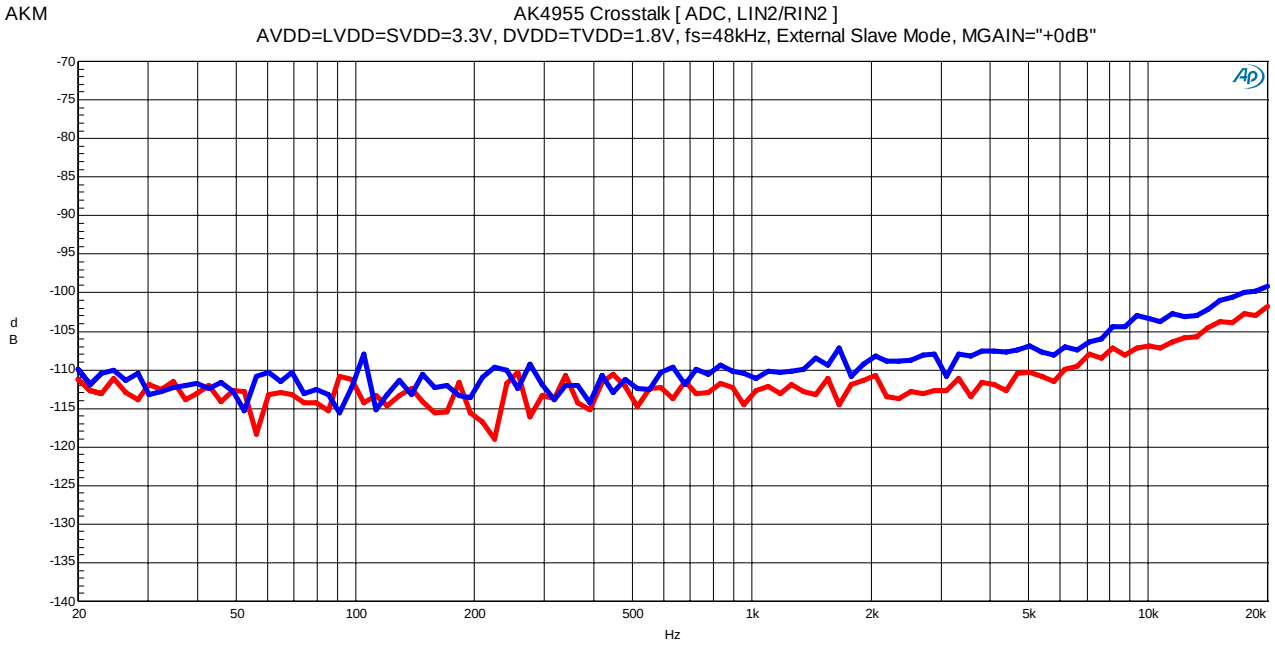


Figure 71.Crosstalk

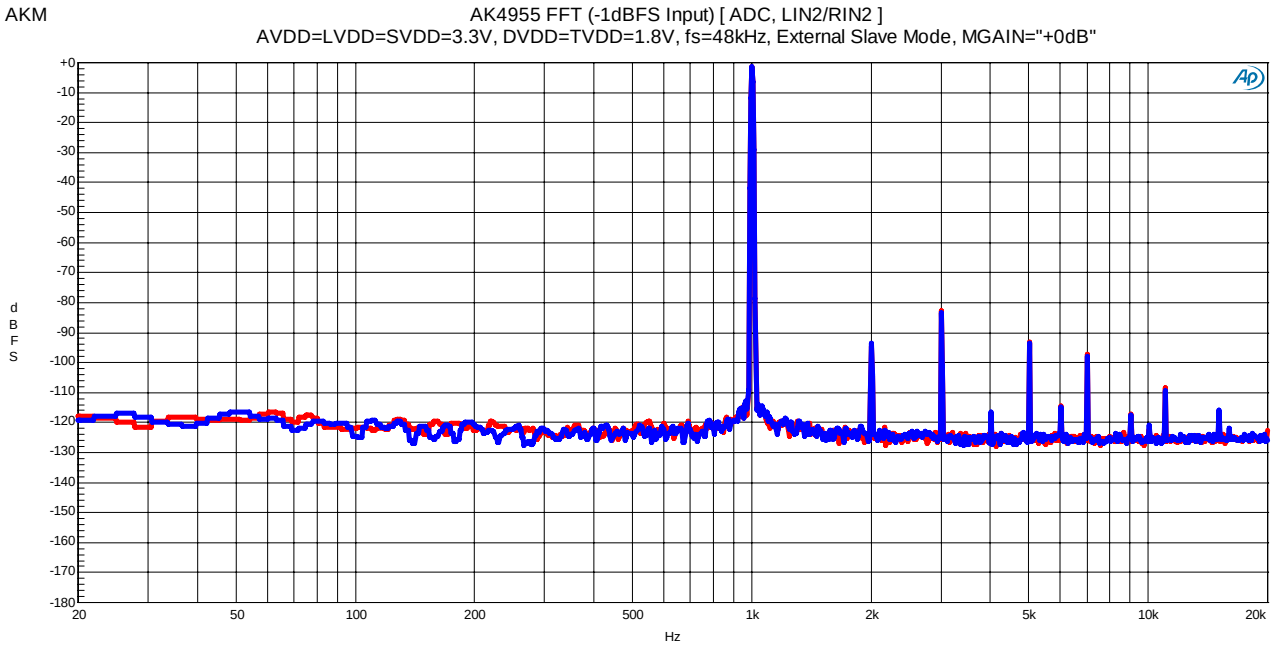


Figure 72.FFT (-1dBFS Input)

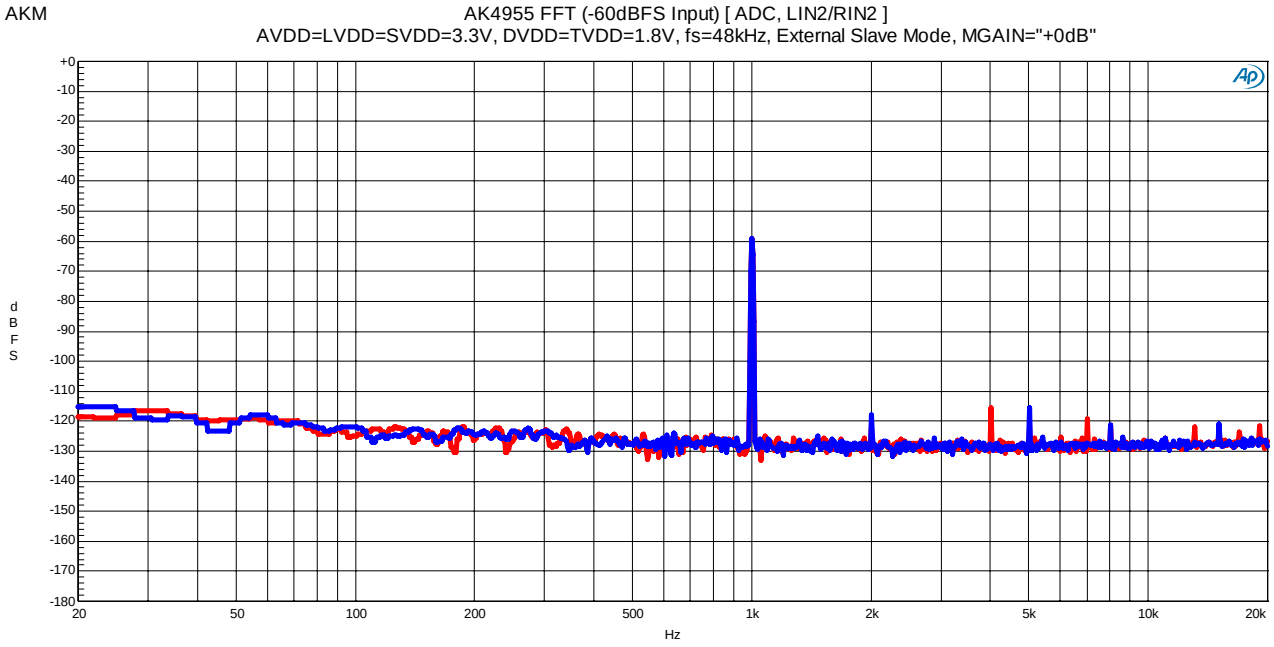


Figure 73.FFT (-60dBFS Input)

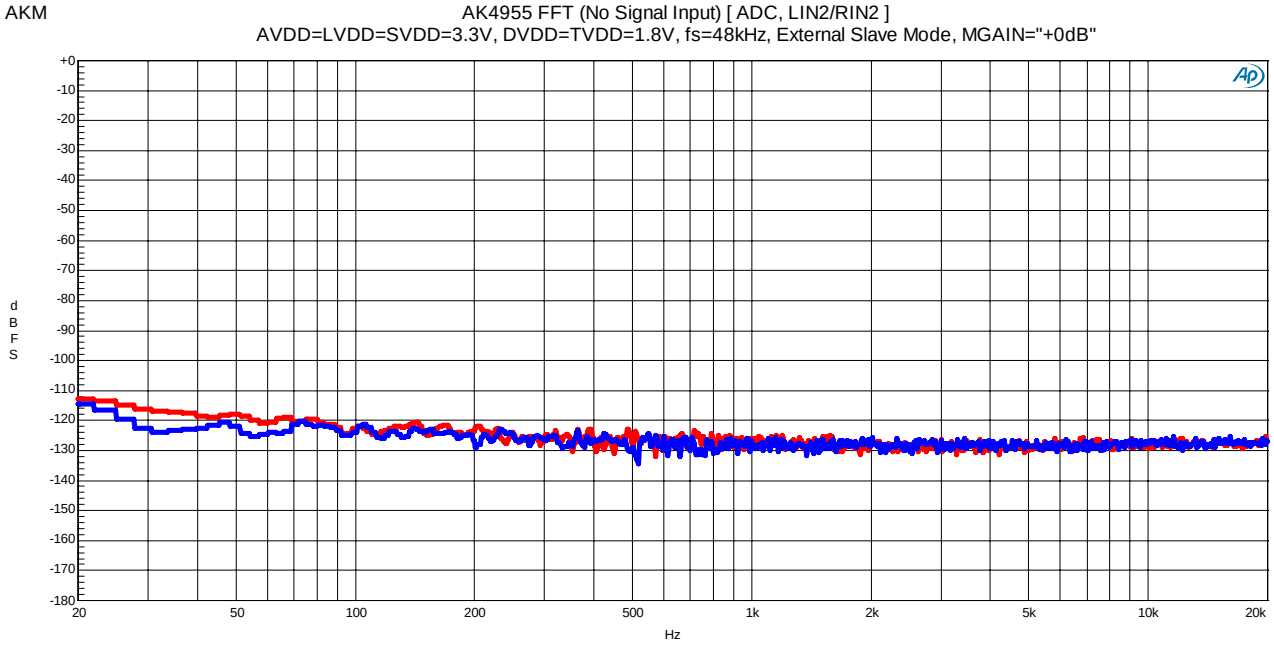


Figure 74.FFT (No Signal Input)

2-a). DAC [LOUT/ROUT pins, LVCM(1-0) bits = “01”]

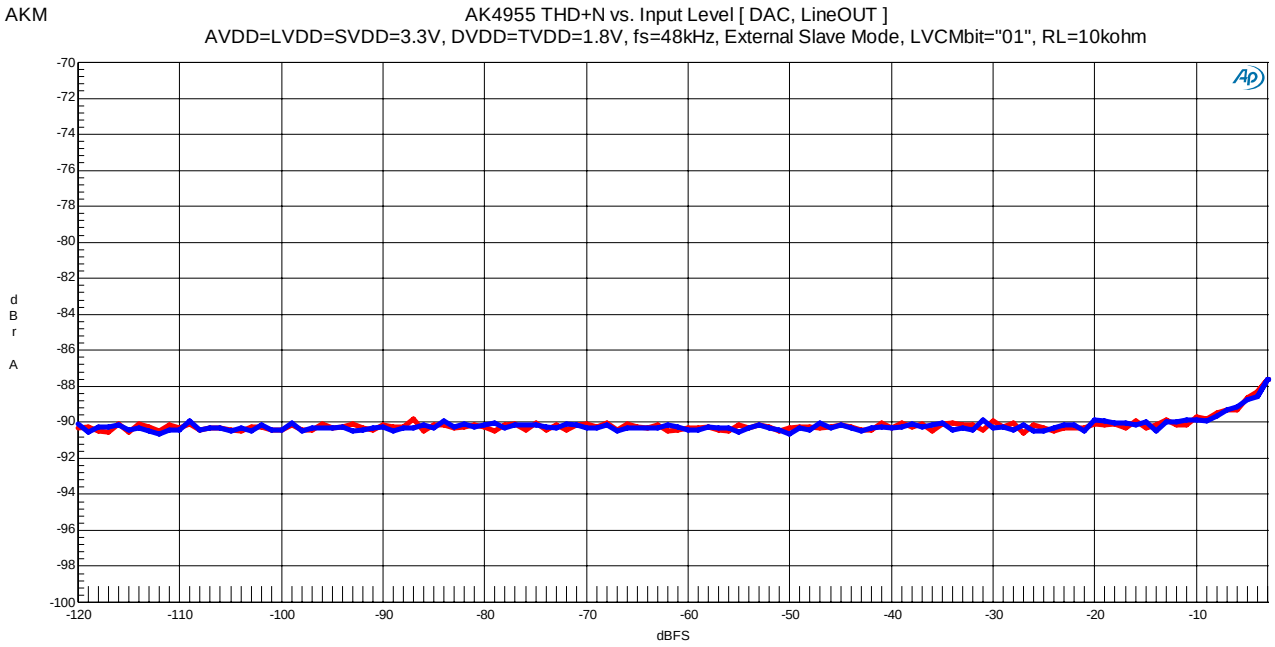


Figure 75.S/(N+D) vs. Input Level

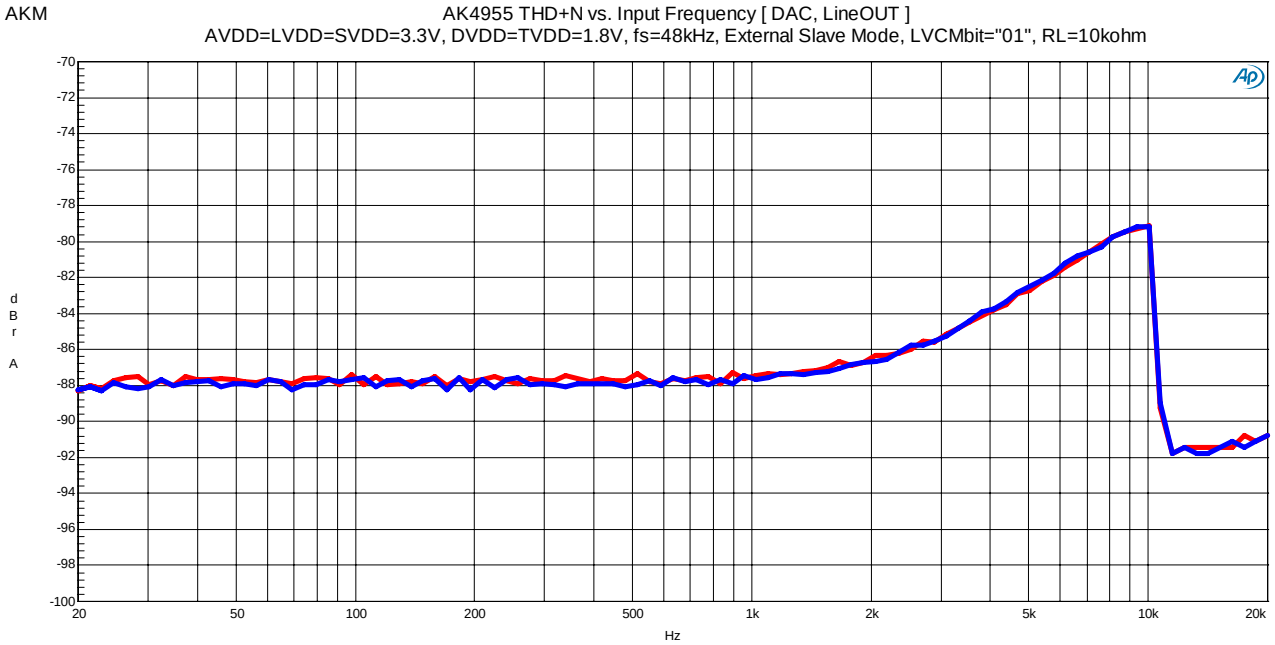


Figure 76.S/(N+D) vs. Input Frequency

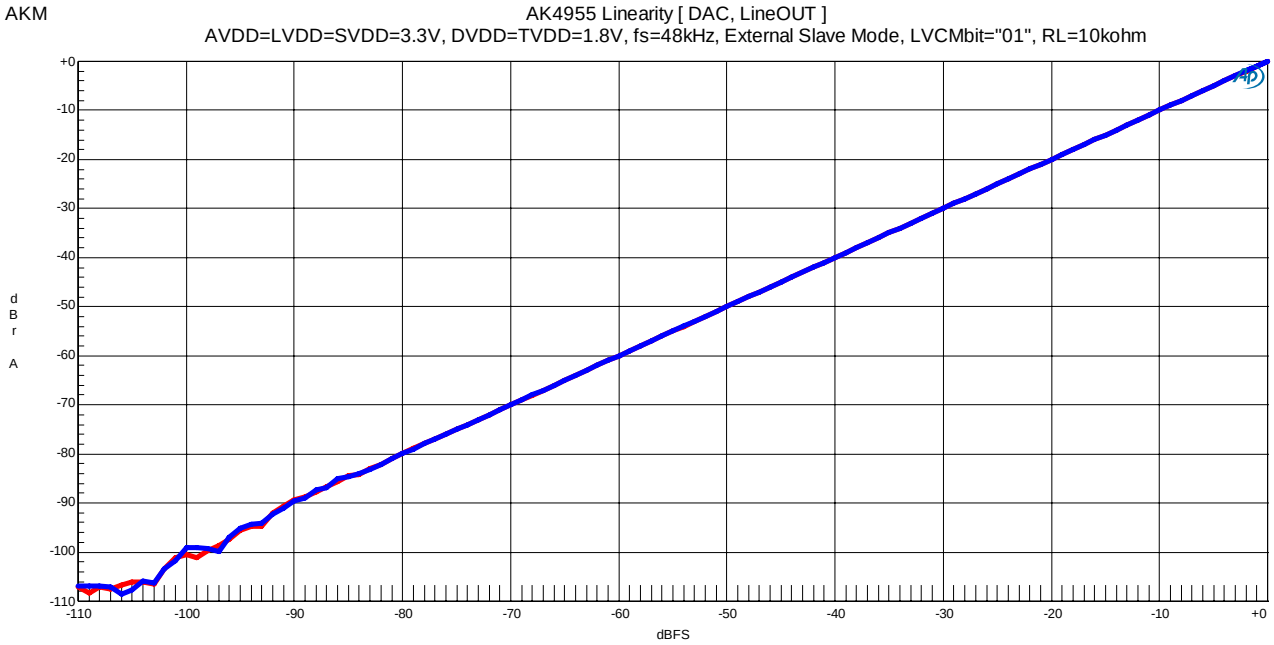


Figure 77.Linearity

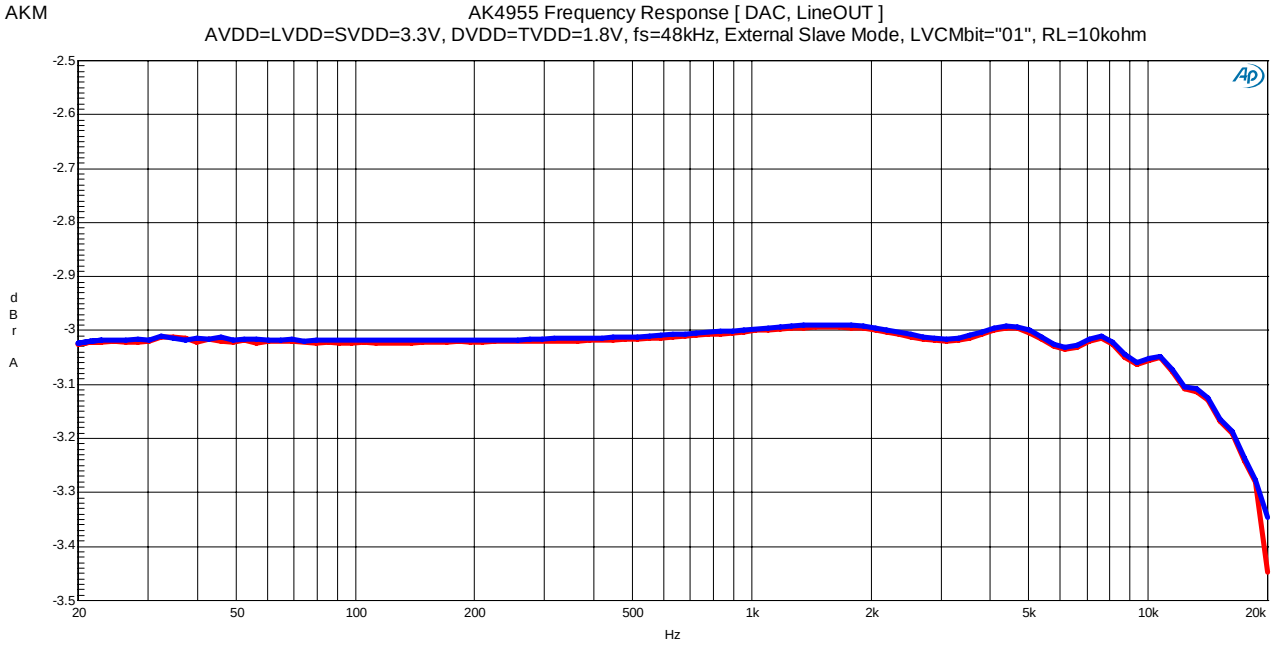


Figure 78.Frequency Response (Pin Direct)

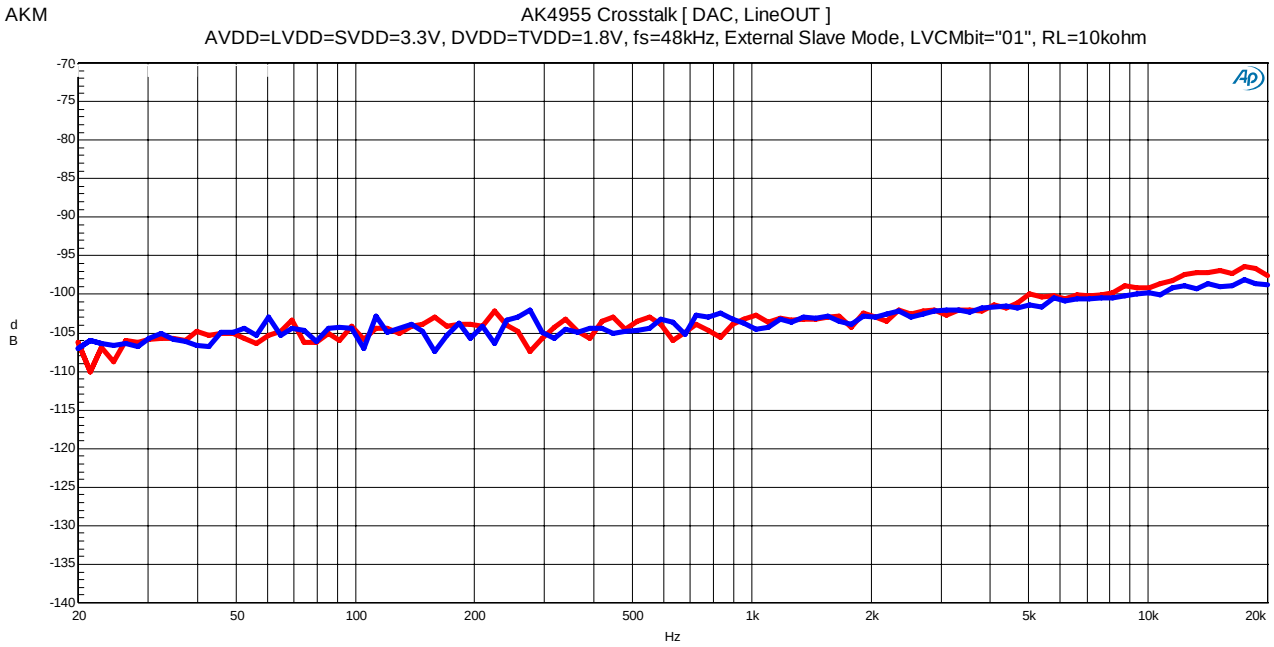


Figure 79.Crosstalk

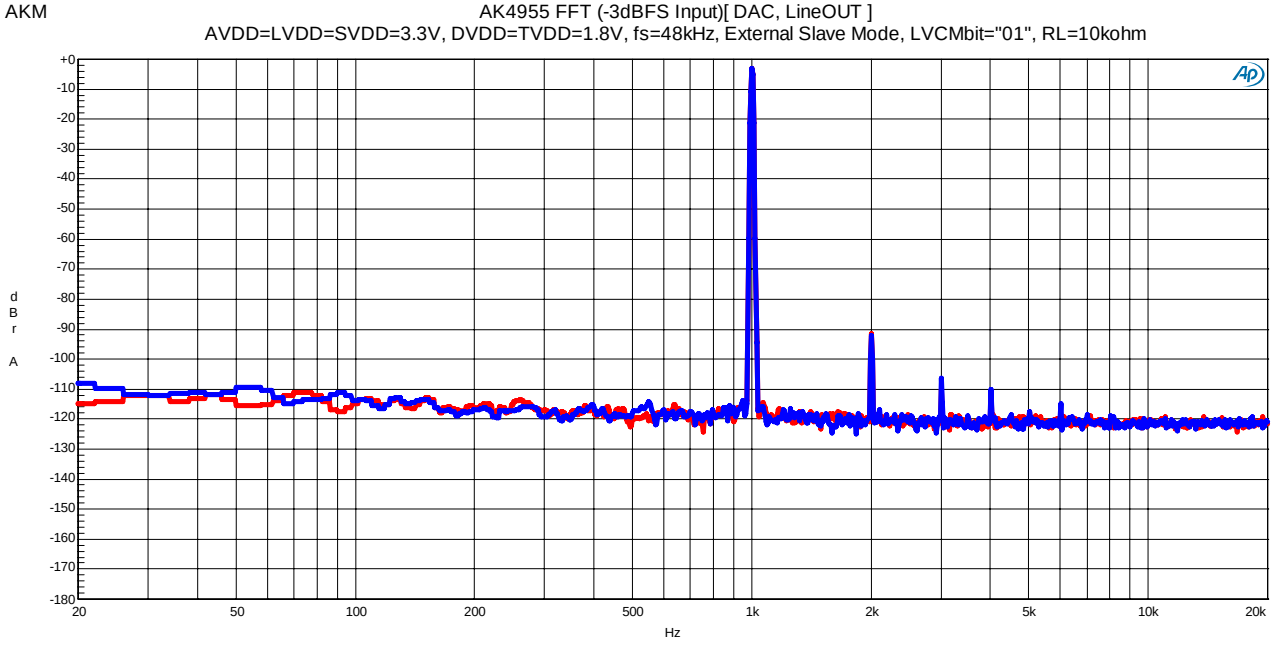


Figure 80.FFT (-3dBFS Input)

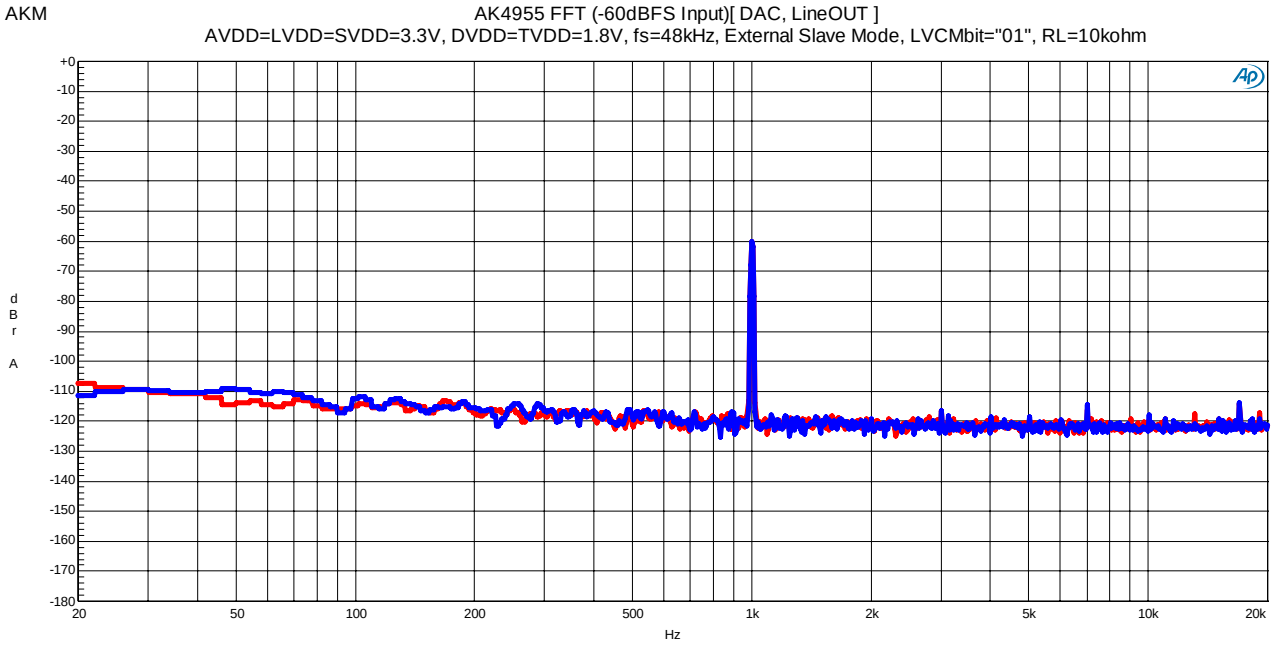


Figure 81.FFT (-60dBFS Input)

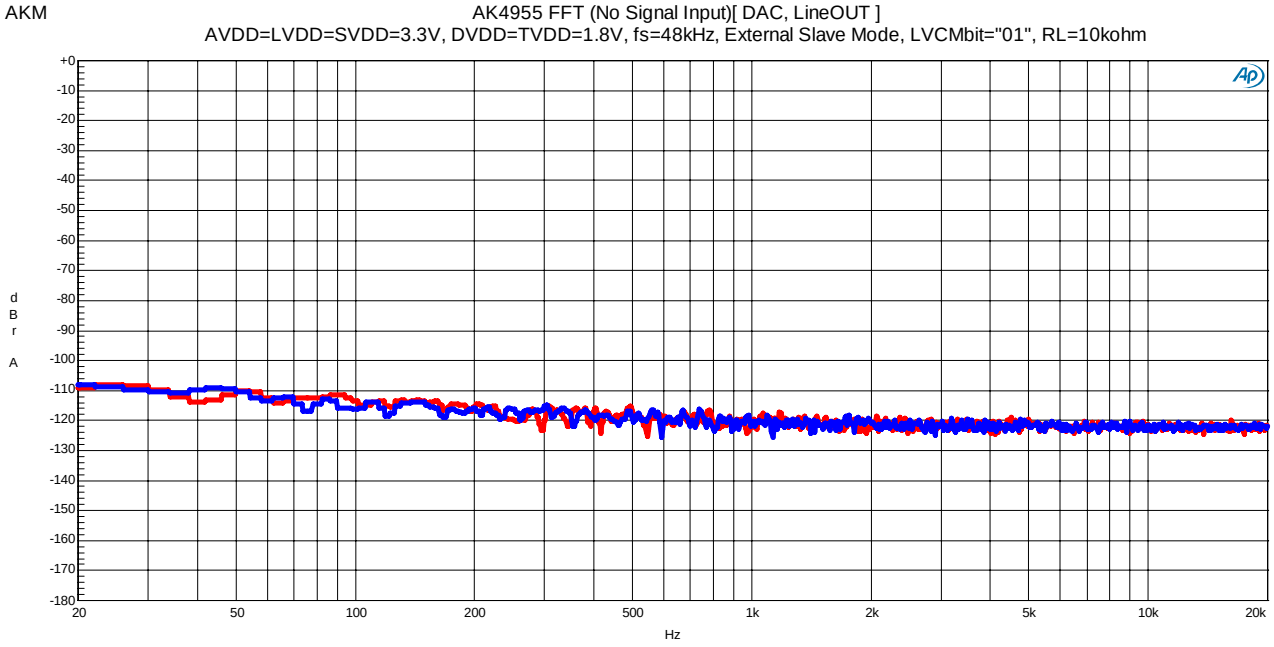


Figure 82.FFT (No Signal Input)

2-b). DAC [SPP/SPN pins, SPKG(1-0) bits = “01”]

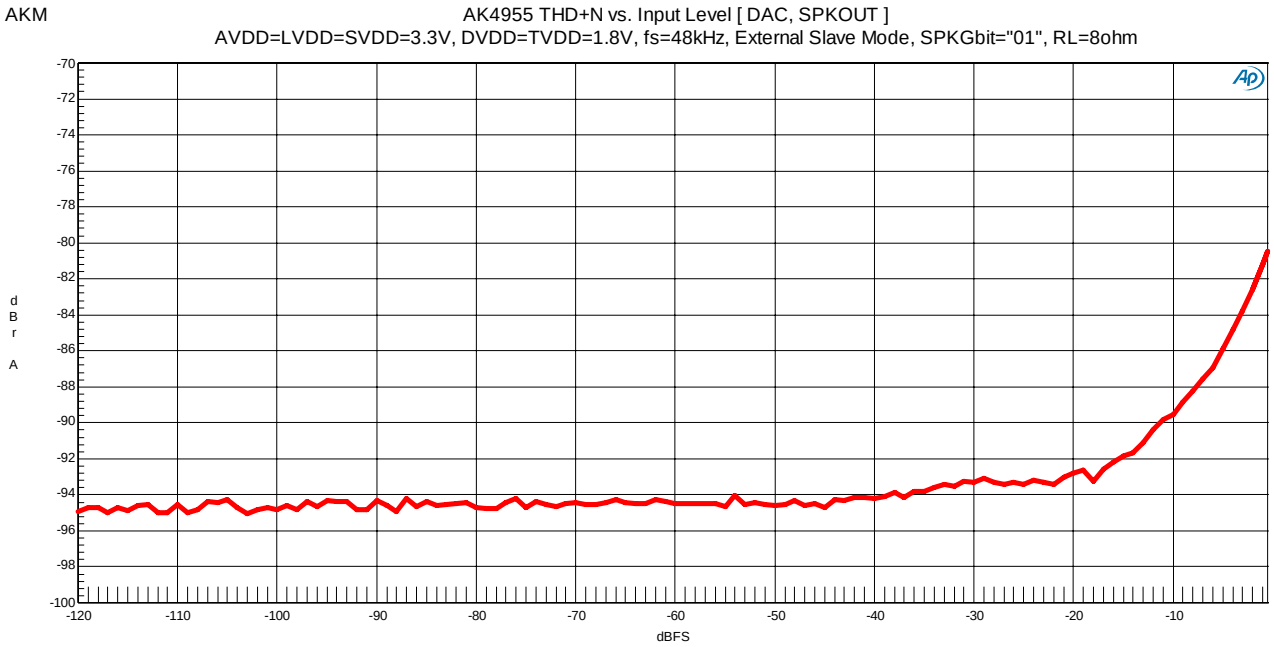


Figure 83.S/(N+D) vs. Input Level

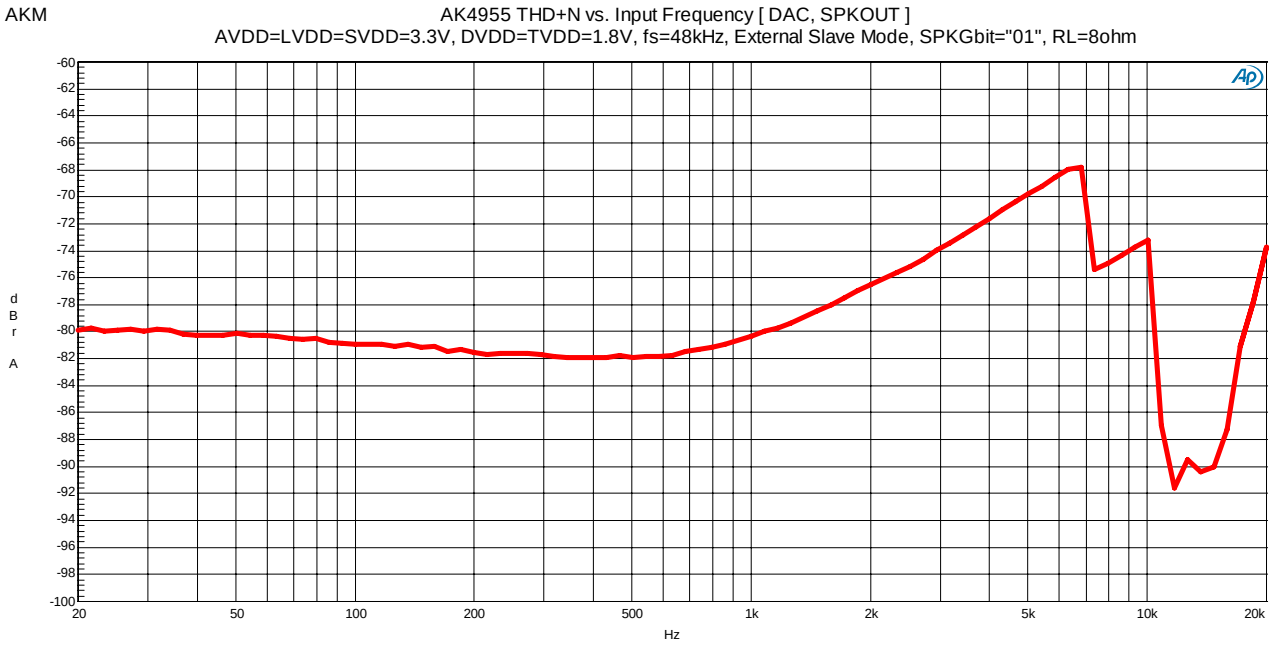


Figure 84.S/(N+D) vs. Input Frequency

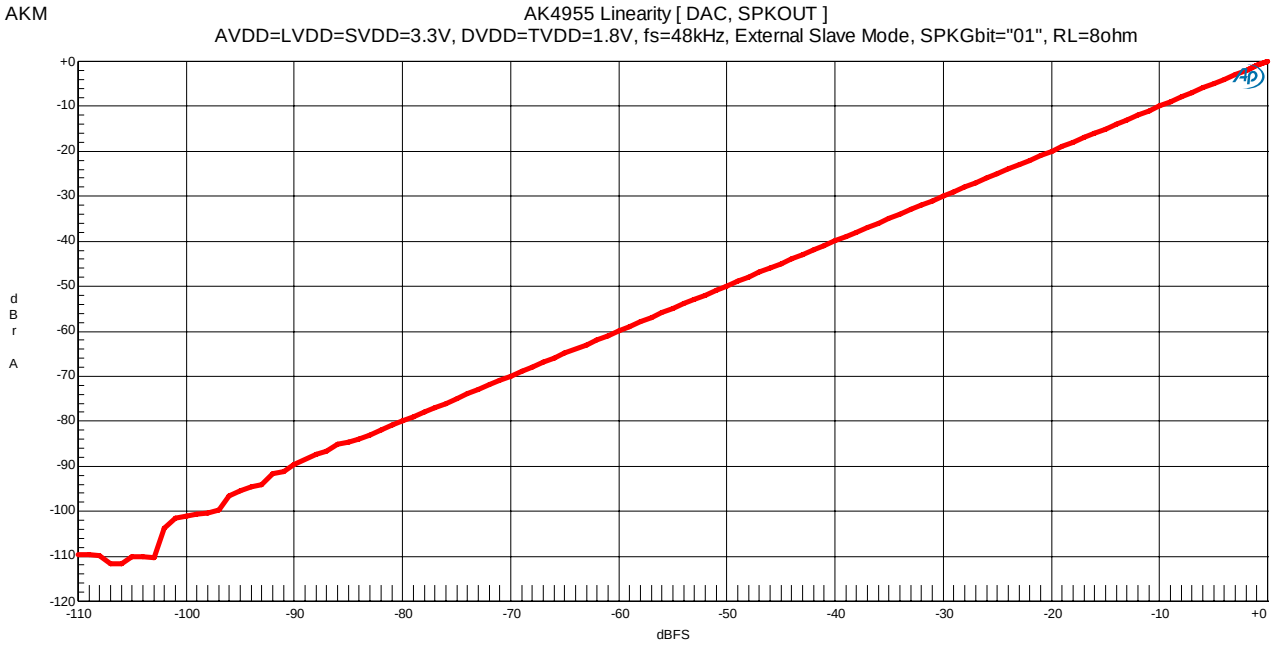


Figure 85.Linearity

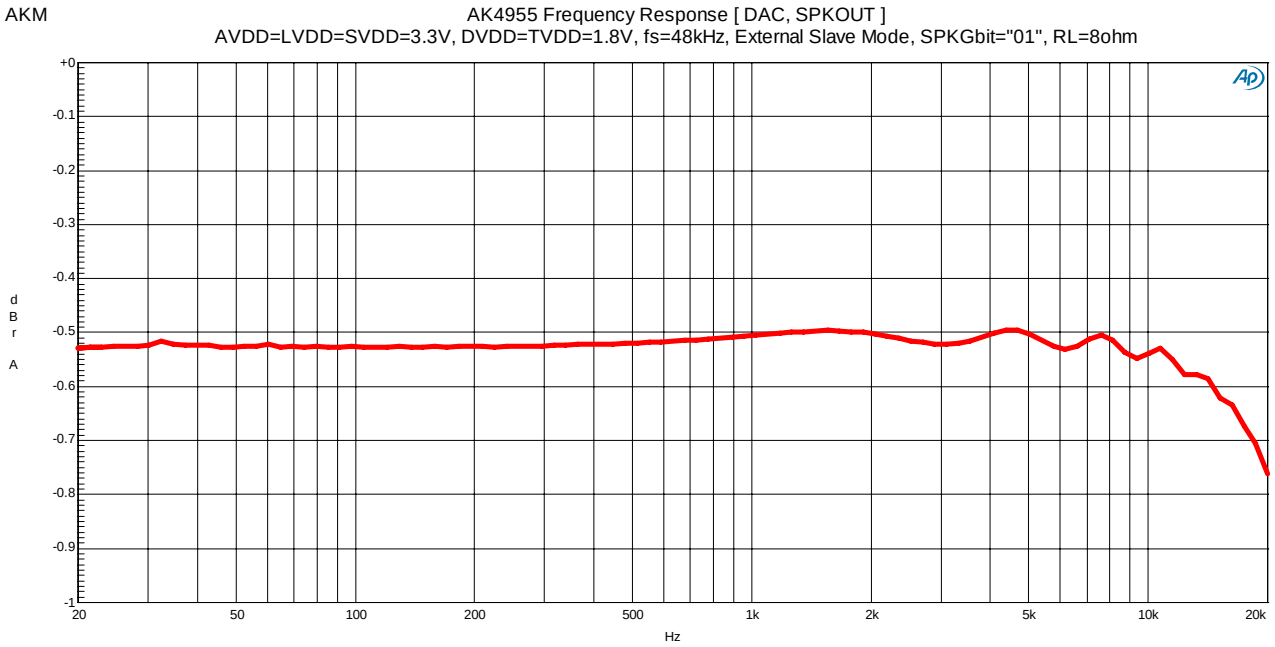


Figure 86.Frequency Response

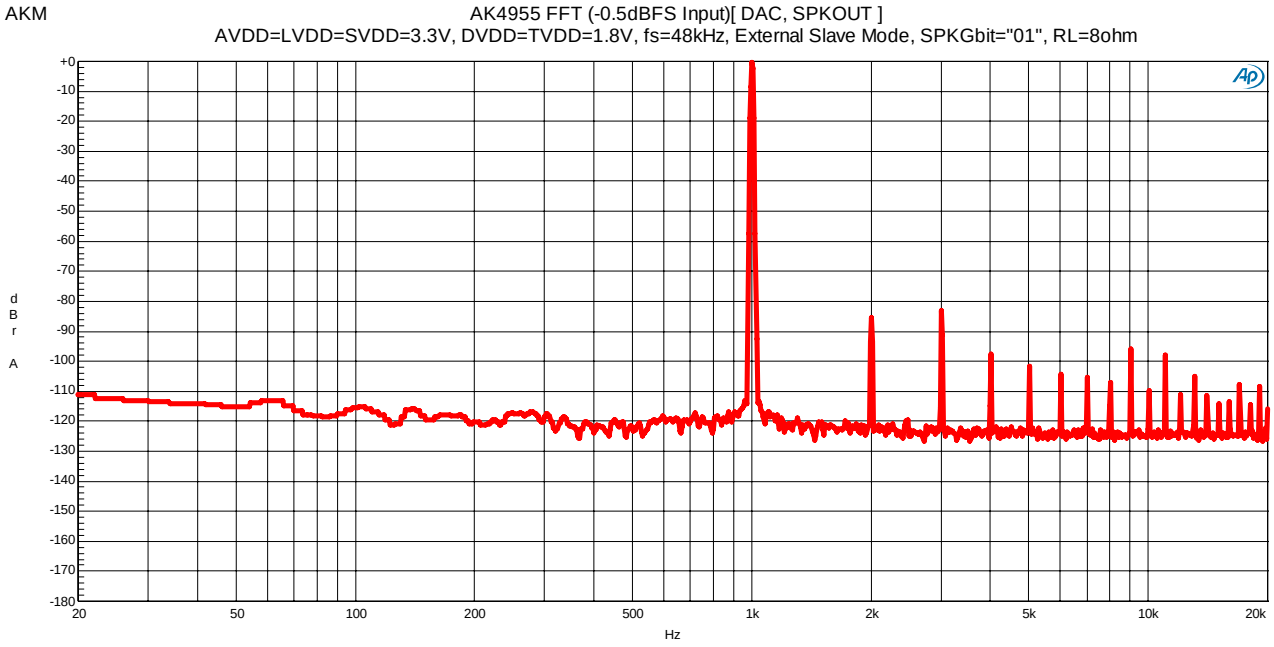


Figure 87.FFT (-0.5dBFS Input)

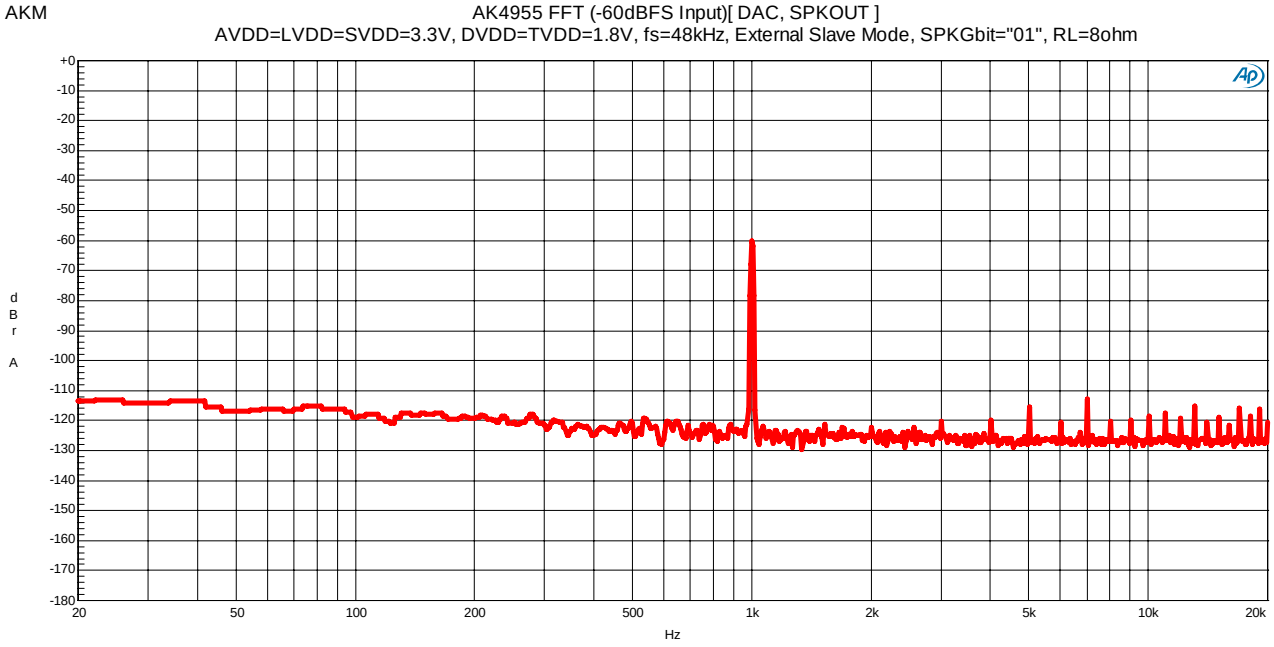


Figure 88.FFT (-60dBFS Input)

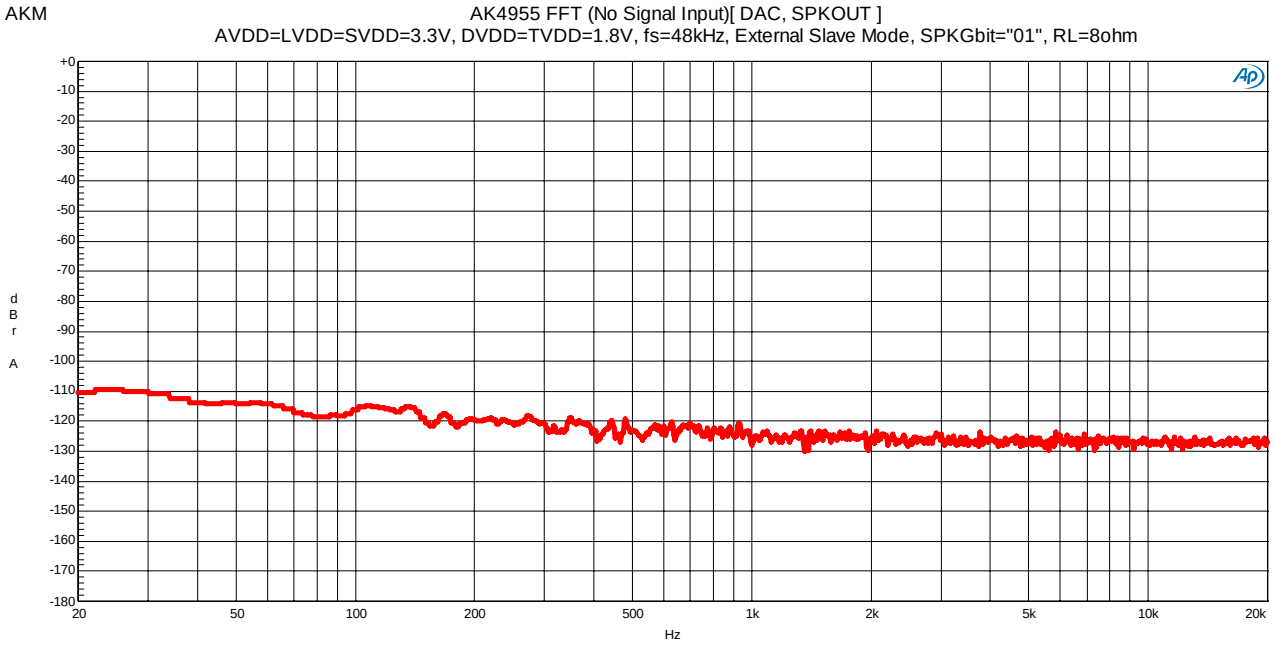


Figure 89.FFT (No Signal Input)

3. VIDEO PLOT DATA

[Measurement condition]

- Measurement unit : Tektronix VM700T Video Measurement set
- Power Supply : AVDD = LVDD = SVDD = 3.3V, DVDD = TVDD = 1.8V
- Temperature : Room Temperature
- Input Level : 1.0Vpp Input
- VG bits : "00" (+6dB)

・S/N

- Input signal : 0% Flat Field
- Measurement Frequency : 100kH ~ 6MHz

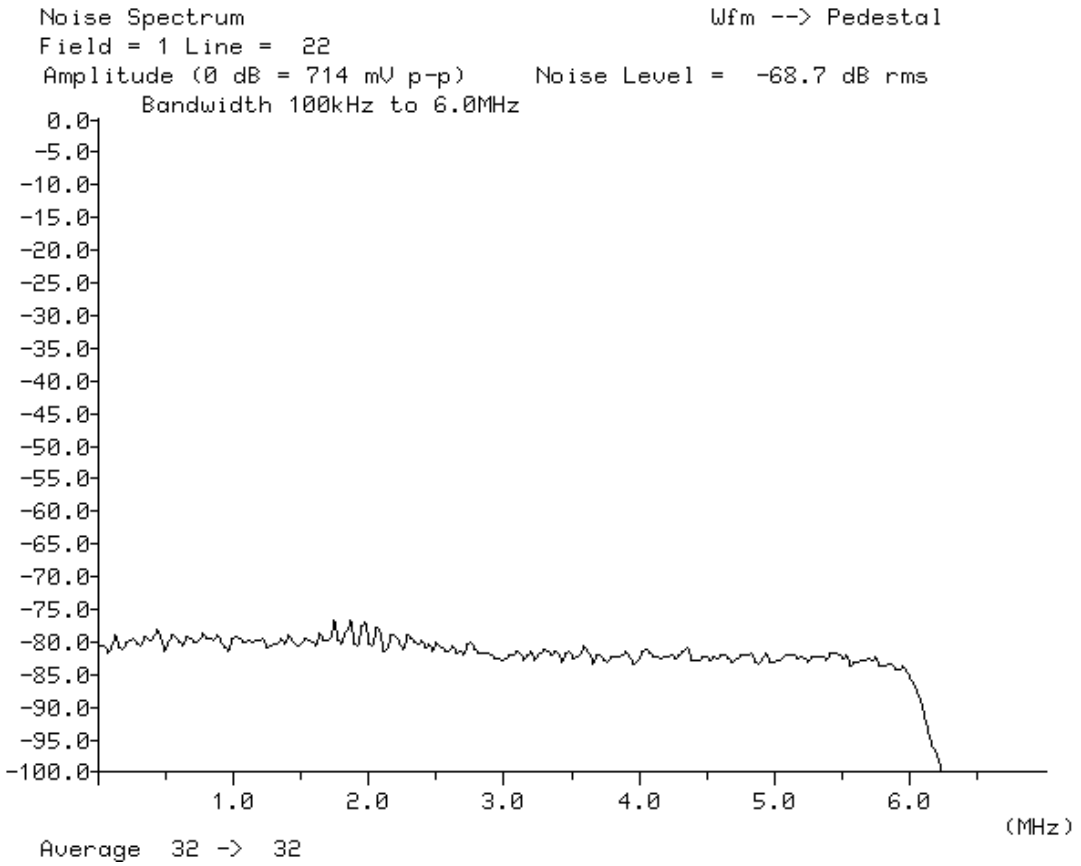


Figure 90.Noise Spectrum

- **DC**
  - Input signal : Field Square Wave

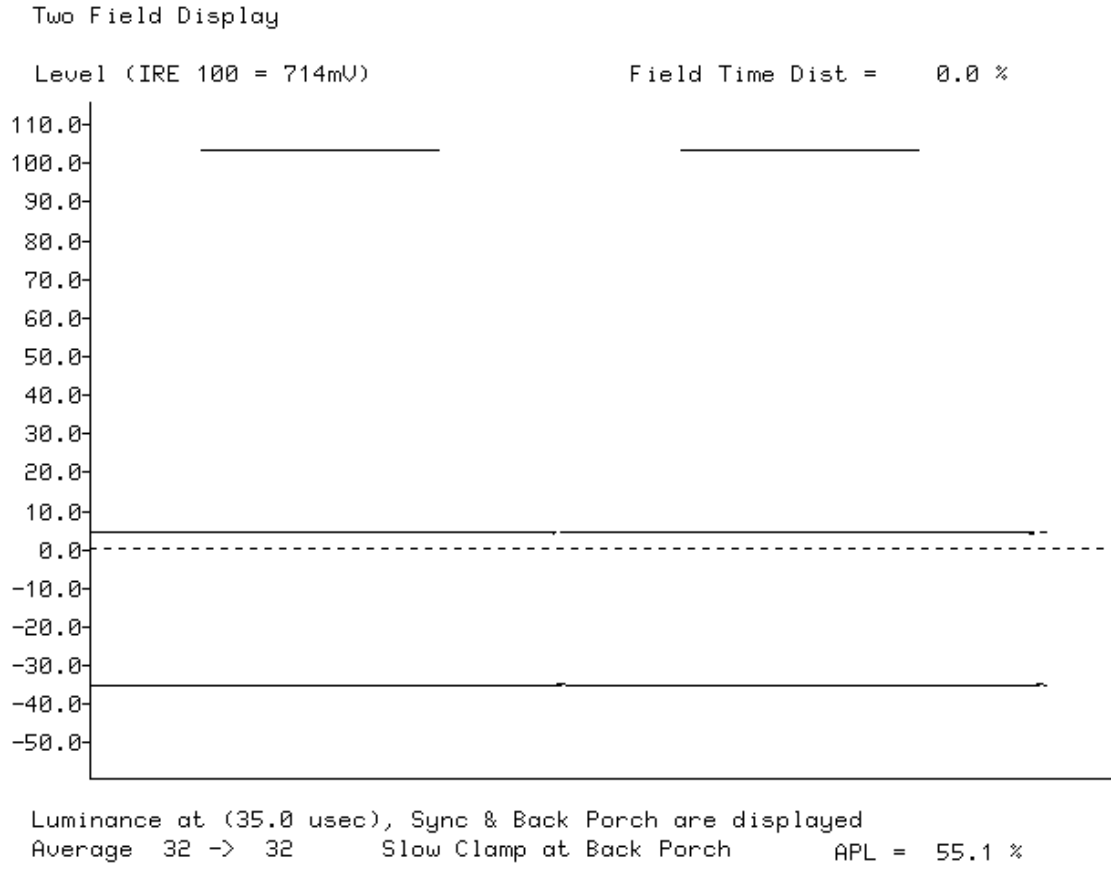


Figure 91.Field Time Distortion

・Vector

- Input signal : 75% Color Bar

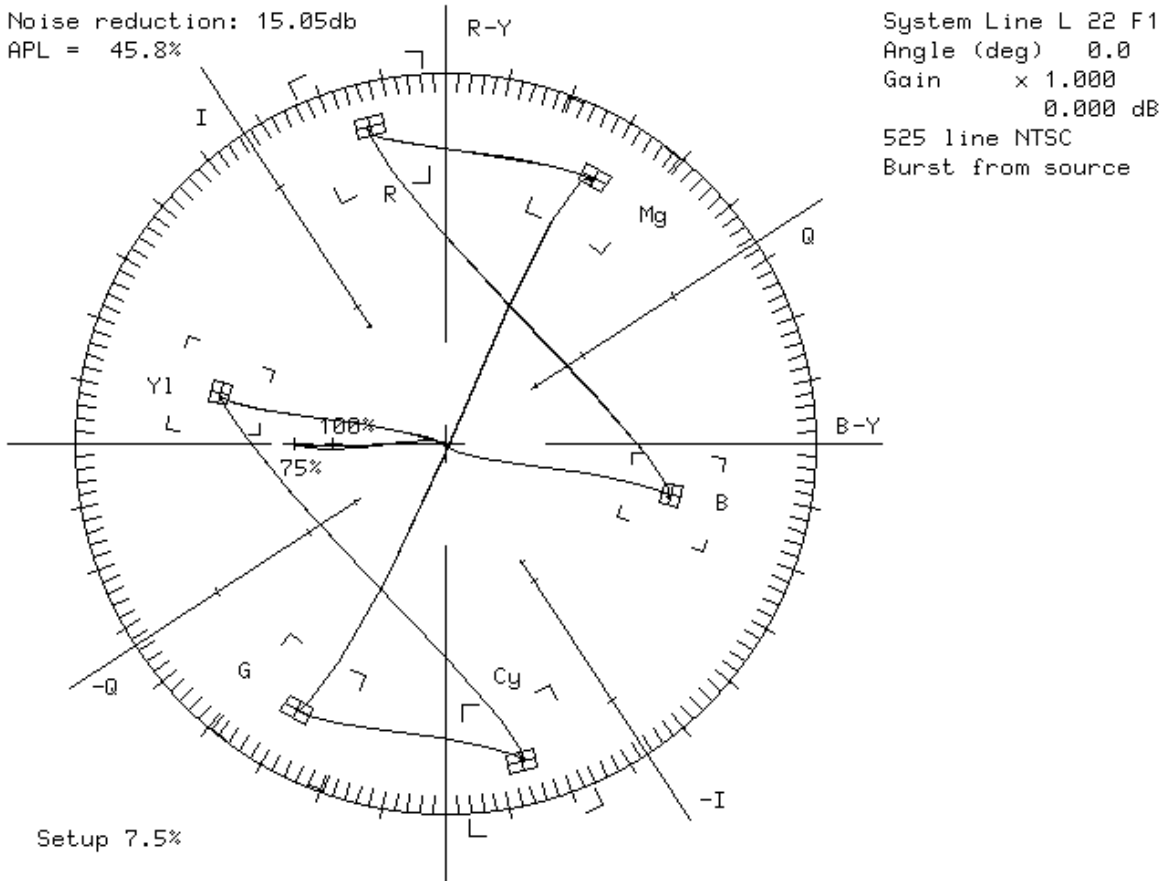
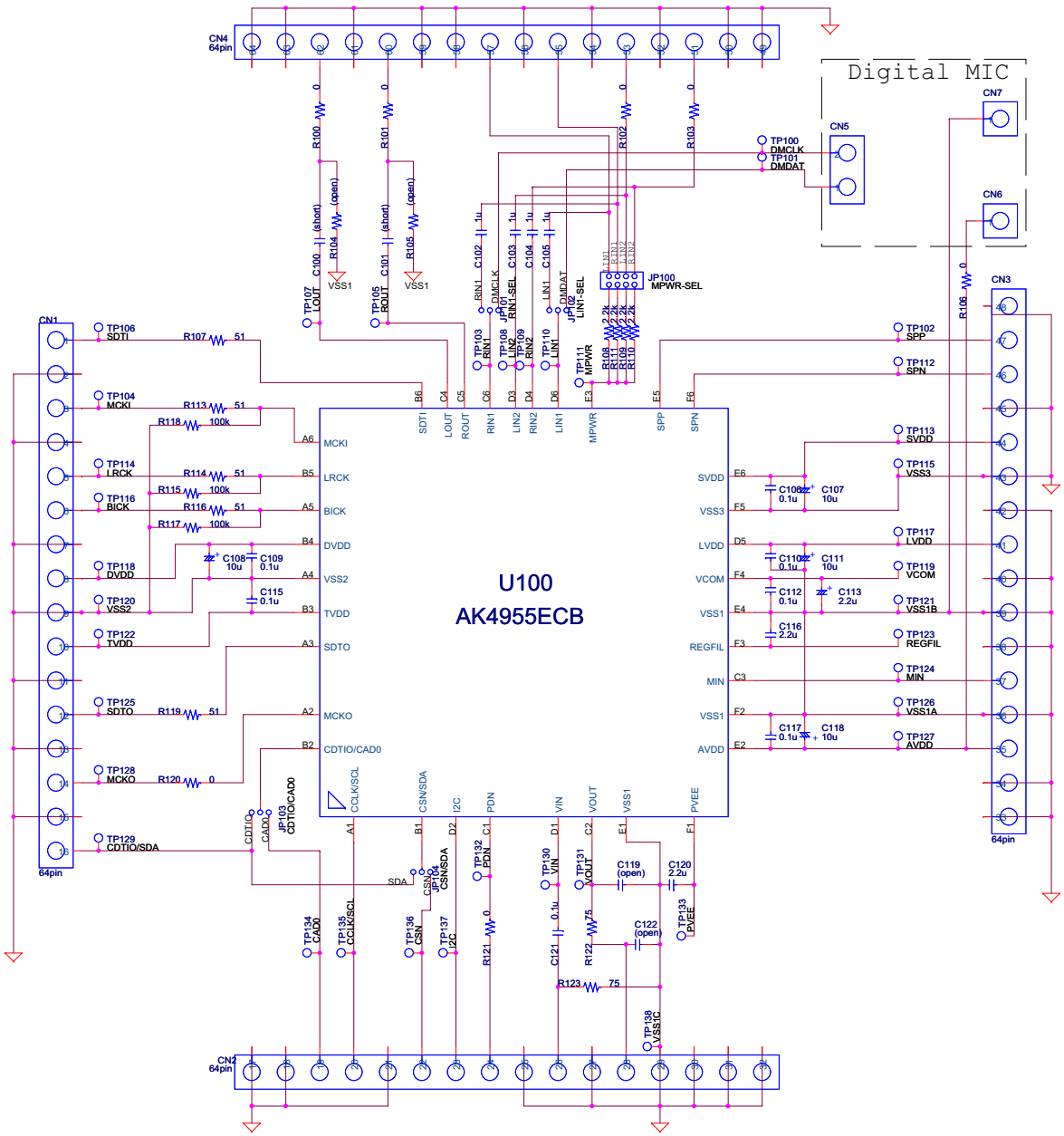


Figure 92.Vector

Revision History

Date (YY/MM/DD)	Manual Revision	Board Revision	Reason	Page	Contents
11/08/24	KM104703	3	First edition	-	



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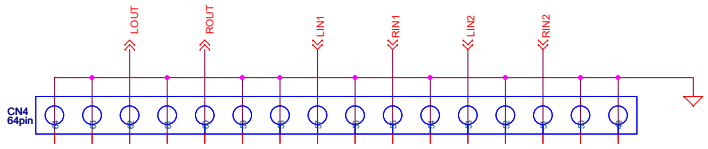

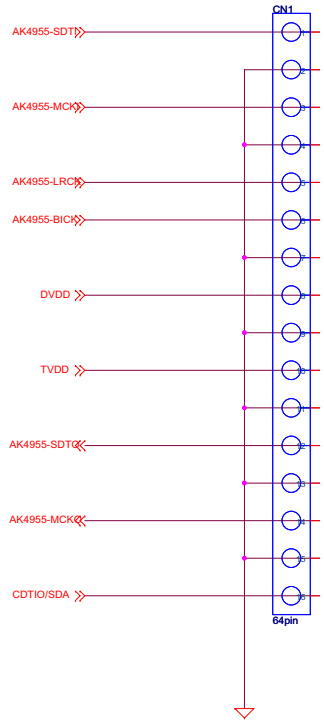

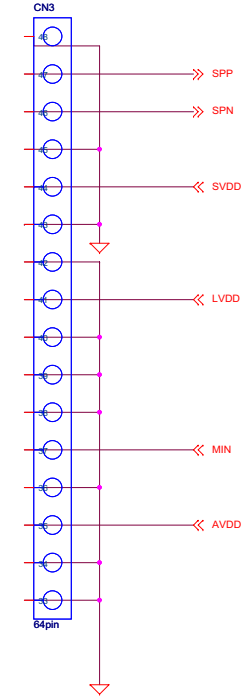

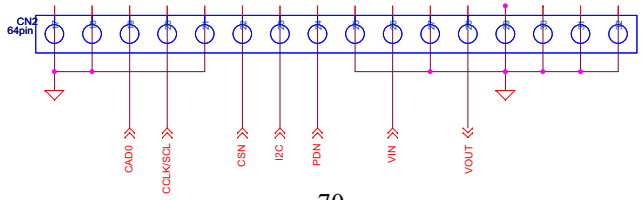

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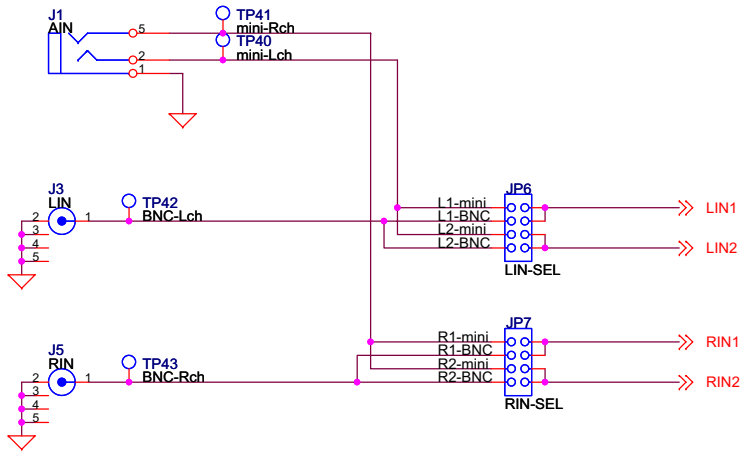

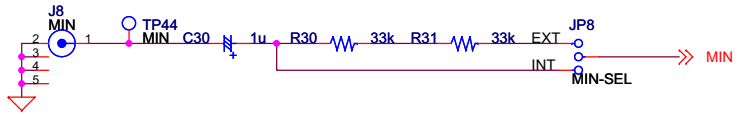

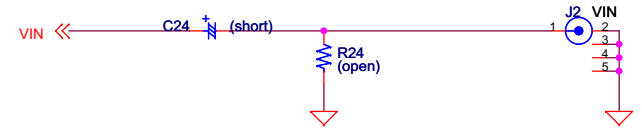

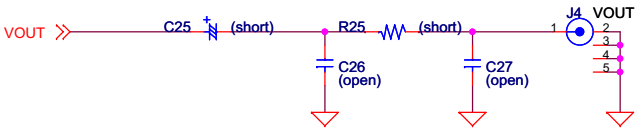

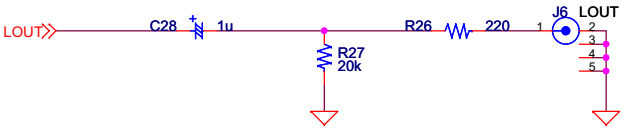

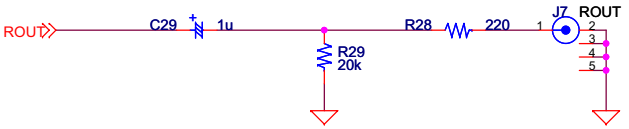

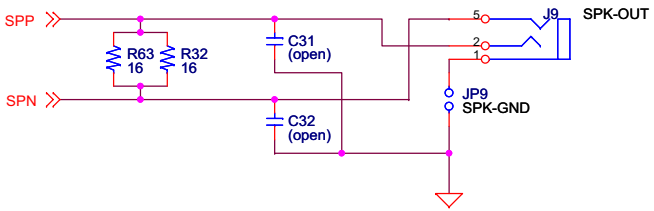

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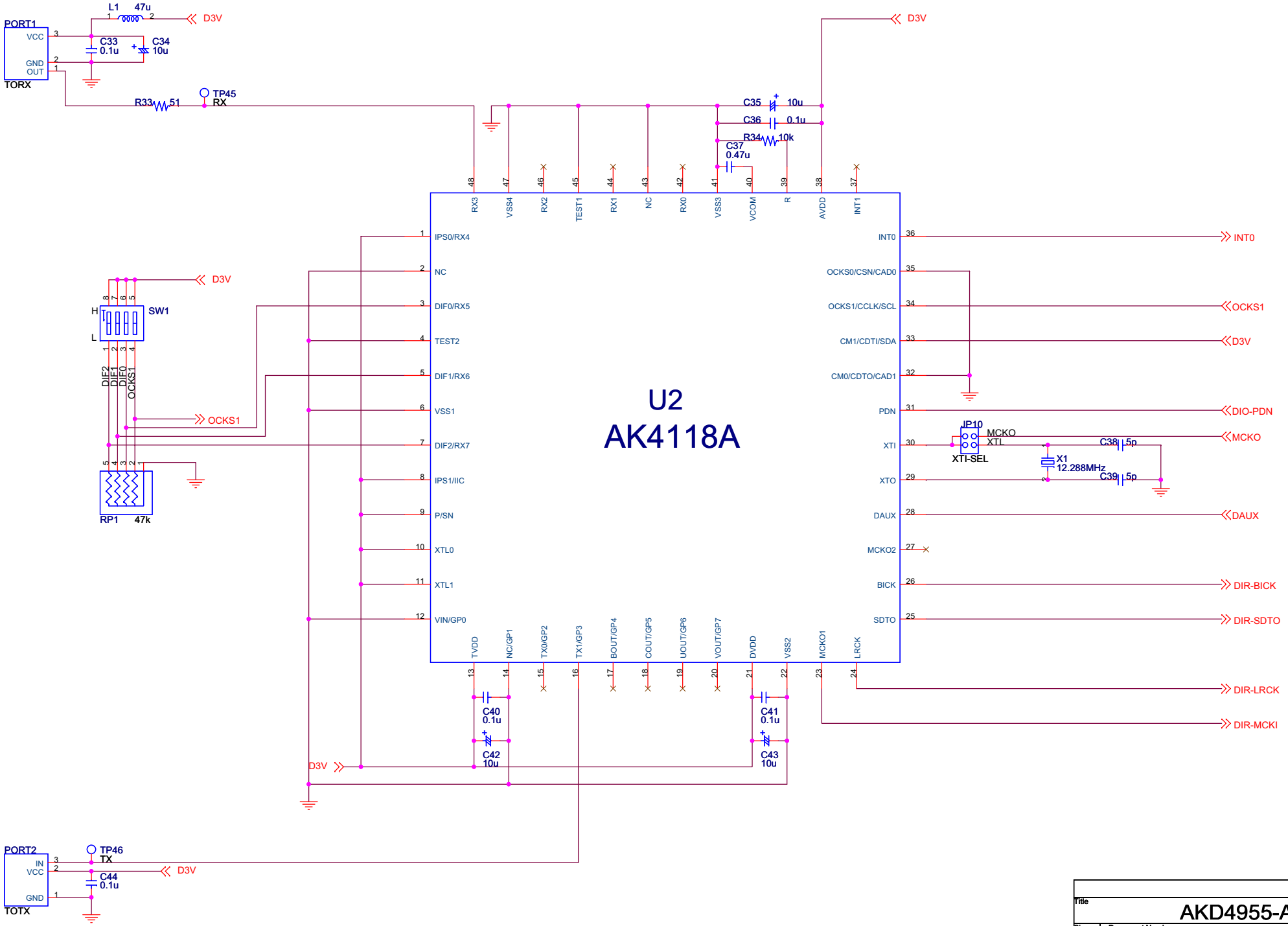

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Size A3	Document Number DIR/DIT	Rev 3
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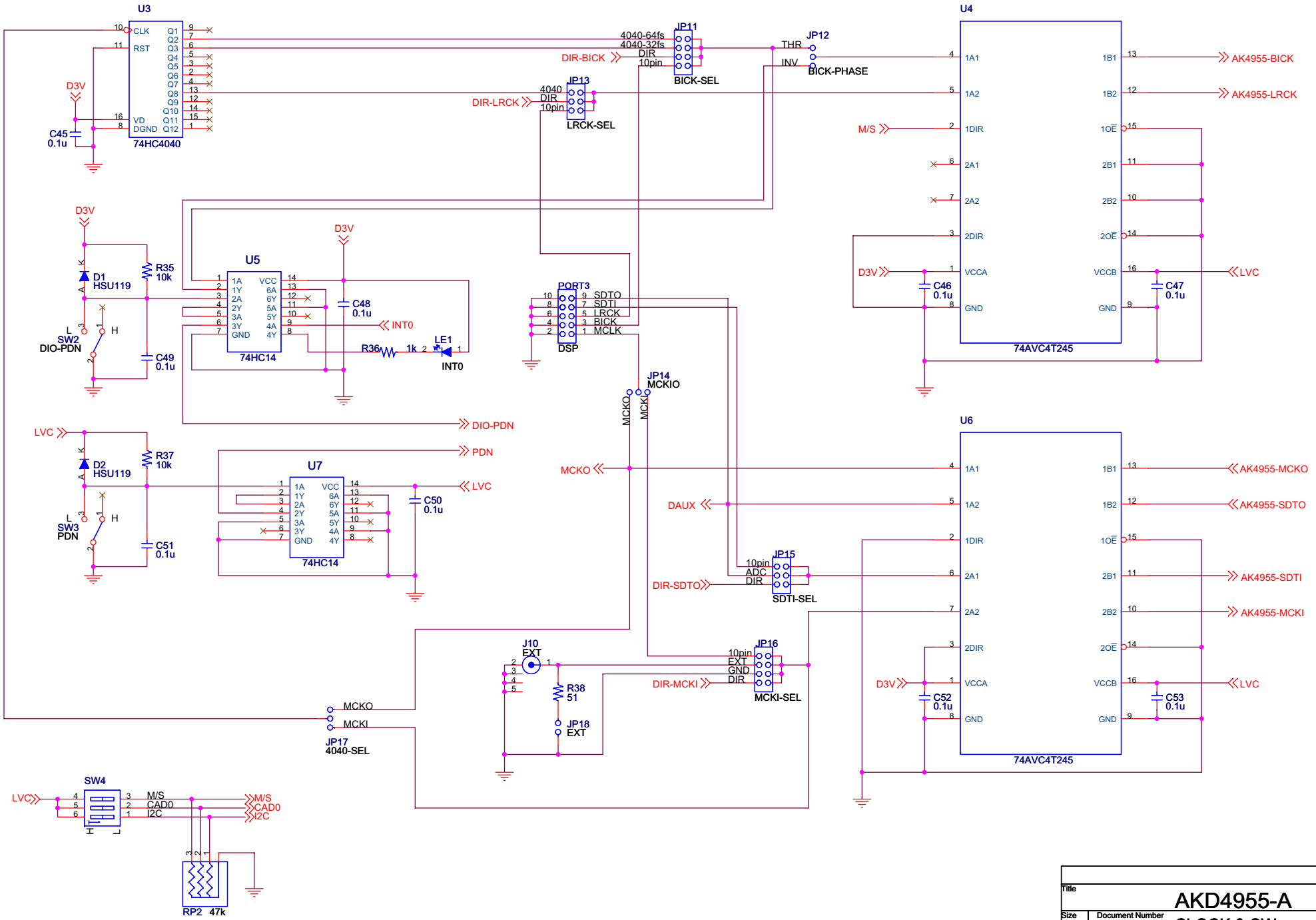

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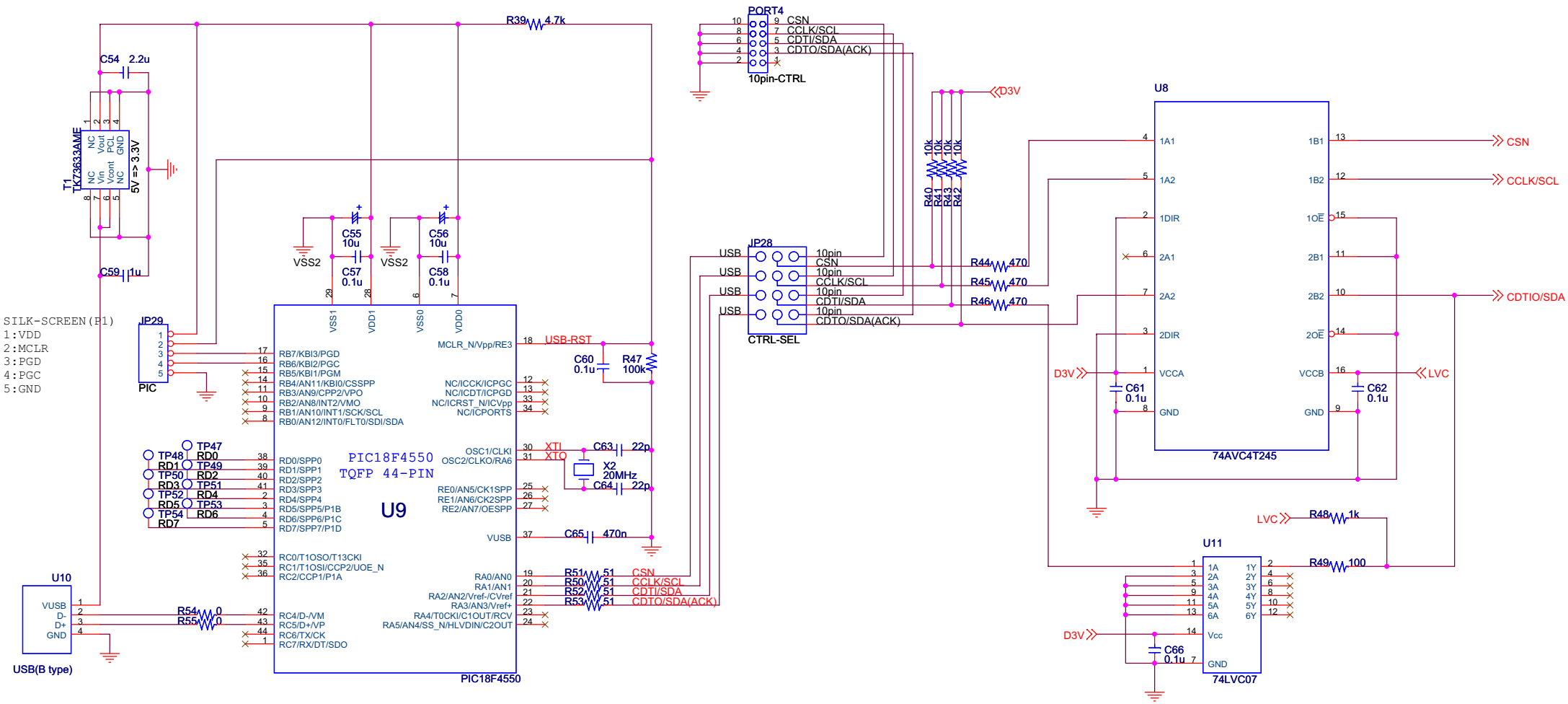

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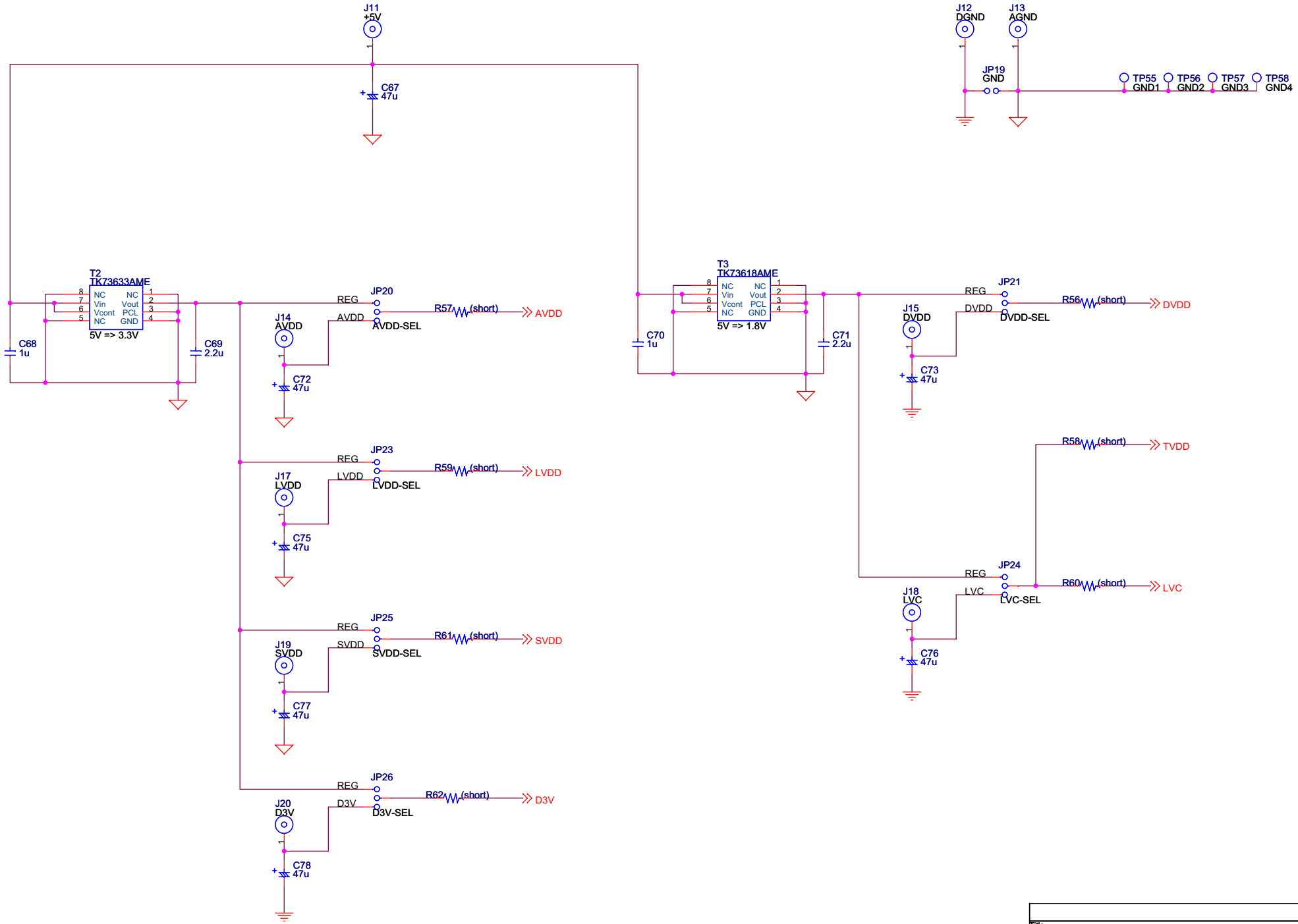
Size A3	Document Number uP-I/F	Rev 3
Date: Monday, November 29, 2010	Sheet 5 of 6	



Title	AKD4955-A	
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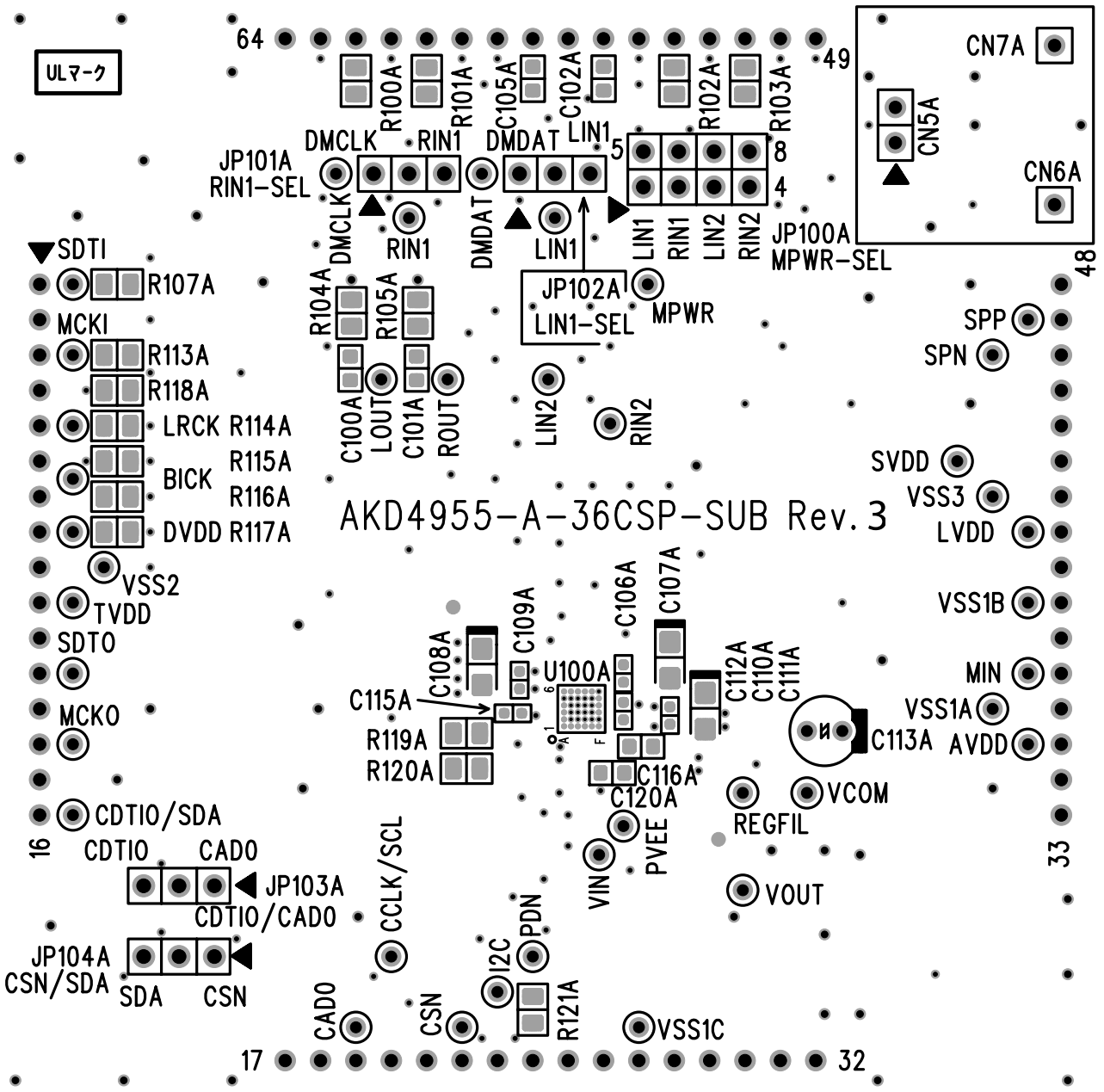
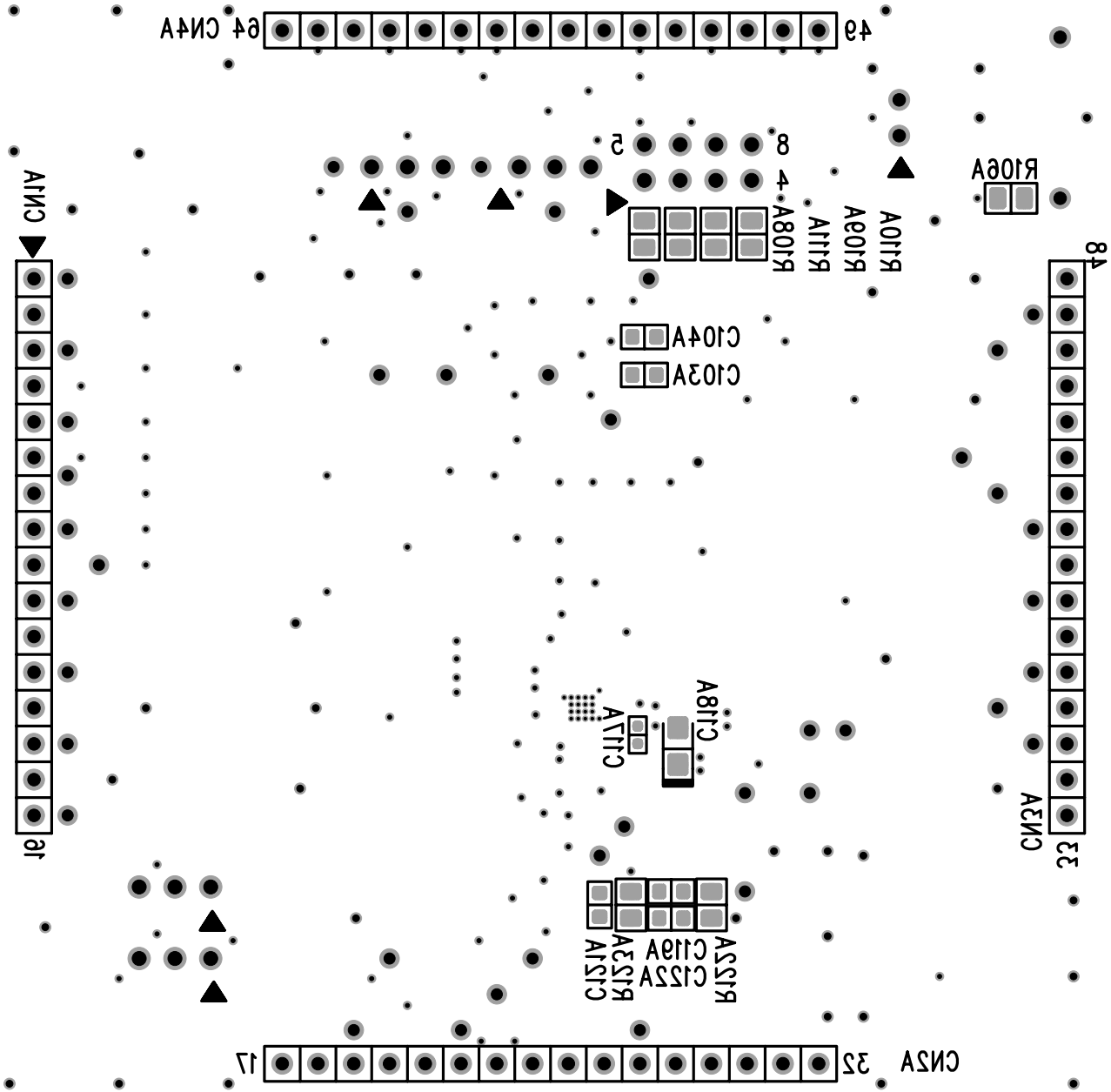
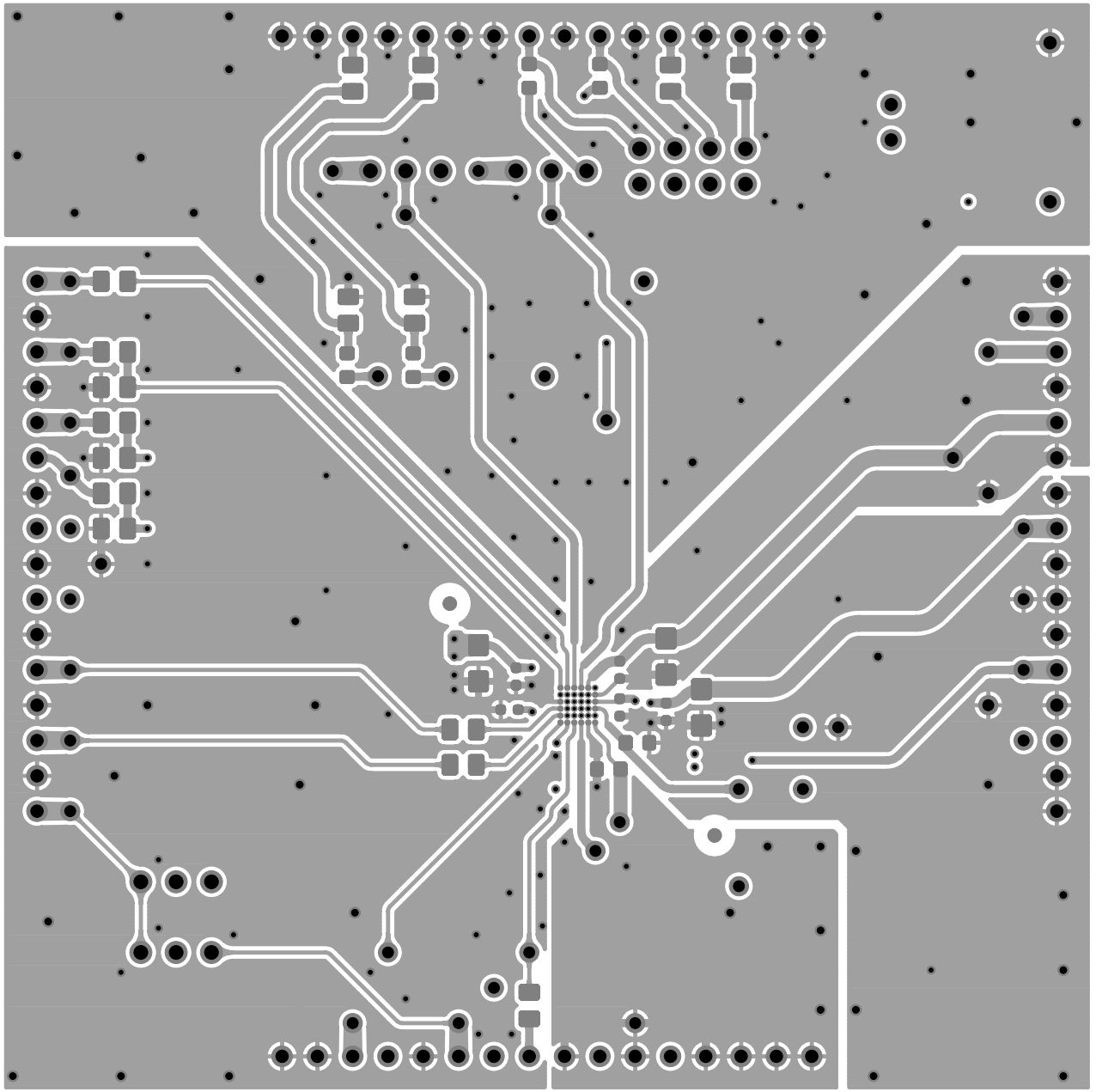
AKD4955-A Rev.3　部品面シルク図

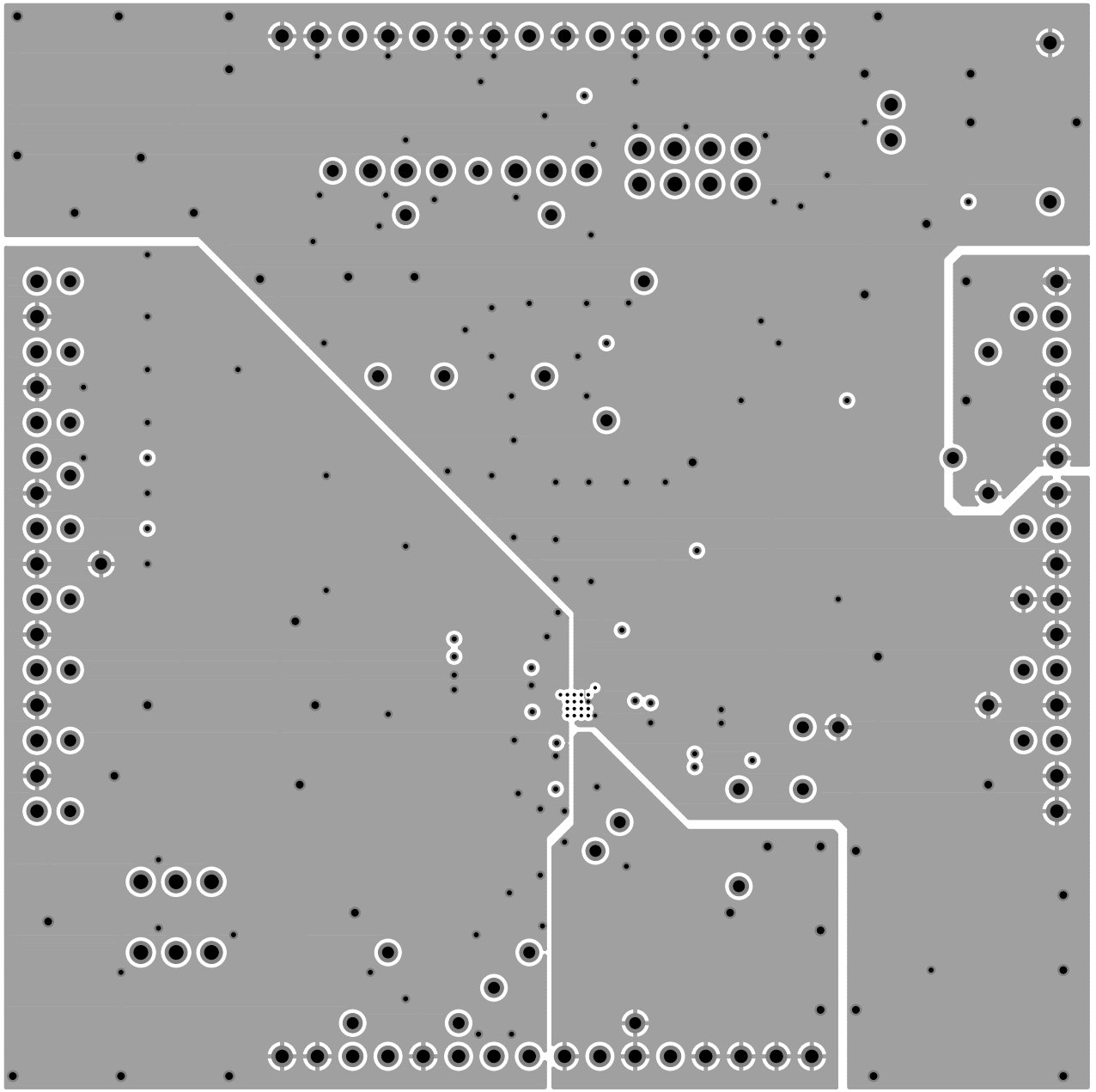


AKD4955-A Rev.3　半田面シルク図



部品面パターン図





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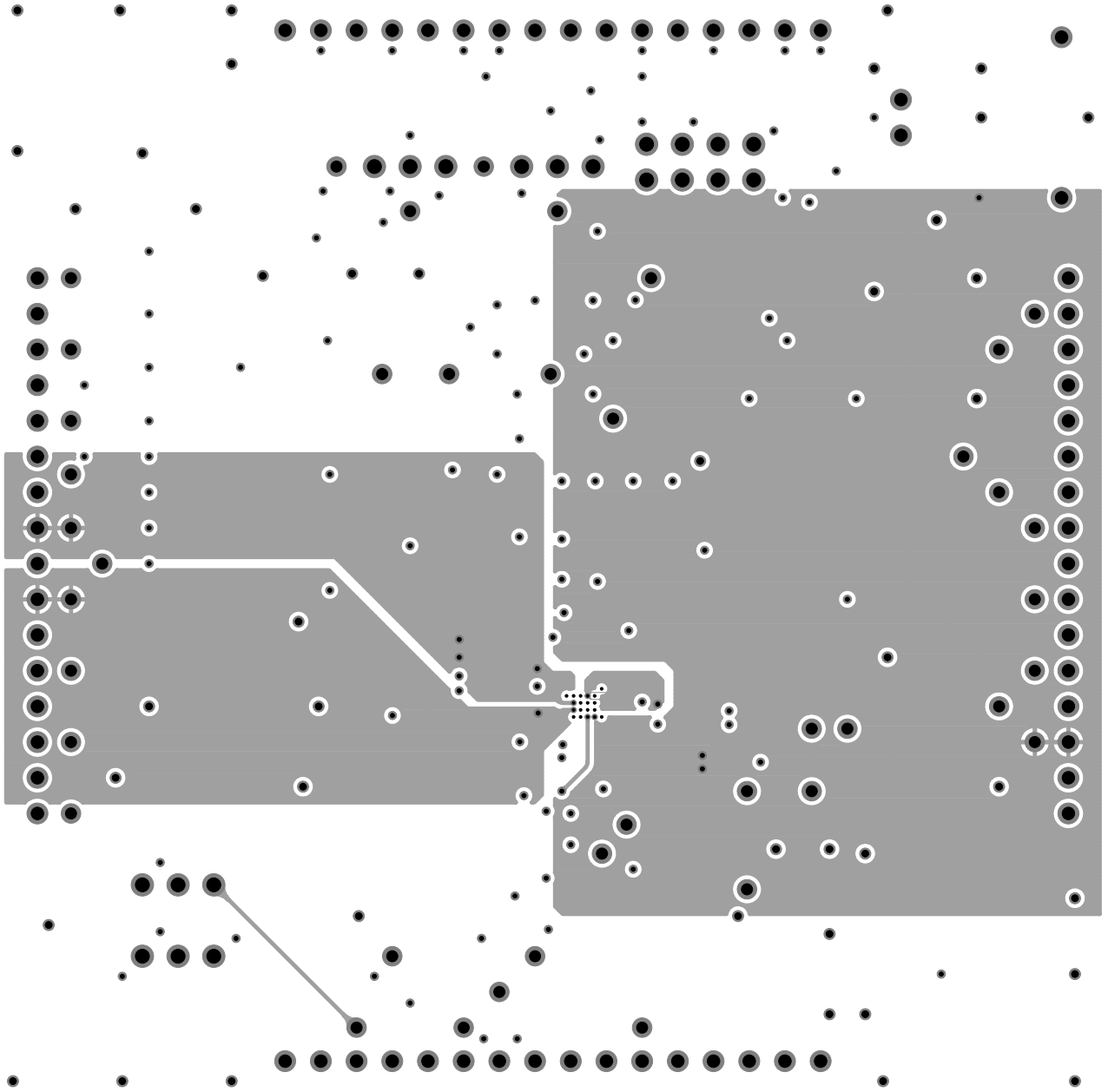

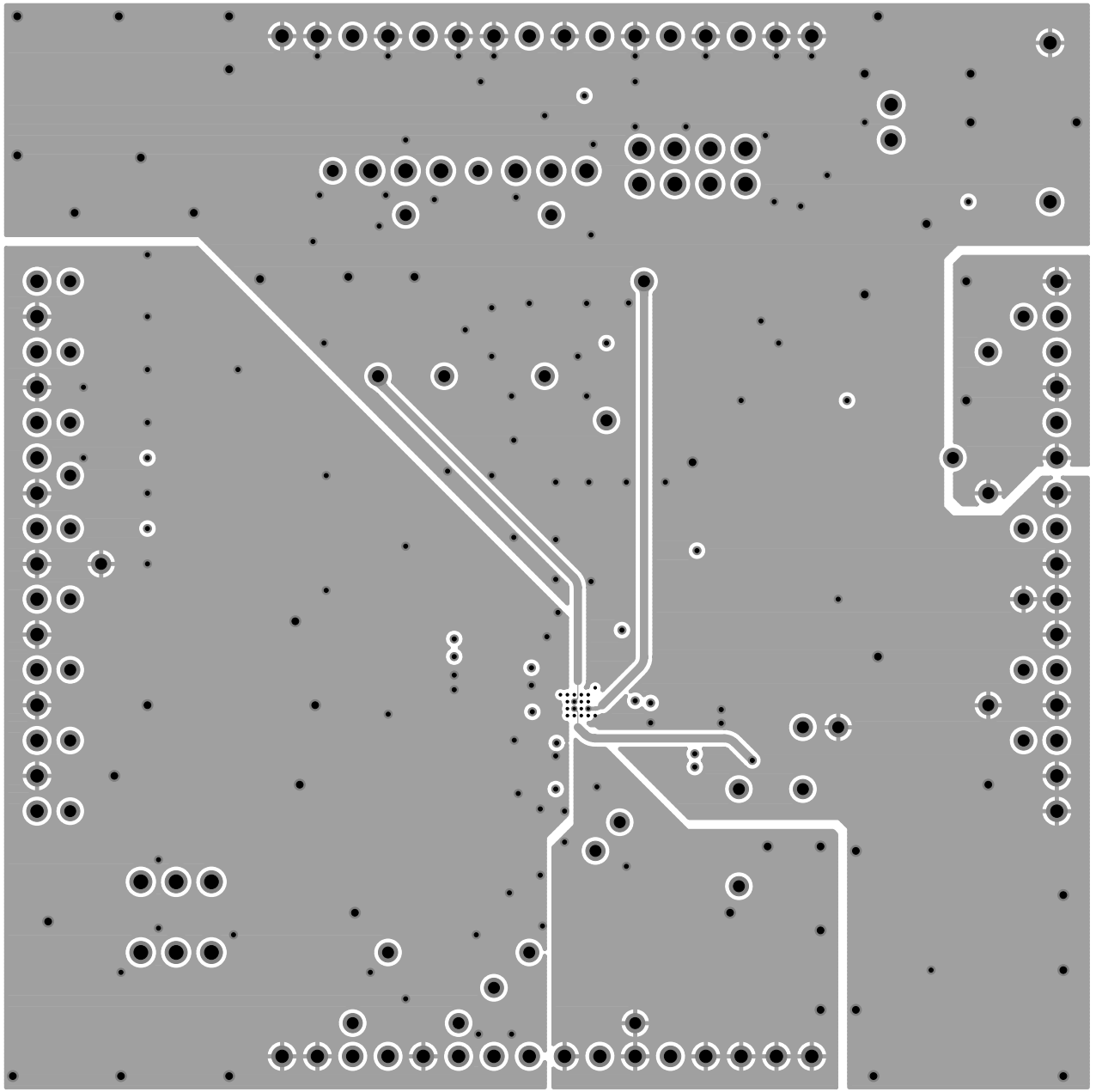

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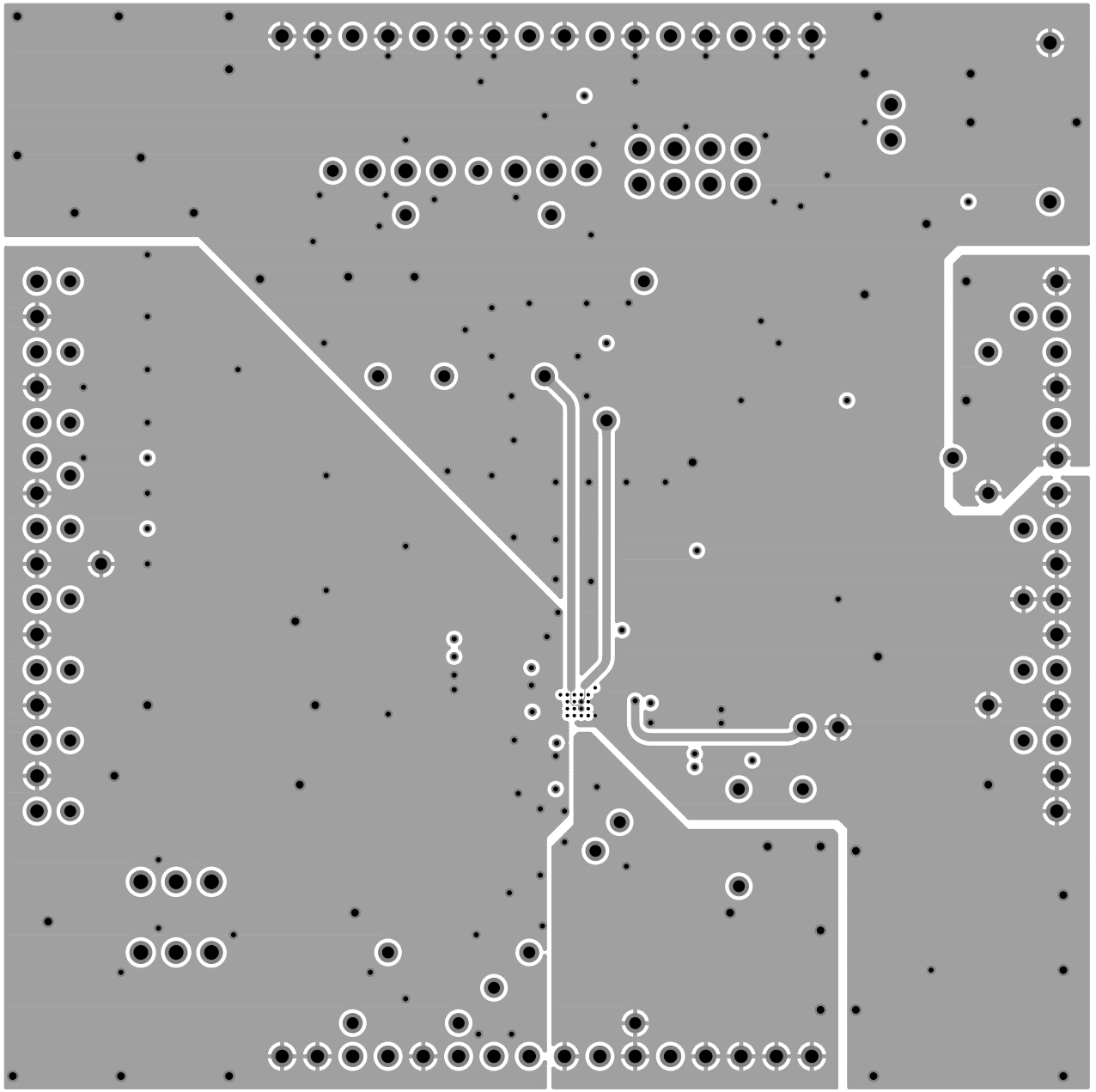

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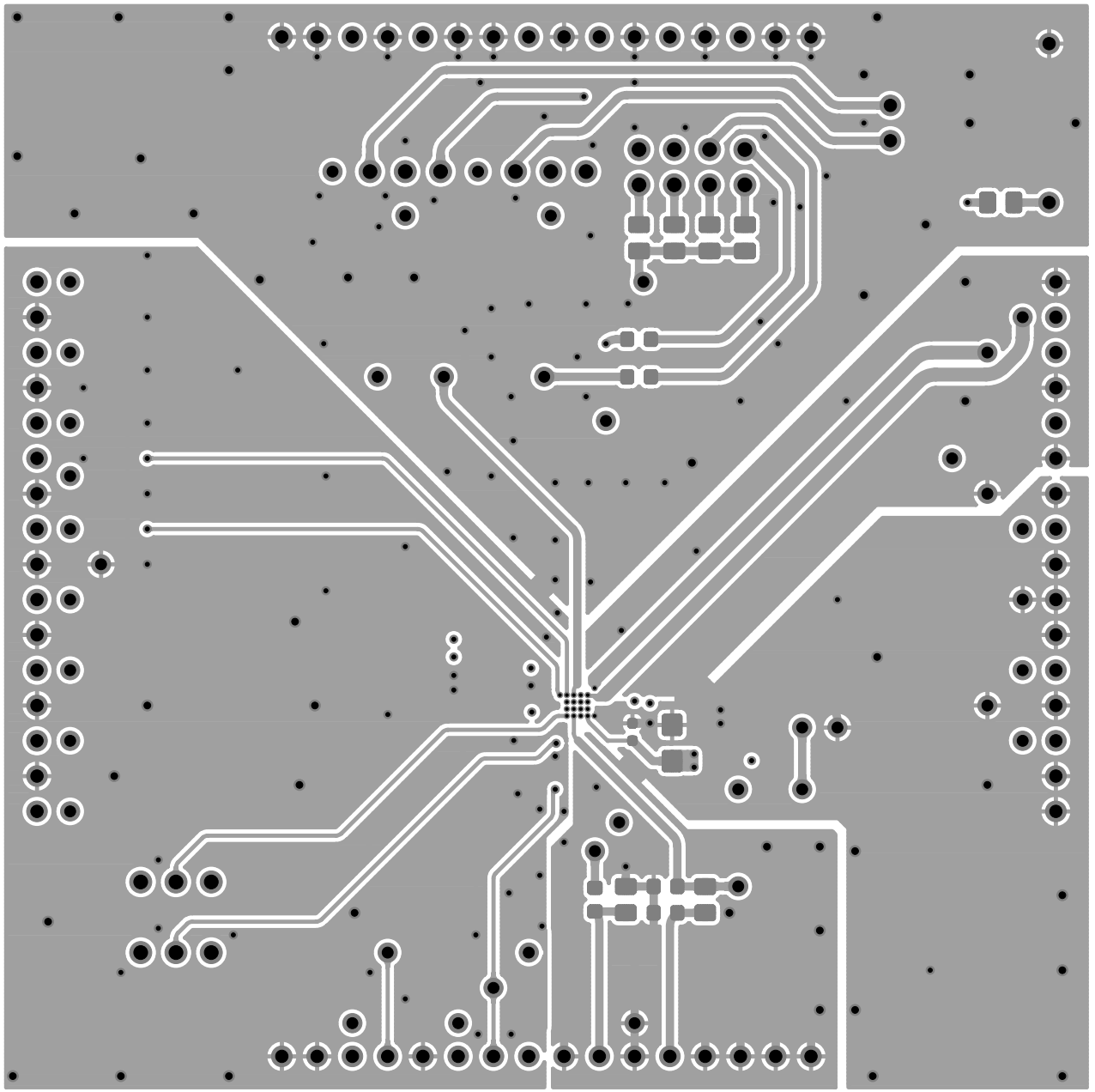

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