

10/100BASE PCMCIA Fast Ethernet MAC Controller

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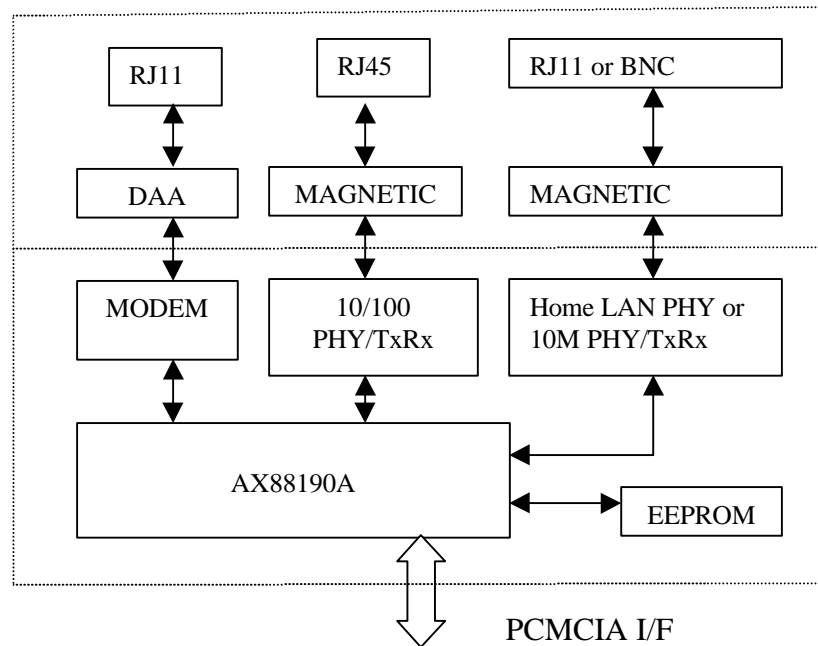
Features

- IEEE 802.3u 100BASE-T, TX, and T4 Compatible
 - Single chip PCMCIA bus 10/100Mbps Fast Ethernet MAC Controller
 - Embedded 8K * 16 bit SRAM
 - NE2000 register level compatible instruction
 - Compliant with 16 bit PC Card Standard - February 1995
 - Support both 10Mbps and 100Mbps data rate
 - Support both full-duplex or half-duplex operation
 - Provides a MII port for both 10/100Mbps operation
 - Provides SNI I/F for Home LAN PHY or 10M transceiver option
 - Support 128/256 bytes EEPROM (used for saving CIS)
 - Support automatic loading of Ethernet ID, CIS and Adapter Configuration from EEPROM on power-on initialization
 - External and internal loop-back capability
 - Support 8 General Purpose I/O ports
 - 128-pin LQFP low profile package
 - 20MHz to 25MHz Operation, Dual 5V and 3.3V CMOS process with 5V I/O tolerance. Or pure 3.3V operation
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Product description

The AX88190A Fast Ethernet Controller is a high performance and highly integrated PCMCIA bus Ethernet Controller with embedded 8K*16 bit SRAM. The AX88190A contains a 16 bit PCMCIA interfaces to host CPU and compliant with PC Card Standard – February 1995. The AX88190A implements both 10Mbps and 100Mbps Ethernet function based on IEEE802.3 / IEEE802.3u LAN standard. The AX88190A supports 10Mbps/100Mbps media-independent interface (MII) and legacy pure 10Mbps SNI interface to simplify the design. Using Serial Network Interface (SNI) transceiver, Home LAN PHY or 10BASE-2 BNC type media can be supported. The AX88190A is built in interface to connect FAX/MODEM chipset with parallel bus interface.

System Block Diagram



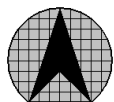
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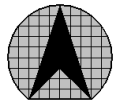


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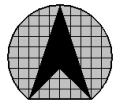


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1.0 Introduction

1.1 General Description:

The AX88190A provides industrial standard NE2000 registers level compatible instruction set. Various drivers are easy acquired, maintenance and usage with no pain and tears

The AX88190A Fast Ethernet Controller is a high performance and highly integrated PCMCIA bus Ethernet Controller with embedded 8K*16 bit SRAM. The AX88190A contains a 16 bit PCMCIA interfaces to host CPU and compliant with PC Card Standard – February 1995. The AX88190A implements both 10Mbps and 100Mbps Ethernet function based on IEEE802.3 / IEEE802.3u LAN standard. The AX88190A support 10Mbps/100Mbps media-independent interface (MII) and legacy pure 10Mbps SNI interface to simplify the design. Using Serial Network Interface (SNI) transceiver, Home LAN PHY or 10BASE-2 BNC type media can be supported. The AX88190A is built in interface to connect FAX/MODEM chipset with parallel bus interface.

The main difference between AX88190A and AX88190 are : 1) Replace memory I/F with SNI I/F. 2) Fix OE# signal synchronous problem 3) Fix interrupt status can't always clean up problem of AX88190. 4) Add 8 general Purpose I/O ports. 5) Change MPD_SET (pin 74 -> pin 68) and PPD_SET (pin 76 -> pin 70) power on setup pins location.

AX88190A use 128-pin LQFP low profile package, typical 25MHz operation, dual 5V and 3.3V CMOS process with 5V I/O tolerance or pure 3.3V operation.

1.2 AX88190A Block Diagram:

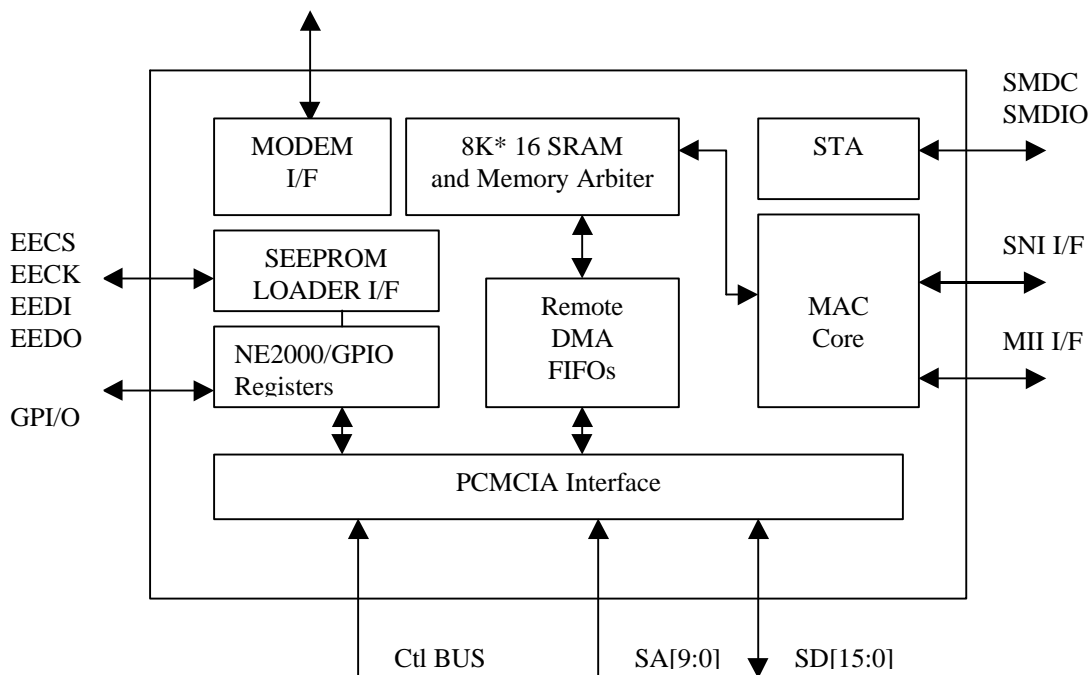
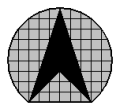


Fig - 1 AX88190A Block Diagram



1.3 AX88190A Pin Connection Diagram

The AX88190A is housed in the 128-pin plastic light quad flat pack. See Fig - 2 AX88190A Pin Connection Diagram.

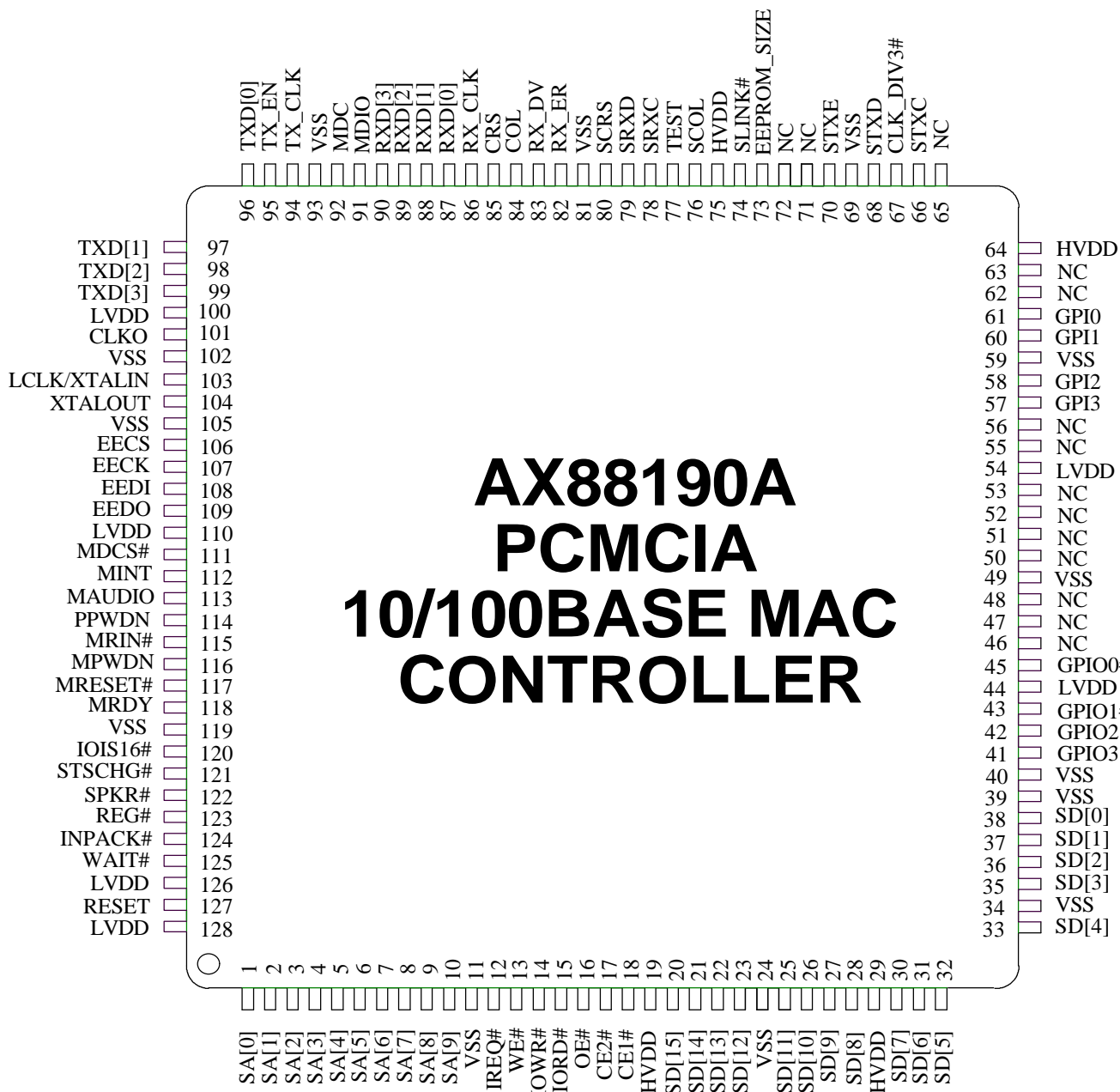
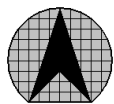


Fig - 2 AX88190A Pin Connection Diagram



2.0 Signal Description

The following terms describe the AX88190A pin-out:

All pin names with the “#” suffix are asserted low.

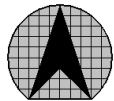
The following abbreviations are used in following Tables.

| | | | |
|------------|---------------------|-----------|------------------|
| I | Input | PU | Pull Up |
| O | Output | PD | Pull Down |
| I/O | Input/Output | P | Power Pin |
| OD | Open Drain | | |

2.1 PCMCIA Bus Interface Signals Group

| SIGNAL | TYPE | PIN NO. | DESCRIPTION |
|--------------|------|---|---|
| SA[9:0] | I | 10 – 1 | System Address : Signals SA[9:0] are address bus input lines which enable direct address of up to 64K memory and I/O spaces on card. |
| SD[15:0] | I/O | 20 – 23, 25 – 38, 30 – 33, 35 – 38 | System Data Bus : Signals SD[15:0] constitute the bi-directional data bus. |
| IREQ# | O | 12 | Interrupt Request : IREQ# is asserted to indicate the host system that the PC Card device requires host software service. |
| WAIT# | O | 125 | Wait : This signal is set low to insert wait states during Remote DMA transfer. |
| REG# | I | 123 | Attribute Memory and I/O Space Select : When the REG# signal is asserted, access is limited to Attribute Memory and to the I/O space. |
| IORD# | I | 15 | I/O Read : The host asserts IORD# to read data from AX88190A I/O space. |
| IOWR# | I | 14 | I/O Write : The host asserts IOWR# to write data into AX88190A I/O space. |
| OE# | I | 16 | Output Enable : The OE# line is used to gate Memory Read data from memory on PC Card |
| WE# | I | 13 | Write Enable : The WE# signal is used for strobing Memory Write data into the memory on PC Card. |
| IOIS16# | O | 120 | I/O is 16 Bit Port : The IOIS16# is asserted when the address at the socket corresponds to an I/O address to which the card responds, and the I/O port addressed is capable of 16-bit access. |
| INPACK# | O | 124 | Input Port Acknowledge : The signal is asserted when the AX88190A is selected and can respond to and I/O read cycle at the address on the address bus. |
| CE1#-CE2# | I | 18, 17 | Card Enable : The CE1# enables even numbered address bytes and CE2# enables odd numbered address bytes |
| BVD1_STSCHG# | O | 121 | Battery Voltage Detect 1 / Status Change |
| BVD2_SPKR# | O | 122 | Battery Voltage Detect 2 / Audio speaker out |

Tab - 1 PCMCIA bus interface signals group



2.2 EEPROM Signals Group

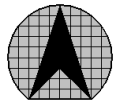
| SIGNAL | TYPE | PIN NO. | DESCRIPTION |
|--------|------|---------|---|
| EECS | O | 106 | EEPROM Chip Select : EEPROM chip select signal. |
| EECK | O | 107 | EEPROM Clock : Signal connected to EEPROM clock pin. |
| EEDI | O | 108 | EEPROM Data In : Signal connected to EEPROM data input pin. |
| EEDO | I/PU | 109 | EEPROM Data Out : Signal connected to EEPROM data output pin. |

Tab - 2 EEPROM bus interface signals group

2.3 MII interface signals group

| SIGNAL | TYPE | PIN NO. | DESCRIPTION |
|----------|--------|---------|---|
| RXD[3:0] | I | 90 – 87 | Receive Data : RXD[3:0] is driven by the PHY synchronously with respect to RX_CLK. |
| CRS | I | 85 | Carrier Sense : Asynchronous signal CRS is asserted by the PHY when either the transmit or receive medium is non-idle. |
| RX_DV | I | 83 | Receive Data Valid : RX_DV is driven by the PHY synchronously with respect to RX_CLK. Asserted high when valid data is present on RXD [3:0]. |
| RX_ER | I | 82 | Receive Error : RX_ER ,is driven by PHY and synchronous to RX_CLK, is asserted for one or more RX_CLK periods to indicate to the port that an error has detected. |
| RX_CLK | I | 86 | Receive Clock : RX_CLK is a continuous clock that provides the timing reference for the transfer of the RX_DV,RXD[3:0] and RX_ER signals from the PHY to the MII port of the repeater. |
| COL | I | 84 | Collision : this signal is driven by PHY when collision is detected. |
| TX_EN | O | 95 | Transmit Enable : TX_EN is transition synchronously with respect to the rising edge of TX_CLK. TX_EN indicates that the port is presenting nibbles on TXD [3:0] for transmission. |
| TXD[3:0] | O | 99 – 96 | Transmit Data : TXD[3:0] is transition synchronously with respect to the rising edge of TX_CLK. For each TX_CLK period in which TX_EN is asserted, TXD[3:0] are accepted for transmission by the PHY. |
| TX_CLK | I | 94 | Transmit Clock : TX_CLK is a continuous clock from PHY. It provides the timing reference for the transfer of the TX_EN and TXD[3:0] signals from the MII port to the PHY. |
| MDC | O | 92 | Station Management Data Clock : The timing reference for MDIO. All data transfers on MDIO are synchronized to the rising edge of this clock. MDC is a 2.5MHz frequency clock output. |
| MDIO | I/O/PU | 91 | Station Management Data Input / Output : Serial data input/output transfers from/to the PHYs . The transfer protocol conforms to the IEEE 802.3u MII specification. |

Tab - 3 MII interface signals group



2.4 SNI Interface pins group

| SIGNAL | TYPE | PIN NO. | DESCRIPTION |
|--------|------|---------|---|
| STXC | I | 66 | Transmit Clock : this signal is driven by PHY with 20MHz clock. |
| STXD | O | 68 | Transmit Data : STXD is transition synchronously with respect to the rising edge of STXC. For each STXC period in which STXE is asserted, STXD is accepted for transmission by the PHY. |
| STXE | O | 70 | Transmit Enable : STXE is transition synchronously with respect to the rising edge of STXC. STXE indicates that the port is presenting data on STXD for transmission. |
| SCOL | I | 76 | Collision : this signal is driven by PHY when collision is detected. |
| SRXC | I | 78 | Receive Clock : SRXC is driven by PHY for received data synchronization. |
| SRXD | I | 79 | Receive Data : SRXD is driven by the PHY synchronously with respect to SRXC. |
| SCRS | I | 80 | Carrier Sense : Asynchronous signal SCRS is asserted by the PHY when either the transmit or receive medium is non-idle. |
| SLINK# | I/PU | 74 | Link indicator : Active low indicate the SNI interface is link to network. When SNI is not used must keep the pin no connection or pull high the signal. |

Tab - 4 Serial Network Interface pins group

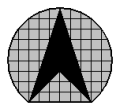
2.5 Modem interface pins group

| Signal Name | Type | Pin No. | Description |
|-------------|------|---------|---|
| MRDY | I/PU | 118 | Modem Ready : MRDY low indicates that modem is initializing the modem after reset signal asserted or the modem is at SLEEP/STOP mode. |
| MRESET# | O | 117 | Modem Reset :This signal asserts low to reset the modem chipset. |
| MDCS# | O | 111 | Modem Chip Select : This signal connected to modem chip select pin. |
| MPWDN | O | 116 | Modem Power Down : Rockwell modem chipset, this signal asserts low to let modem chipset into power down mode. AT&T modem chipset, this signal asserts high to let modem chipset into power down mode. |
| MINT | I/PD | 112 | Modem Interrupt : This signal driven by modem chipset to active interrupt. |
| MRIN# | I/PU | 115 | Ring Input :This signal is driven by DAA's ring detect circuit. When a telephone ringing signal is being received. |
| MAUDIO | I/PD | 113 | Modem Audio : This signal is passed to PCMCIA interface via SPKR. |

Tab - 5 Modem interface signals group

2.6 General Purpose I/O pins group

| Signal Name | Type | Pin No. | Description |
|-------------|------|---------|---|
| GPI[3] | I | 57 | Read register offset 18h bit 3 value reflects this input value. |
| GPI[2] | I | 58 | Read register offset 18h bit 2 value reflects this input value. |
| GPI[1] | I | 60 | Read register offset 18h bit 1 value reflects this input value. |
| GPI[0] | I | 61 | Read register offset 18h bit 0 value reflects this input value. |



| | | | |
|--------|-----|----|---|
| GPIO3# | I/O | 41 | Default "1". The pin reflects register offset 1Ah bit 3 inverted value. |
| GPIO2 | I/O | 42 | Default "0". The pin reflects register offset 1Ah bit 2 value. |
| GPIO1# | I/O | 43 | Default "1". The pin reflects register offset 1Ah bit 1 inverted value. |
| GPIO0# | I/O | 45 | Default "1". The pin reflects register offset 1Ah bit 0 inverted value. |

Tab - 6 General Purpose I/O pins group

2.7 Miscellaneous pins group

| SIGNAL | TYPE | PIN NO. | DESCRIPTION |
|-------------|------|---|--|
| LCLK/XTALIN | I | 103 | CMOS Local Clock : Typical a 25Mhz clock, +/- 100 ppm, 40%-60% duty cycle. (See application note also) Crystal Oscillator Input : Typical a 25Mhz crystal, +/- 25 ppm can be connected across XTALIN and XTALOUT. |
| XTALOUT | O | 104 | Crystal Oscillator Output : Typical a 25Mhz crystal, +/- 25 ppm can be connected across XTALIN and XTALOUT. If a single-ended external clock (LCLK) is connected to XTALIN, the crystal output pin should be left floating. |
| CLKO | O | 101 | Clock Output : This clock is source from LCLK/XTALIN. |
| CLK_DIV3# | I/PU | 67 | Clock Divide 3 Enable : Active low to enable the divided 3 circuit. That internally divides LCLK/XTALIN input frequency by 3 and then feed into internal circuit for system clock used. Default value set to logic high, this function is disabled. |
| PPWDN | O | 114 | Phy Power Down : This pin connects to PHY chip power down mode control input. |
| RESET | I/PD | 127 | Reset Reset is active high then place AX88190A into reset mode immediately. During Falling edge the AX88190A loads the EEPROM data. |
| TEST# | I/PU | 77 | Test Pin : Active LOW The pin is just for test mode setting purpose only. Must be pull high when normal operation. |
| EEPROM SIZE | I/PU | 73 | EEPROM SIZE = 0 : 93C46 128 byte type EEPROM is used. EEPROM SIZE = 1 : 93C56 256 byte type EEPROM is used. |
| NC | N/A | 46-48, 50-53, 55-56, | No Connection : for manufacturing test only. |
| LVDD | P | 44, 54, 100, 110, 126, 128 | Power Supply : +3.3V DC. |
| HVDD | P | 19, 29, 64, 75 | Power Supply : +5V DC. Note : for pure 3.3V single power solution, all the HVDD pin can connect to +3.3V. Care should be taken that HVDD input power must be greater or equal (> =) than LVDD. |
| VSS | P | 11, 24, 34, 39, 40, 49, 59, 69, 81, 93, 102, 105, 119 | Power Supply : +0V DC or Ground Power. |

Tab - 7 Miscellaneous pins group

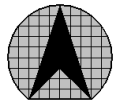


2.8 Power on configuration setup signals cross reference table

| Signal Name | Share with | Description |
|--------------------|-------------------|---|
| MPD_SET | STXD | MPD_SET = 0 : MPWDN pin active high. MPD_SET = 1 : MPWDN pin active low. |
| PPD_SET | STXE | PPD_SET = 0 : PPWDN pin active high. PPD_SET = 1 : PPWDN pin active low. |

All of the above signals are pull-up for default values.

Tab - 8 Power on Configuration Setup Table



3.0 Memory and I/O Mapping

There are four memory or I/O mapping used in AX88190A.

1. EEPROM Memory Mapping
2. Attribute Memory Mapping
3. I/O Mapping
4. Local Memory Mapping

3.1 EEPROM Memory Mapping

| EEPROM OFFSET | HIGH BYTE | LOW BYTE |
|----------------------|------------------|-----------------|
| 00H | RESERVED | WORD COUNT |
| 01H | CFH | CFL |
| 02H | NODE-ID1 | NODE ID 0 |
| 03H | NODE ID 3 | NODE ID 2 |
| 04H | NODE ID 5 | NODE ID 4 |
| 05H | CHECKSUM | RESERVED |
| 06H – 10H | RESERVED | RESERVED |
| 10H – FFH | CIS | CIS |

Tab - 9 EEPROM Memory Mapping

Note : bit 3 register of LCOR in AX88190 is replaced by bit 0 of CFL in AX88190A

Bit 0 of CFL : Enable Power Down mode

this bit is set to 1, the LAN will go into power down mode. At power down mode AX88190A will disable MAC transmitting and receiving operation. But the host interface will not be affected.

3.2 Attribute Memory Mapping

| ATTRIBUTE MEMORY OFFSET | CONTENTS |
|--------------------------------|-----------------|
| 0000H | CIS |
| 03BFH | |
| 03C0H | LCOR |
| 03C2H | LCCSR |
| 03C4H | - |
| 03C6H | - |
| 03CAH | LIOWBASE0 |
| 03CCH | LIOWBASE1 |
| 03CEH | RESERVED |
| 03DFH | |
| 03E0H | MCOR |
| 03E2H | MCCSR |
| 03E4H | - |
| 03E6H | - |
| 03EAH | MIOBASE0 |
| 03ECH | MIOBASE1 |
| 03EEH | RESERVED |
| 03FFH | |

Tab - 10 Attribute Memory Mapping



3.3 I/O Mapping

| SYSTEM I/O OFFSET | FUNCTION |
|-------------------|-------------------|
| 0000H 001FH | MAC CORE REGISTER |

Tab - 11 I/O Address Mapping

3.4 SRAM Memory Mapping

| OFFSET | FUNCTION |
|----------------|------------------------|
| 0000H 03BFH | CIS *1 |
| 03C0H | LCOR *1 |
| 03C2H | LCCSR *1 |
| 03C4H | - |
| 03C6H | - |
| 03CAH | LIODBASE0 *1 |
| 03CCH | LIODBASE1 *1 |
| 03CEH 03DFH | RESERVED |
| 03E0H | MCOR *1 |
| 03E2H | MCCSR *1 |
| 03E4H | - |
| 03E6H | - |
| 03EAH | MIOBASE0 *1 |
| 03ECH | MIOBASE1 *1 |
| 03EEH 03FFH | RESERVED |
| 0400H | NODE ID 0 |
| 0401H | NODE ID 1 |
| 0402H | NODE ID 2 |
| 0403H | NODE ID 3 |
| 0404H | NODE ID 4 |
| 0405H | NODE ID 5 |
| 0406H 07FFH | RESERVED |
| 4000H 7FFFH | 8K X 16 SRAM BUFFER |

Tab - 12 Local Memory Mapping



4.0 Registers Operation

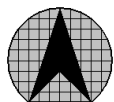
There are three register sets in AX88190A :

- The PCMCIA function configuration registers of LAN.
- The PCMCIA function configuration registers of MODEM.
- The MAC core register.

4.1 PCMCIA Function Configuration Register Set of LAN

| REGISTER | NAME | OFFSET |
|-----------------|-----------------------------------|---------------|
| LCOR | CONFIGURATION OPTION REGISTER | 3C0H |
| LCSR | CONFIGURATION AND STATUS REGISTER | 3C2H |
| LIORBASE0 | I/O BASED REGISTER 0 | 3CAH |
| LIORBASE1 | I/O BASED REGISTER 1 | 3CCH |

Tab - 13 PCMCIA Function Configuration Register Mapping of LAN

**4.1.1 Configuration Option Register of LAN (LCOR) Offset 3C0H (Read/Write)**

| FIELD | R/W/C | DESCRIPTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------------|--------------|---|--------------|------------------------------|-------|--------------|----------------|---|---|---|------|------------------------------|---|---|---|------|------|---|---|---|------|------|---|---|---|------|------|---|---|---|------|------------------------------|---|---|---|------|------|---|---|---|------|------|---|---|---|------|------|
| 7 | R/W | <p>Software Reset</p> <p>Assert this bit will reset the LAN function of AX88190A. Return a 0 to this bit will leave the LAN function of AX88190A in a post-reset state as same as that following a hardware reset. The value of this bit is 0 at power-on.</p> | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 6 | R/W | <p>Level IRQ</p> <p>This bit should be set to 1, the AX88190A always generates Level Mode Interrupt.</p> | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 5:0 | R/W | <p>Function Configuration Index</p> <p>These six bits are used to indicate entry of the card configuration table locate in the CIS. The default value is 0</p> <p>.</p> <p>On multifunction PC Card,</p> <p>Bit 5, Bit 4, Bit 3 : MODEM I/O base registers</p> <table border="0"> <thead> <tr> <th>Bit 5</th> <th>Bit 4</th> <th>Bit 3</th> <th>LAN I/O base</th> <th>MODEM I/O base</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>300H</td> <td>Decided by MIOBASE registers</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>320H</td> <td>2f8H</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>340H</td> <td>3e8H</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>360H</td> <td>2e8H</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>380H</td> <td>Decided by MIOBASE registers</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>200H</td> <td>2f8H</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>220H</td> <td>3e8H</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>240H</td> <td>2e8H</td> </tr> </tbody> </table> <p>Bit 2 : Enable IREQ# Routing If bit 0 of LCOR is set to 0, this bit is ignored. If bit 0 of LCOR is set to 1 and this bit is set to 1, the LAN will generate interrupt request via IREQ# signal. If this bit is set to 0, the LAN will not generate interrupt request via IREQ# line.</p> <p>Bit 1 : Enable Base and Limit Registers If bit 0 of LCOR is set to 0, this bit is ignored. If bit 0 of LCOR is set to 1 and this bit is set to 1, only I/O addresses that are qualified by the Base and Limit registers are passed to LAN function. If this bit is set to 0, all I/O addresses are passed to LAN function.</p> <p>Bit 0 : Enable Function If this bit is set to 0, the LAN function is disabled. If this bit is set to 1, the LAN function is enabled.</p> | Bit 5 | Bit 4 | Bit 3 | LAN I/O base | MODEM I/O base | 0 | 0 | 0 | 300H | Decided by MIOBASE registers | 0 | 0 | 1 | 320H | 2f8H | 0 | 1 | 0 | 340H | 3e8H | 0 | 1 | 1 | 360H | 2e8H | 1 | 0 | 0 | 380H | Decided by MIOBASE registers | 1 | 0 | 1 | 200H | 2f8H | 1 | 1 | 0 | 220H | 3e8H | 1 | 1 | 1 | 240H | 2e8H |
| Bit 5 | Bit 4 | Bit 3 | LAN I/O base | MODEM I/O base | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | 300H | Decided by MIOBASE registers | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 1 | 320H | 2f8H | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 0 | 340H | 3e8H | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 1 | 360H | 2e8H | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 0 | 380H | Decided by MIOBASE registers | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 1 | 200H | 2f8H | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 0 | 220H | 3e8H | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 1 | 240H | 2e8H | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

**4.1.2 Configuration and Status Register of LAN (LCSR) Offset 3C2H (Read/Write)**

| FIELD | R/W/C | DESCRIPTION |
|--------------|--------------|--|
| 7:3 | - | Reserved |
| 2 | R/W | PPwrDwn : PHY power down setting While this bit set to 1, PPWDN pin (pin 114) will be active to force PHY chip into power down mode. As for PPWDN is active high or active low. Please refer section 2.7 Power on configuration setup signal cross reference table. |
| 1 | R | Intr : Interrupt Request The LAN function will set this bit to 1 when it need interrupt service and set it to 0 when it is not request interrupt service. |
| 0 | R | IntrAck : Interrupt Acknowledge This bit will be 0. The Intr will reflect the status of interrupt requesting. |

4.1.3 I/O Base Register 0/1 of LAN (LIOBASE0/1) Offset 3CAH/3CCH (Read/Write)

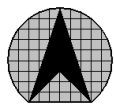
The I/O Base registers (LIOBASE0 and LIOBASE1) determine the base address of the I/O range used to access the LAN specific registers (MAC Core Registers).

I/O Base Register 0

| FIELD | R/W/C | DESCRIPTION |
|--------------|--------------|-----------------------------|
| 7:0 | R/W | Base I/O address bit 7 – 0. |

I/O Base Register 1

| FIELD | R/W/C | DESCRIPTION |
|--------------|--------------|------------------------------|
| 7:0 | R/W | Base I/O address bit 15 – 8. |



4.2 PCMCIA Function Configuration Register Set of MODEM

| REGISTER | NAME | OFFSET |
|-----------|-----------------------------------|--------|
| MCOR | CONFIGURATION OPTION REGISTER | 3E0H |
| MCSR | CONFIGURATION AND STATUS REGISTER | 3E2H |
| MIODBASE0 | I/O BASED REGISTER 0 | 3EAH |
| MIODBASE1 | I/O BASED REGISTER 1 | 3ECH |

Tab - 14 PCMCIA Function Configuration Register Mapping of MODEM

4.2.1 Configuration Option Register of MODEM (MCOR) Offset 3E0H (Read/Write)

| FIELD | R/W/C | DESCRIPTION |
|-------|-------|--|
| 7 | R/W | Software Reset Assert this bit will reset the MODEM function of AX88190A. Return a 0 to this bit will leave the MODEM function of AX88190A in a post-reset state as same as that following a hardware reset. The value of this bit is 0 at power-on. |
| 6 | R/W | Level IRQ This bit should be set to 1, the AX88190A always generates Level Mode Interrupt. |
| 5:0 | R/W | Function Configuration Index These six bits are used to indicate entry of the card configuration table locate in the CIS. The default value is 0 . On multifunction PC Card, Bit 5, Bit4 : Reserved Bit 3 : MINT route to STSCHG# If bit 0 of MCOR is set to 0, this bit is ignored. If both bit 0 and bit 2 of MCOR are set to 1 and this bit is set to 1, the MODEM will route interrupt request to STSCHG# signal. If this bit is set to 0, the MODEM will generate interrupt request via IREQ# line. Bit 2 : MINT route to IREQ# (Enable IREQ# Routing) If bit 0 of MCOR is set to 0, this bit is ignored. If bit 0 of MCOR is set to 1 and this bit is set to 1, the MODEM will generate interrupt request via IREQ# signal. If this bit is set to 0, the MODEM will not generate interrupt request via IREQ# line. Bit 1 : Enable Base and Limit Registers If bit 0 of MCOR is set to 0, this bit is ignored. If bit 0 of MCOR is set to 1 and this bit is set to 1, only I/O addresses that are qualified by the Base and Limit registers are passed to MODEM function. If this bit is set to 0, all I/O addresses are passed to LAN function. Bit 0 : Enable Function If this bit is set to 0, the MODEM function is disabled. If this bit is set to 1, the MODEM function is enabled. |

**4.2.2 Configuration and Status Register of MODEM (MCSR) Offset 3E2H (Read/Write)**

| FIELD | R/W/C | DESCRIPTION |
|--------------|--------------|--|
| 7:3 | - | Reserved |
| 2 | R/W | MPwrDwn : Modem power down setting While this bit set to 1, MPWDN pin (pin 116) will be active to force modem chip into power down mode. As for MPWDN is active high or active low. Please refer section 2.7 Power on configuration setup signal cross reference table. |
| 1 | R | Intr : Interrupt Request The LAN function will set this bit to 1 when it need interrupt service and set it to 0 when it is not request interrupt service. |
| 0 | R | IntrAck : Interrupt Acknowledge This bit will be 0. The Intr will reflect the status of interrupt requesting. |

4.2.3 I/O Base Register 0/1 of MODEM (MIOBASE0/1) Offset 3EAH/3ECH (Read/Write)

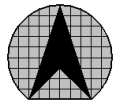
The I/O Base registers (MIOBASE0 and MIOBASE1) determine the base address of the I/O range used to access the MODEM specific registers.

I/O Base Register 0

| FIELD | R/W/C | DESCRIPTION |
|--------------|--------------|-----------------------------|
| 7:0 | R/W | Base I/O address bit 7 – 0. |

I/O Base Register 1

| FIELD | R/W/C | DESCRIPTION |
|--------------|--------------|------------------------------|
| 7:0 | R/W | Base I/O address bit 15 – 8. |



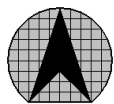
4.3 MAC Core Registers

All registers of MAC Core are 8-bit wide and mapped into pages which are selected by PS in the Command Register.

PAGE 0 (PS1=0,PS0=0)

| OFFSET | READ | WRITE |
|------------|---|--|
| 00H | Command Register (CR) | Command Register (CR) |
| 01H | Page Start Register (PSTART) | Page Start Register (PSTART) |
| 02H | Page Stop Register (PSTOP) | Page Stop Register (PSTOP) |
| 03H | Boundary Pointer (BNR) | Boundary Pointer (BNR) |
| 04H | Transmit Status Register (TSR) | Transmit Page Start Address (TPSR) |
| 05H | Number of Collisions Register (NCR) | Transmit Byte Count Register 0 (TBCR0) |
| 06H | Current Page Register (CPR) | Transmit Byte Count Register 1 (TBCR1) |
| 07H | Interrupt Status Register (ISR) | Interrupt Status Register (ISR) |
| 08H | Current Remote DMA Address 0 (CRDA0) | Remote Start Address Register 0 (RSAR0) |
| 09H | Current Remote DMA Address 1 (CRDA1) | Remote Start Address Register 1 (RSAR1) |
| 0AH | Reserved | Remote Byte Count 0 (RBCR0) |
| 0BH | Reserved | Remote Byte Count 1 (RBCR1) |
| 0CH | Receive Status Register (RSR) | Receive Configuration Register (RCR) |
| 0DH | Frame Alignment Errors (CNTR0) | Transmit Configuration Register (TCR) |
| 0EH | CRC Errors (CNTR1) | Data Configuration Register (DCR) |
| 0FH | Missed Packet Errors (CNTR2) | Interrupt Mask Register (IMR) |
| 10H 11H | Data Port | Data Port |
| 12H | IFGS1 | IFGS1 |
| 13H | IFGS2 | IFGS2 |
| 14H | MII/EEPROM Access | MII/EEPROM Access |
| 15H | - | Test Register |
| 16H | Inter-frame Gap (IFG) | Inter-frame Gap (IFG) |
| 17H – 18H | Reserved | Reserved |
| 19H | GPI | Reserved |
| 1AH | GPIO | GPIO |
| 1BH - 1EH | Reserved | Reserved |
| 1FH | Reset | Reserved |

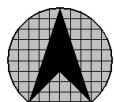
Tab - 15 Page 0 of MAC Core Registers Mapping



PAGE 1 (PS1=0,PS0=1)

| OFFSET | READ | WRITE |
|---------------|--|--|
| 00H | Command Register (CR) | Command Register (CR) |
| 01H | Physical Address Register 0 (PARA0) | Physical Address Register 0 (PAR0) |
| 02H | Physical Address Register 1 (PARA1) | Physical Address Register 1 (PAR1) |
| 03H | Physical Address Register 2 (PARA2) | Physical Address Register 2 (PAR2) |
| 04H | Physical Address Register 3 (PARA3) | Physical Address Register 3 (PAR3) |
| 05H | Physical Address Register 4 (PARA4) | Physical Address Register 4 (PAR4) |
| 06H | Physical Address Register 5 (PARA5) | Physical Address Register 5 (PAR5) |
| 07H | Current Page Register (CPR) | Current Page Register (CPR) |
| 08H | Multicast Address Register 0 (MAR0) | Multicast Address Register 0 (MAR0) |
| 09H | Multicast Address Register 1 (MAR1) | Multicast Address Register 1 (MAR1) |
| 0AH | Multicast Address Register 2 (MAR2) | Multicast Address Register 2 (MAR2) |
| 0BH | Multicast Address Register 3 (MAR3) | Multicast Address Register 3 (MAR3) |
| 0CH | Multicast Address Register 4 (MAR4) | Multicast Address Register 4 (MAR4) |
| 0DH | Multicast Address Register 5 (MAR5) | Multicast Address Register 5 (MAR5) |
| 0EH | Multicast Address Register 6 (MAR6) | Multicast Address Register 6 (MAR6) |
| 0FH | Multicast Address Register 7 (MAR7) | Multicast Address Register 7 (MAR7) |
| 10H 11H | Data Port | Data Port |
| 12H | Inter-frame Gap Segment 1 IFGS1 | Inter-frame Gap Segment 1 IFGS1 |
| 13H | Inter-frame Gap Segment 2 IFGS2 | Inter-frame Gap Segment 2 IFGS2 |
| 14H | MII/EEPROM Access | MII/EEPROM Access |
| 15H | - | Test Register |
| 16H | Inter-frame Gap (IFG) | Inter-frame Gap (IFG) |
| 17H – 18H | Reserved | Reserved |
| 19H | GPI | Reserved |
| 1AH | GPIO | GPIO |
| 1BH - 1EH | Reserved | Reserved |
| 1FH | Reset | Reserved |

Tab - 16 Page 1 of MAC Core Registers Mapping

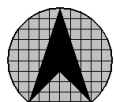


4.3.1 Command Register (CR) Offset 00H (Read/Write)

| FIELD | NAME | DESCRIPTION | | | | | | | | | | | | | | | | | | | | | | | | |
|-------|-------------|--|-----------------------------|-----|-----|---|---|--------|---|-------------|--------|---|---|-------------|---|---|---|--------------|---|---|---|-------------|---|---|---|-----------------------------|
| 7:6 | PS1,PS0 | PS1,PS0 : Page Select The two bit selects which register page is to be accessed. <table style="margin-left: 40px;"> <tr> <td>PS1</td> <td>PS0</td> <td></td> </tr> <tr> <td>0</td> <td>0</td> <td>page 0</td> </tr> <tr> <td>0</td> <td>1</td> <td>page 1</td> </tr> </table> | PS1 | PS0 | | 0 | 0 | page 0 | 0 | 1 | page 1 | | | | | | | | | | | | | | | |
| PS1 | PS0 | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | page 0 | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | page 1 | | | | | | | | | | | | | | | | | | | | | | | | |
| 5:3 | RD2,RD1,RD0 | RD2,RD1,RD0 : Remote DMA Command These three encoded bits control operation of the Remote DMA channel. RD2 could be set to abort any Remote DMA command in process. RD2 is reset by AX88190A when a Remote DMA has been completed. The Remote Byte Count should be cleared when a Remote DMA has been aborted. The Remote Start Address are not restored to the starting address if the Remote DMA is aborted. <table style="margin-left: 40px;"> <tr> <td>RD2</td> <td>RD1</td> <td>RD0</td> <td></td> </tr> <tr> <td>0</td> <td>0</td> <td>0</td> <td>Not allowed</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>Remote Read</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>Remote Write</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>Not allowed</td> </tr> <tr> <td>1</td> <td>X</td> <td>X</td> <td>Abort / Complete Remote DMA</td> </tr> </table> | RD2 | RD1 | RD0 | | 0 | 0 | 0 | Not allowed | 0 | 0 | 1 | Remote Read | 0 | 1 | 0 | Remote Write | 0 | 1 | 1 | Not allowed | 1 | X | X | Abort / Complete Remote DMA |
| RD2 | RD1 | RD0 | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | Not allowed | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 1 | Remote Read | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 0 | Remote Write | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 1 | Not allowed | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | X | X | Abort / Complete Remote DMA | | | | | | | | | | | | | | | | | | | | | | | |
| 2 | TXP | TXP : Transmit Packet This bit could be set to initiate transmission of a packet | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | START | START : This bit is used to active AX88190A operation. | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | STOP | STOP : Stop AX88190A This bit is used to stop the AX88190A operation. | | | | | | | | | | | | | | | | | | | | | | | | |

4.3.2 Interrupt Status Register (ISR) Offset 07H (Read/Write)

| FIELD | NAME | DESCRIPTION |
|-------|------|---|
| 7 | RST | Reset Status : Set when AX88190A enters reset state and cleared when a start command is issued to the CR. Writing to this bit is no effect. |
| 6 | RDC | Remote DMA Complete Set when remote DMA operation has been completed |
| 5 | CNT | Counter Overflow Set when MSB of one or more of the Tally Counters has been set. |
| 4 | OVW | Over Write : Set when receive buffer ring storage resources have been exhausted. |
| 3 | TXE | Transmit Error Set when packet transmitted with one or more of the following errors Excessive collisions FIFO Under-run |
| 2 | RXE | Receive Error Indicates that a packet was received with one or more of the following errors CRC error Frame Alignment Error FIFO Overrun Missed Packet |
| 1 | PTX | Packet Transmitted Indicates packet transmitted with no error |
| 0 | PRX | Packet Received Indicates packet received with no error. |

**4.3.3 Interrupt mask register (IMR) Offset 0FH (Write)**

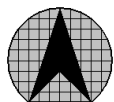
| FIELD | NAME | DESCRIPTION |
|-------|------|--|
| 7 | - | Reserved |
| 6 | RDCE | DMA Complete Interrupt Enable. Default "low" disabled. |
| 5 | CNTE | Counter Overflow Interrupt Enable. Default "low" disabled. |
| 4 | OVWE | Overwrite Interrupt Enable. Default "low" disabled. |
| 3 | TXEE | Transmit Error Interrupt Enable. Default "low" disabled. |
| 2 | RXEE | Receive Error Interrupt Enable. Default "low" disabled. |
| 1 | PTXE | Packet Transmitted Interrupt Enable. Default "low" disabled. |
| 0 | PRXE | Packet Received Interrupt Enable. Default "low" disabled. |

4.3.4 Data Configuration Register (DCR) Offset 0EH (Write)

| FIELD | NAME | DESCRIPTION |
|-------|------|--|
| 7 | RDCR | Remote DMA always completed |
| 6:2 | - | Reserved |
| 1 | BOS | Byte Order Select 0: MS byte placed on AD15:AD8 and LS byte on AD7-AD0 (80X86). 1: MS byte placed on AD7::AD0 and LS byte on AD15:AD0(68K) |
| 0 | WTS | Word Transfer Select 0 : Selects byte-wide DMA transfers. 1 : Selects word-wide DMA transfers. |

4.3.5 Transmit Configuration Register (TCR) Offset 0DH (Write)

| FIELD | NAME | DESCRIPTION | | | | | | | | | | | | |
|--------|----------|--|-----|-----|--|--------|-----|------------------|--------|-----|------------------------|--------|-----|----------------------|
| 7 | FDU | Full Duplex : This bit indicates the current media mode is Full Duplex or not. 0 : Half duplex 1 : Full duplex | | | | | | | | | | | | |
| 6 | PD | Pad Disable 0 : Pad will be added when packet length less than 60. 1 : Pad will not be added when packet length less than 60. | | | | | | | | | | | | |
| 5 | RLO | Retry of late collision 0 : Don't retransmit packet when late collision happens. 1 : Retransmit packet when late collision happens. | | | | | | | | | | | | |
| 4:3 | - | Reserved | | | | | | | | | | | | |
| 2:1 | LB1, LB0 | Encoded Loop-back Control These encoded configuration bits set the type of loop-back that is to be performed. <table style="margin-left: 40px;"> <tr> <td>LB1</td> <td>LB0</td> <td></td> </tr> <tr> <td>Mode 0</td> <td>0 0</td> <td>Normal operation</td> </tr> <tr> <td>Mode 1</td> <td>0 1</td> <td>Internal NIC loop-back</td> </tr> <tr> <td>Mode 2</td> <td>1 0</td> <td>PHYcevisor loop-back</td> </tr> </table> | LB1 | LB0 | | Mode 0 | 0 0 | Normal operation | Mode 1 | 0 1 | Internal NIC loop-back | Mode 2 | 1 0 | PHYcevisor loop-back |
| LB1 | LB0 | | | | | | | | | | | | | |
| Mode 0 | 0 0 | Normal operation | | | | | | | | | | | | |
| Mode 1 | 0 1 | Internal NIC loop-back | | | | | | | | | | | | |
| Mode 2 | 1 0 | PHYcevisor loop-back | | | | | | | | | | | | |
| 0 | CRC | Inhibit CRC 0 : CRC appended by transmitter. 1 : CRC inhibited by transmitter. | | | | | | | | | | | | |

**4.3.6 Transmit Status Register (TSR) Offset 04H (Read)**

| FIELD | NAME | DESCRIPTION |
|-------|------|--|
| 7 | OWC | Out of window collision |
| 6:4 | - | Reserved |
| 3 | ABT | Transmit Aborted Indicates the AX88190A aborted transmission because of excessive collision. |
| 2 | COL | Transmit Collided Indicates that the transmission collided at least once with another station on the network. |
| 1 | - | Reserved |
| 0 | PTX | Packet Transmitted Indicates transmission without error. |

4.3.7 Receive Configuration (RCR) Offset 0CH (Write)

| FIELD | NAME | DESCRIPTION |
|-------|--------|---|
| 7 | INT_RG | Interrupt Regeneration 0 : Enable interrupt regeneration function in multifunction application. (default) But must set CIS relative Enable function first, than the function will be open. 1: Disable |
| 6 | - | Reserved |
| 5 | MON | Monitor Mode 0 : Normal Operation 1 : Monitor Mode, the input packet will be checked on NODE ADDRESS and CRC but not buffered into memory. |
| 4 | PRO | PRO : Promiscuous Mode Enable the receiver to accept all packets with a physical address. |
| 3 | AM | AM : Accept Multicast Enable the receiver to accept packets with a multicast address. That multicast address must pass the hashing array. |
| 2 | AB | AB : Accept Broadcast Enable the receiver to accept broadcast packet. |
| 1 | AR | AR : Accept Runt Enable the receiver to accept runt packet. |
| 0 | SEP | SEP : Save Error Packet Enable the receiver to accept and save packets with error. |

4.3.8 Receive Status Register (RSR) Offset 0CH (Read)

| FIELD | NAME | DESCRIPTION |
|-------|------|-----------------------------|
| 7 | - | Reserved |
| 6 | DIS | Receiver Disabled |
| 5 | PHY | Multicast Address Received. |
| 4 | MPA | Missed Packet |
| 3 | FO | FIFO Overrun |
| 2 | FAE | Frame alignment error. |
| 1 | CR | CRC error. |
| 0 | PRX | Packet Received Intact |

4.3.9 Inter-frame gap (IFG) Offset 16H (Read/Write)

| FIELD | NAME | DESCRIPTION |
|-------|------|-------------------------------------|
| 7 | - | Reserved |
| 6:0 | IFG | Inter-frame Gap. Default value 15H. |

**4.3.10 Inter-frame gap Segment 1(IFGS1) Offset 12H (Read/Write)**

| FIELD | NAME | DESCRIPTION |
|-------|------|---|
| 7 | - | Reserved |
| 6:0 | IFG | Inter-frame Gap Segment 1. Default value 1cH. |

4.3.11 Inter-frame gap Segment 2(IFGS2) Offset 13H (Read/Write)

| FIELD | NAME | DESCRIPTION |
|-------|------|---|
| 7 | - | Reserved |
| 6:0 | IFG | Inter-frame Gap Segment 2. Default value 11H. |

4.3.12 MII/EEPROM Management Register (MEMR) Offset 14H (Read/Write)

| FIELD | NAME | DESCRIPTION |
|-------|-------|--|
| 7 | EECLK | EECLK EEPROM Clock |
| 6 | EEO | EEO EEPROM Data Out |
| 5 | EEI | EEI EEPROM Data In |
| 4 | EECS | EECS EEPROM Chip Select |
| 3 | MDO | MDO MII Data Out |
| 2 | MDI | MDI MII Data In |
| 1 | MDIR | MII STA MDIO signal Direction MII Read Control Bit, assert this bit let MDIO signal as the input signal. Deassert this bit let MDIO as output signal. |
| 0 | MDC | MDC MII Clock |

4.3.13 Test Register (TR) Offset 15H (Write)

| FIELD | NAME | DESCRIPTION |
|-------|-------|--|
| 7 | - | Reserved |
| 6 | MPSEL | Media Priority Select : default value is logic 0 MPSEL /SLINK Media Selected 0 0 SNI 0 1 MII 1 x Depand on MPSET bit |
| 5 | MPSET | Media Set by Program : The signal is valid only when MPSEL is set to high. When MPSET is logic 0 , SNI is selected. When MPSET is logic 1 , MII is selected. |
| 4 | TF16T | Test for Collision, default value is logic 0 |
| 3 | TPE | Test pin Enable, default value is logic 0 |
| 2:0 | IFG | Select Test Pins Output, default value is logic 0 |

4.3.14 General Purpose Input Register (GPI) Offset 18H (Read)

| FIELD | NAME | DESCRIPTION |
|-------|------|---|
| 7:4 | - | Reserved |
| 3 | GPI3 | This register reflects GPI[3] input value |
| 2 | GPI2 | This register reflects GPI[2] input value |
| 1 | GPI1 | This register reflects GPI[1] input value |
| 0 | GPI0 | This register reflects GPI[0] input value |

**4.3.15 General Purpose I/O Register (GPIO) Offset 1AH (Read/Write)**

| FIELD | NAME | DESCRIPTION |
|--------------|-------------|---|
| 7:6 | - | Reserved |
| 5 | CTL | Default "1". And must keep it to logic 1 always. |
| 4 | - | Reserved |
| 3 | GPIO3 | Default "0". The register reflects to GPIO3# pin with inverted value. |
| 2 | GPIO2 | Default "0". The register reflects to GPIO2 pin directly. |
| 1 | GPIO1 | Default "0". The register reflects to GPIO1# pin with inverted value. |
| 0 | GPIO0 | Default "0". The register reflects to GPIO0# pin with inverted value. |



5.0 PCMCIA Device Access Functions

5.1 Attribute Memory access function functions.

Attribute Memory Read function

| Function Mode | REG# | CE2# | CE1# | SA0 | OE# | WE# | SD[15:8] | SD[7:0] |
|-----------------------|------|------|------|-----|-----|-----|-----------|-----------|
| Standby Mode | X | H | H | X | X | X | High-Z | High-Z |
| Byte Access (8 bits) | L | H | L | L | L | H | High-Z | Even-Byte |
| | L | H | L | H | L | H | High-Z | Not Valid |
| Word Access (16 bits) | L | L | L | X | L | H | Not Valid | Even-Byte |
| Odd Byte Only Access | L | L | H | X | L | H | Not Valid | High-Z |

Attribute Memory Write function

| Function Mode | REG# | CE2# | CE1# | SA0 | OE# | WE# | SD[15:8] | SD[7:0] |
|-----------------------|------|------|------|-----|-----|-----|----------|-----------|
| Standby Mode | X | H | H | X | X | X | X | X |
| Byte Access (8 bits) | L | H | L | L | H | L | X | Even-Byte |
| | L | H | L | H | H | L | X | X |
| Word Access (16 bits) | L | L | L | X | H | L | X | Even-Byte |
| Odd Byte Only Access | L | L | H | X | H | L | X | X |

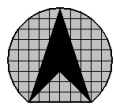
5.2 I/O access function functions.

I/O Read function

| Function Mode | REG# | CE2# | CE1# | SA0 | OE# | WE# | SD[15:8] | SD[7:0] |
|-----------------------|------|------|------|-----|-----|-----|----------|-----------|
| Standby Mode | X | H | H | X | X | X | High-Z | High-Z |
| Byte Access (8 bits) | L | H | L | L | L | H | High-Z | Even-Byte |
| | L | H | L | H | L | H | High-Z | Odd-Byte |
| Word Access (16 bits) | L | L | L | L | L | H | Odd-Byte | Even-Byte |
| I/O Inhibit | H | X | X | X | L | H | High-Z | High-Z |
| Odd Byte Only Access | L | L | H | X | L | H | Odd-Byte | High-Z |

I/O Write function

| Function Mode | REG# | CE2# | CE1# | SA0 | IORD# | IOWR# | SD[15:8] | SD[7:0] |
|-----------------------|------|------|------|-----|-------|-------|----------|-----------|
| Standby Mode | X | H | H | X | X | X | X | X |
| Byte Access (8 bits) | L | H | L | L | H | L | X | Even-Byte |
| | L | H | L | H | H | L | X | Odd-Byte |
| Word Access (16 bits) | L | L | L | L | H | L | Odd-Byte | Even-Byte |
| I/O Inhibit | H | X | X | X | H | L | X | X |
| Odd Byte Only Access | L | L | H | X | H | L | Odd-Byte | X |



6.0 Electrical Specification and Timings

6.1 Absolute Maximum Ratings

| Description | SYM | Min | Max | Units |
|---|-------|------|----------|-------|
| Operating Temperature | Ta | 0 | +85 | °C |
| Storage Temperature | Ts | -55 | +150 | °C |
| Supply Voltage | HVdd | -0.3 | +6 | V |
| Supply Voltage | LVdd | -0.3 | +4.6 | V |
| Input Voltage | HVin | -0.3 | HVdd+0.5 | V |
| | LVin | -0.3 | LVdd+0.5 | V |
| Output Voltage | HVout | -0.3 | HVdd+0.5 | V |
| | LVin | -0.3 | LVdd+0.5 | V |
| Lead Temperature (soldering 10 seconds maximum) | Tl | -55 | +220 | °C |

Note : Stress above those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to Absolute Maximum Ratings conditions for extended period, adversely affect device life and reliability.

Note : The power supply voltages must always fulfill HVdd >= LVdd inequality.

6.2 General Operation Conditions

| Description | SYM | Min | Tpy | Max | Units |
|-----------------------|------|--------|--------|--------|-------|
| Operating Temperature | Ta | 0 | 25 | +75 | °C |
| Supply Voltage | HVdd | +4.75V | +5.00V | +5.25V | V |
| | LVdd | +2.70 | +3.00 | +3.30 | V |
| | | +3.00 | +3.30 | +3.60 | V |

Note : The power supply voltages must always fulfill HVdd >= LVdd inequality.

6.3 DC Characteristics

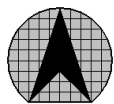
(Vdd=5.0V, Vss=0V, Ta=0°C to 75°C)

| Description | SYM | Min | Tpy | Max | Units |
|------------------------|-----|---------|-----|-----|-------|
| Low Input Voltage | Vil | - | | 0.8 | V |
| High Input Voltage | Vih | 2 | | - | V |
| Low Output Voltage | Vol | - | | 0.4 | V |
| High Output Voltage | Voh | Vdd-0.4 | | - | V |
| Input Leakage Current | Iil | -1 | | +1 | uA |
| Output Leakage Current | Iol | -1 | | +1 | uA |

(Vdd=3.0V to 3.6V, Vss=0V, Ta=0°C to 75°C)

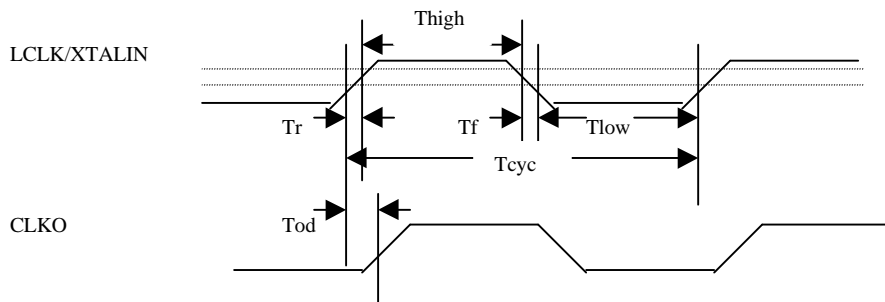
| Description | SYM | Min | Tpy | Max | Units |
|------------------------|-----|---------|-----|-----|-------|
| Low Input Voltage | Vil | - | | 0.8 | V |
| High Input Voltage | Vih | 1.9 | | - | V |
| Low Output Voltage | Vol | - | | 0.4 | V |
| High Output Voltage | Voh | Vdd-0.4 | | - | V |
| Input Leakage Current | Iil | -1 | | +1 | uA |
| Output Leakage Current | Iol | -1 | | +1 | uA |

| Description | SYM | Min | Tpy | Max | Units |
|---------------------------------------|-------|-----|-----|-----|-------|
| Power Consumption (Dual power) | DPT5v | | 17 | | mA |
| | DPT3v | | 31 | | mA |
| Power Consumption (Single power 3.3V) | SPt3v | | 48 | | mA |



6.4 A.C. Timing Characteristics

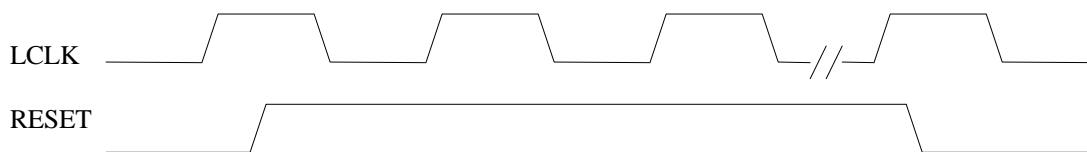
6.4.1 XTAL / CLOCK



| Symbol | Description | Min | Typ. | Max | Units |
|--------|-------------------------------|-----|------|-----|-------|
| Tcyc | CYCLE TIME | | 40* | | ns |
| Thigh | CLK HIGH TIME | 16 | 20 | 24 | ns |
| Tlow | CLK LOW TIME | 16 | 20 | 24 | ns |
| Tr/Tf | CLK SLEW RATE | 1 | - | 4 | ns |
| Tod | LCLK/XTALIN TO CLKO OUT DELAY | | 10 | | |

* Note : The Tcyc can be from 16.6ns to 50ns, that is frequency from 60MHz to 20MHz.

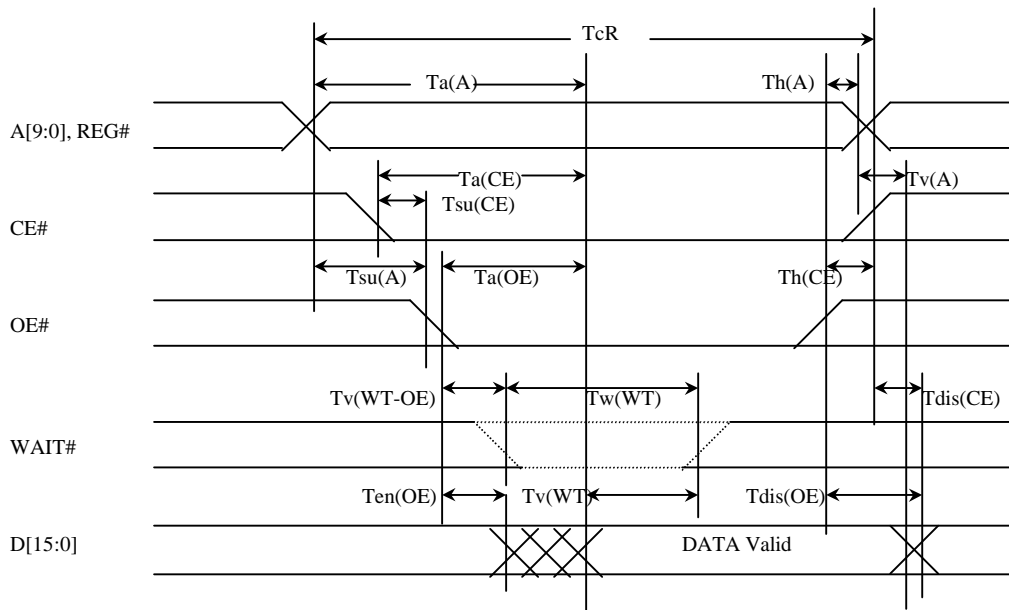
6.4.2 Reset Timing



| Symbol | Description | Min | Typ. | Max | Units |
|--------|-------------------|-----|------|-----|-------|
| Trst | Reset pulse width | 100 | - | - | LClk |



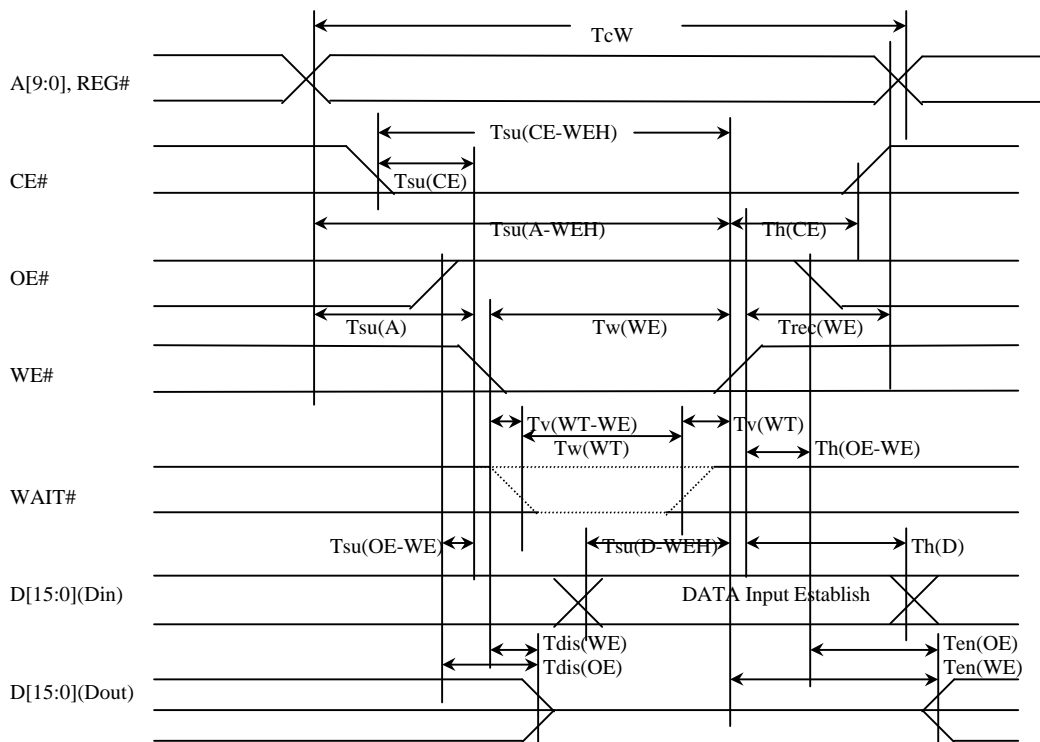
6.4.3 Attribute Memory Read Timing



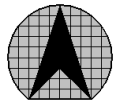
| Symbol | Description | Min | Typ. | Max | Units |
|-----------|--------------------------------|-----|------|-----|-------|
| TcR | READ CYCLE TIME | 300 | - | - | ns |
| Ta(A) | ADDRESS ACCESS TIME | - | - | 120 | ns |
| Ta(CE) | CARD ENABLE ACCESS TIME | - | - | 100 | ns |
| Ta(OE) | OUTPUT ENABLE ACCESS TIME | - | - | 100 | ns |
| Tdis(OE) | OUTPUT DISABLE TIME FROM OE# | 0.5 | - | - | ns |
| Ten(OE) | OUTPUT ENABLE TIME FROM OE# | - | - | 100 | ns |
| Tv(A) | DATA VALID FROM ADDRESS CHANGE | 0 | - | - | ns |
| Tsu(A) | ADDRESS SETUP TIME | 30 | - | - | ns |
| Th(A) | ADDRESS HOLD TIME | 20 | - | - | ns |
| Tsu(CE) | CARD ENABLE SETUP TIME | 0 | - | - | ns |
| Th(CE) | CARD ENABLE HOLD TIME | 20 | - | - | ns |
| Tv(WT-OE) | WAIT# VALID FROM OE# | - | - | 10 | ns |
| Tw(WT) | WAIT# PULSE WIDTH | - | - | 200 | ns |
| Tv(WT) | DATA SETUP FOR WAIT# RELEASED | 100 | - | - | ns |



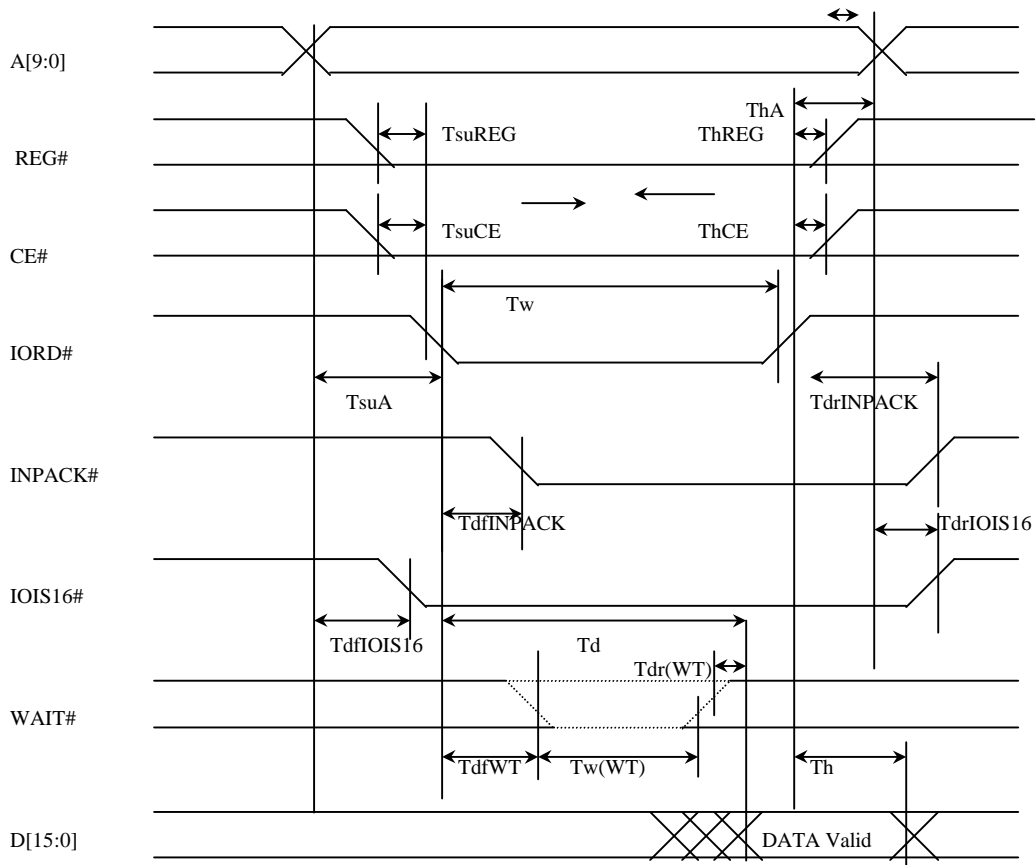
6.4.4 Attribute Memory Write Timing



| Symbol | Description | Min | Typ. | Max | Units |
|-------------|-----------------------------------|-----|------|-----|-------|
| TcW | WRITE CYCLE TIME | 250 | - | - | ns |
| Tw(WE) | WRITE PULSE WIDTH | 150 | - | - | ns |
| Tsu(A) | ADDRESS SETUP TIME | 30 | - | - | ns |
| Tsu(A-WEH) | ADDRESS SETUP TIME FOR WE# | 180 | - | - | ns |
| Tsu(CE-WEH) | CARD ENABLE SETUP TIME FOR WE# | 180 | - | - | ns |
| Tsu(D-WEH) | DATA SETUP TIME FOR WE# | 80 | - | - | ns |
| Th(D) | DATA HOLD TIME | 30 | - | - | ns |
| Trec(WE) | WRITE RECOVER TIME | 30 | - | - | ns |
| Tdis(WE) | OUTPUT DISABLE TIME FROM WE# | - | - | 5 | ns |
| Tdis(OE) | OUTPUT DISABLE TIME FROM OE# | - | - | 5 | ns |
| Ten(WE) | OUTPUT ENABLE TIME FROM WE# | 5 | - | - | ns |
| Ten(OE) | OUTPUT ENABLE TIME FROM OE# | 5 | - | - | ns |
| Tsu(OE-WE) | OUTPUT ENABLE SETUP TIME FROM OE# | 10 | - | - | ns |
| Th(OE-WE) | OUTPUT ENABLE HOLD TIME FROM OE# | 10 | - | - | ns |
| Tsu(CE) | CARD ENABLE SETUP TIME | 0 | - | - | ns |
| Th(CE) | CARD ENABLE HOLD TIME | 20 | - | - | ns |
| Tv(WT-WE) | WAIT# VALID FROM WE# | - | - | 15 | ns |
| Tw(WT) | WAIT# PULSE WIDTH | - | - | 200 | ns |
| Tv(WT) | WE# HIGH FROM WAIT# RELEASED | 0 | - | - | ns |

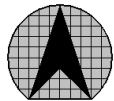


6.4.5 I/O Read Timing

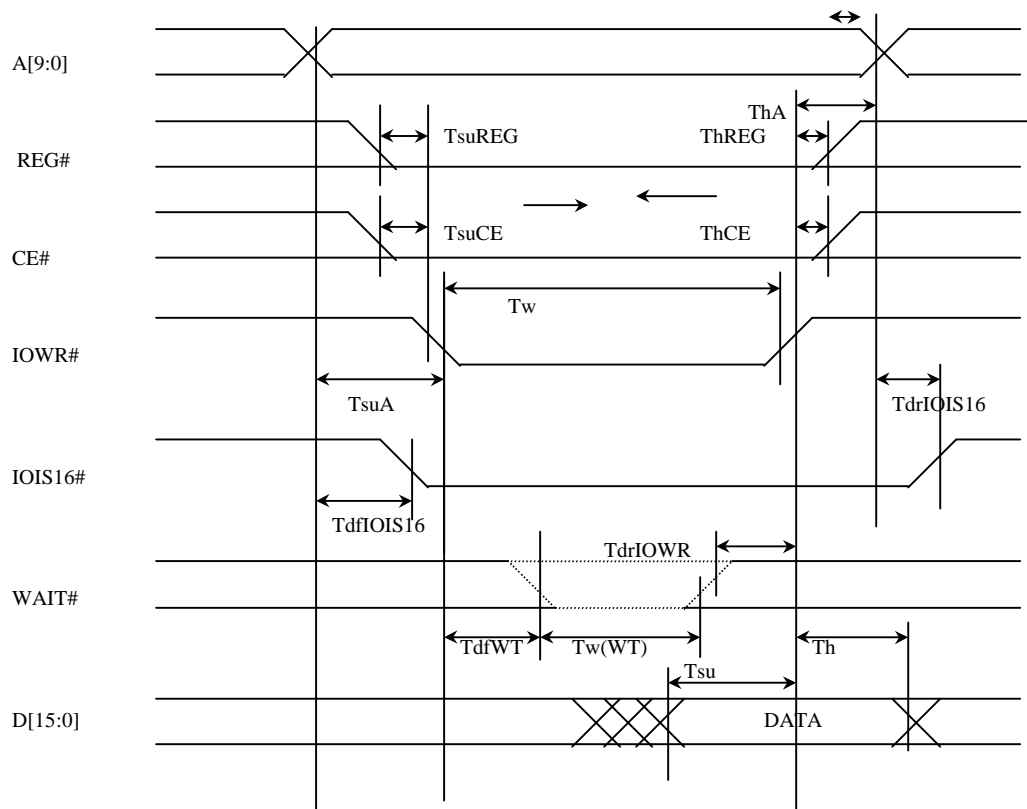


| Symbol | Description | Min | Typ. | Max | Units |
|-----------|-------------------------------------|-----|------|-----|-------|
| Td | DATA DELAY AFTER IORD# | - | - | 50 | ns |
| Th | DATA HOLD FOLLOWING IORD# | 0.5 | - | - | ns |
| Tw | IORD# WIDTH TIME | 165 | - | - | ns |
| TsuA | ADDRESS SETUP BEFORE IORD# | 70 | - | - | ns |
| ThA | ADDRESS HOLD BEFORE IORD# | 20 | - | - | ns |
| TsuCE | CE# SETUP BEFORE IORD# | 5 | - | - | ns |
| ThCE | CE# HOLD BEFORE IORD# | 20 | - | - | ns |
| TsuREG | REG# SETUP BEFORE IORD# | 5 | - | - | ns |
| ThREG | REG# HOLD BEFORE IORD# | 0 | - | - | ns |
| TdfINPACK | INPACK# DELAY FALLING FROM IORD# | 0 | - | 10 | ns |
| TdrINPACK | INPACK# DELAY RISING FROM IORD# | - | - | 10 | ns |
| TdfIOIS16 | IOIS16# DELAY FALLING FROM ADDRESS* | - | - | 10 | ns |
| TdrIOIS16 | IOIS16# DELAY RISING FROM ADDRESS* | - | - | 0 | ns |
| TdfWT | WAIT# DELAY FALLING FROM IORD# | - | - | 5 | ns |
| Tdr(WT) | DATA DELAY FROM WAIT# RISING | - | - | 0 | us |
| Tw(WT) | WAIT# WIDTH TIME | - | - | 100 | ns |

* Note : The address includes REG# and CE1# signal



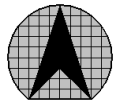
6.4.6 I/O Write Timing



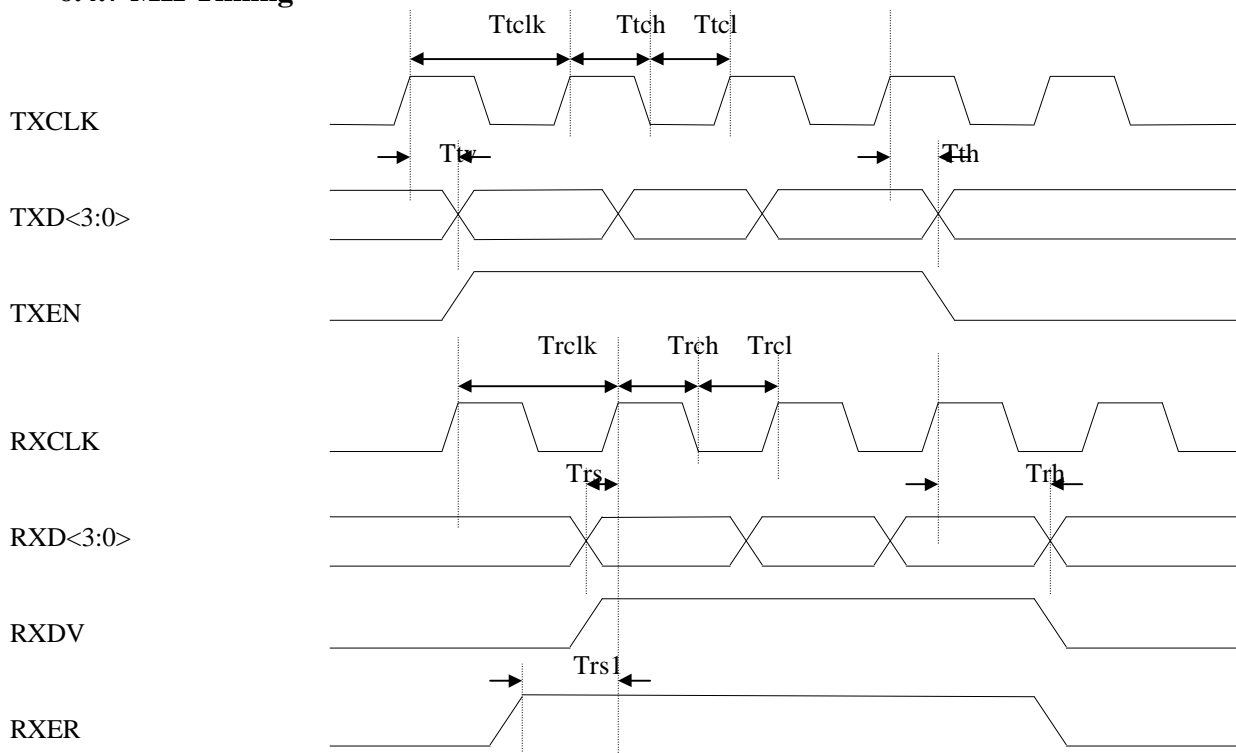
| Symbol | Description | Min | Typ. | Max | Units |
|----------------|-------------------------------------|-----|------|-----|-------|
| T_{su} | DATA SETUP BEFORE IOWR# | 60 | - | - | ns |
| T_h | DATA HOLD FOLLOWING IOWR# | 30 | - | - | ns |
| T_w | IOWR# WIDTH TIME | 165 | - | - | ns |
| T_{sA} | ADDRESS SETUP BEFORE IOWR# | 70 | - | - | ns |
| T_{hA} | ADDRESS HOLD BEFORE IOWR# | 20 | - | - | ns |
| T_{sCE} | CE# SETUP BEFORE IOWR# | 5 | - | - | ns |
| T_{hCE} | CE# HOLD BEFORE IOWR# | 20 | - | - | ns |
| T_{sREG} | REG# SETUP BEFORE IOWR# | 5 | - | - | ns |
| T_{hREG} | REG# HOLD BEFORE IOWR# | 0 | - | - | ns |
| $T_{dfIOIS16}$ | IOIS16# DELAY FALLING FROM ADDRESS* | - | - | 10 | ns |
| $T_{drIOIS16}$ | IOIS16# DELAY RISING FROM ADDRESS* | - | - | 0 | ns |
| T_{dfWT} | WAIT# DELAY FALLING FROM IOWR# | - | - | ** | ns |
| $T_w(WT)$ | WAIT# WIDTH TIME | - | - | ** | ns |
| T_{drIOWR} | IOWR# HIGH FROM WAIT# HIGH | 0 | - | - | us |

*Note : The address includes REG# and CE1# signal

** Note : There is no wait state while I/O Write operation



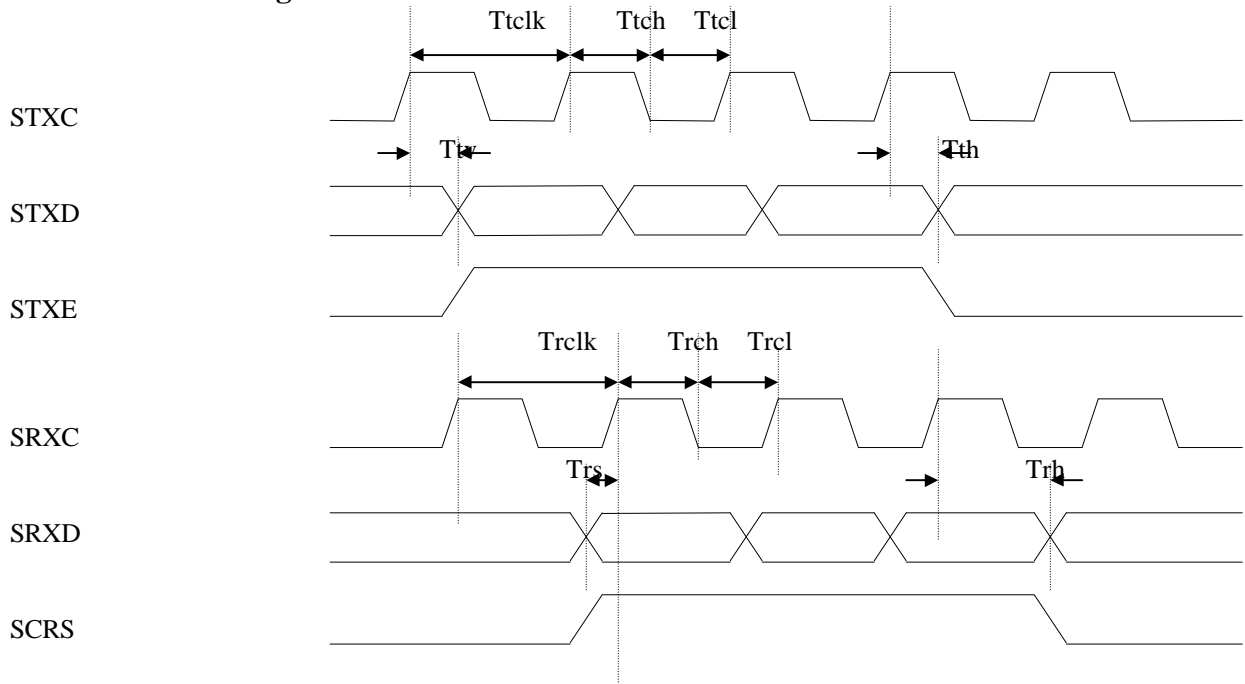
6.4.7 MII Timing



| Symbol | Description | Min | Typ. | Max | Units |
|--------|-----------------------|-----|------|-----|-------|
| Ttclk | Cycle time(100Mbps) | - | 40 | - | ns |
| Ttclk | Cycle time(10Mbps) | - | 400 | - | ns |
| Ttch | high time(100Mbps) | 14 | - | 26 | ns |
| Ttch | high time(10Mbps) | 140 | - | 260 | ns |
| Trch | low time(100Mbps) | 14 | - | 26 | ns |
| Trch | low time(10Mbps) | 140 | - | 260 | ns |
| Ttv | Clock to data valid | - | - | 20 | ns |
| Tth | Data output hold time | 5 | - | - | ns |
| Trclk | Cycle time(100Mbps) | - | 40 | - | ns |
| Trclk | Cycle time(10Mbps) | - | 400 | - | ns |
| Trch | high time(100Mbps) | 14 | - | 26 | ns |
| Trch | high time(10Mbps) | 140 | - | 260 | ns |
| Trcl | low time(100Mbps) | 14 | - | 26 | ns |
| Trcl | low time(10Mbps) | 140 | - | 260 | ns |
| Trs | data setup time | 6 | - | - | ns |
| Trh | data hold time | 10 | - | - | ns |
| Trsl | RXER data setup time | 10 | - | - | ns |



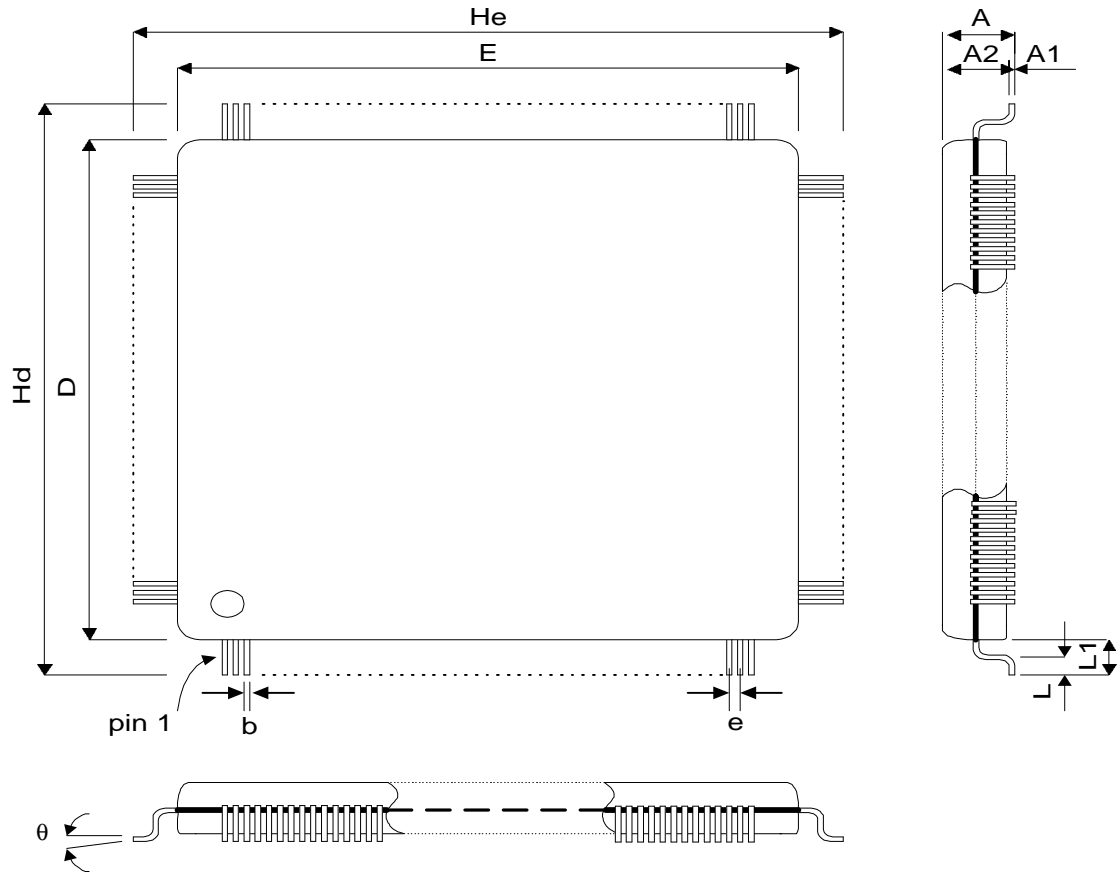
6.4.8 SNI Timing



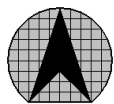
| Symbol | Description | Min | Typ. | Max | Units |
|--------|-----------------------|-----|------|-----|-------|
| Ttclk | Cycle time(10Mbps) | - | 100 | - | ns |
| Ttch | high time(10Mbps) | 45 | - | 55 | ns |
| Trch | low time(10Mbps) | 45 | - | 55 | ns |
| Ttv | Clock to data valid | - | - | 26 | ns |
| Tth | Data output hold time | 5 | - | - | ns |
| Trclk | Cycle time(10Mbps) | - | 100 | - | ns |
| Trch | high time(10Mbps) | 45 | - | 55 | ns |
| Trcl | low time(10Mbps) | 45 | - | 55 | ns |
| Trs | data setup time | 10 | - | - | ns |
| Trh | data hold time | 5 | - | - | ns |



7.0 Package Information

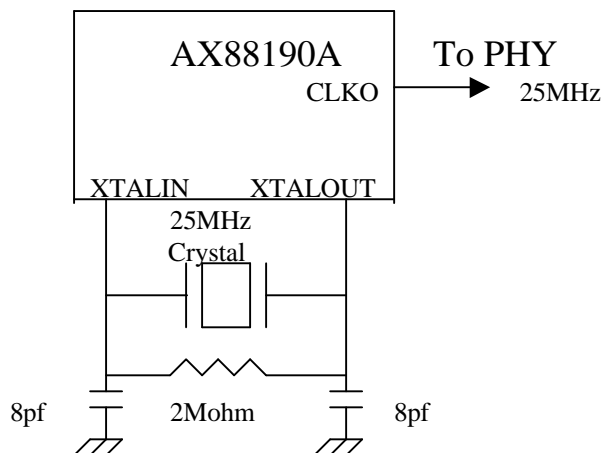


| SYMBOL | MILIMETER | | |
|--------|-----------|-------|-------|
| | MIN. | NOM | MAX |
| A1 | | 0.1 | |
| A2 | 1.3 | 1.4 | 1.5 |
| A | | | 1.7 |
| b | 0.155 | 0.16 | 0.26 |
| D | 13.90 | 14.00 | 14.10 |
| E | 13.90 | 14.00 | 14.10 |
| e | | 0.40 | |
| Hd | 15.60 | 16.00 | 16.40 |
| He | 15.60 | 16.00 | 16.40 |
| L | 0.30 | 0.50 | 0.70 |
| L1 | | 1.00 | |
| θ | 0 | | 10 |



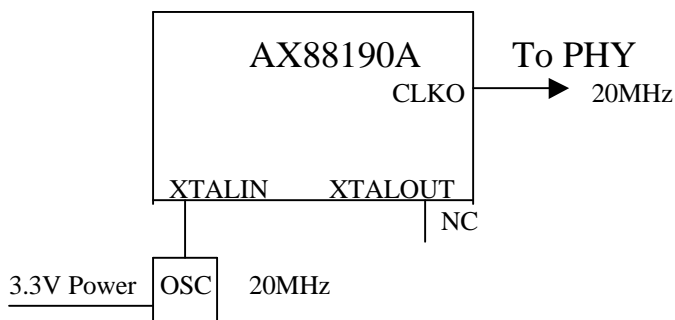
Appendix A: Application Note

A.1 Using Crystal 25MHz or 20MHz

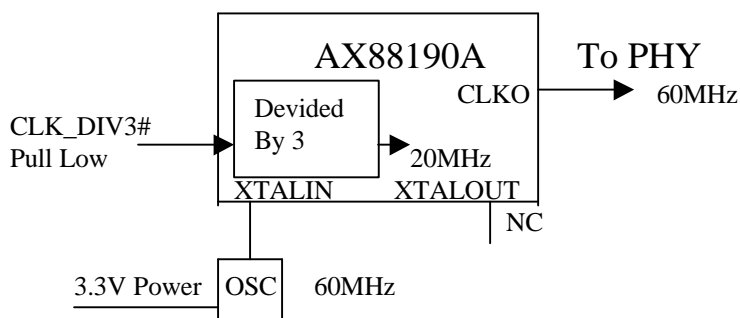


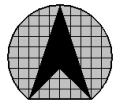
Note : The capacitors (8pf) may be various depend on the specification of crystal. While designing, please refer to the suggest circuit provided by crystal supplier.

A.2 Using Oscillator 25MHz or 20MHz

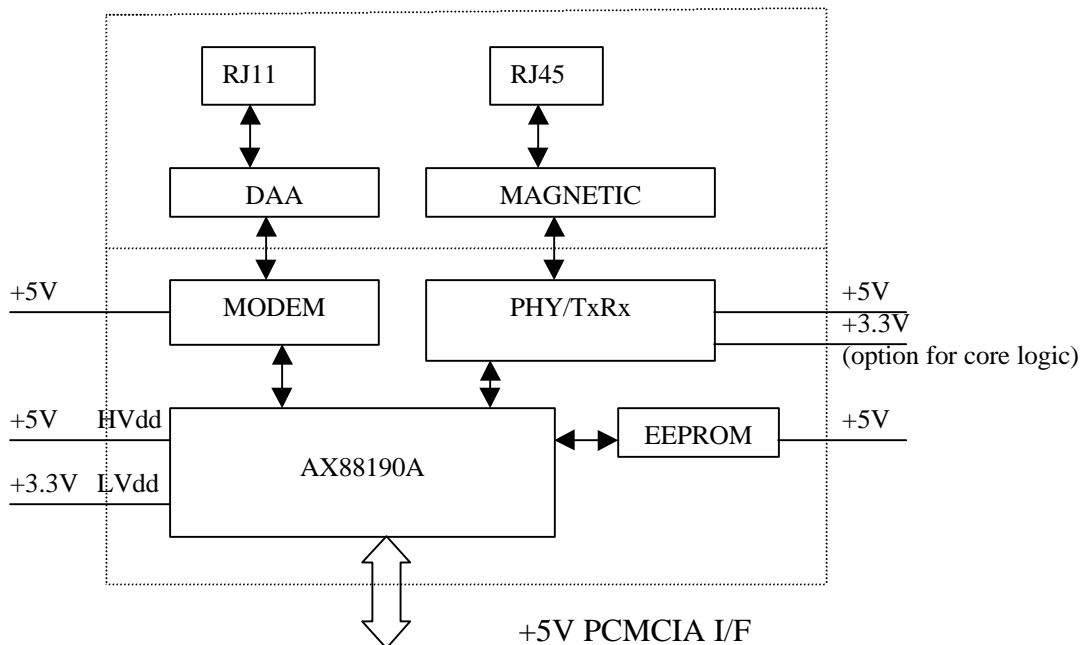


A.3 Using 60MHz Oscillator/Crystal

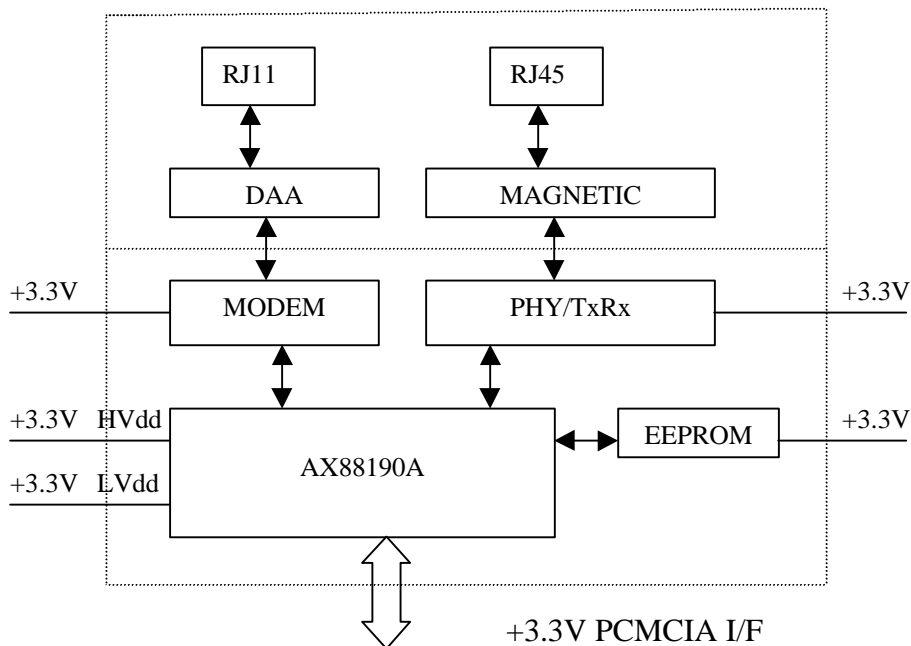




A.4 Dual power (5V and 3.3V) application



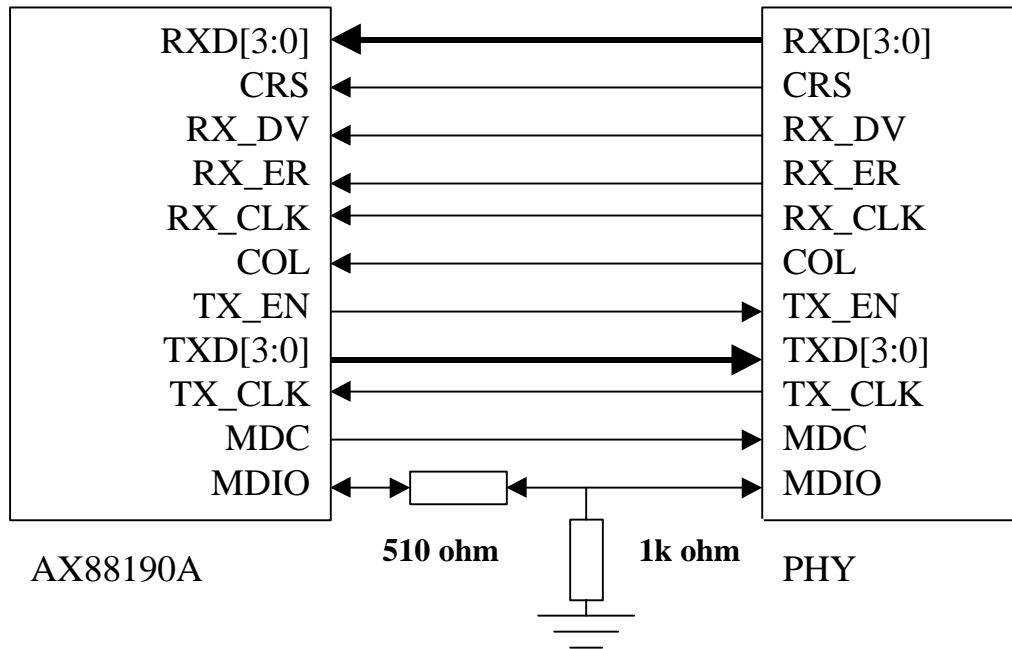
A.5 Single power (3.3V) application





A.6 Dual power (5V and 3.3V) application with 3.3V PHY

The 510 and 1K Ohm resistors are just for voltage adjustment

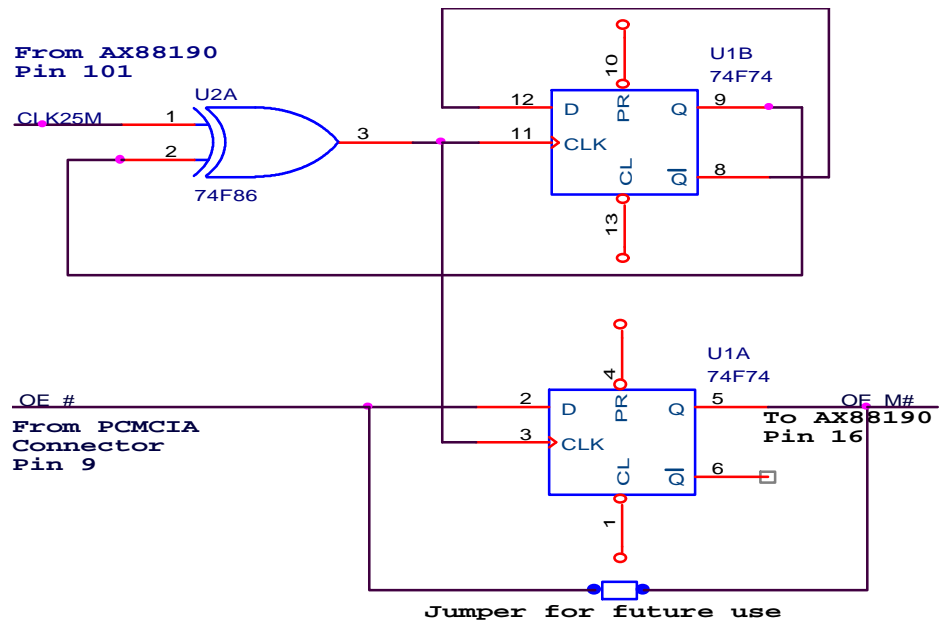




Appendix B: AX88190 design changes to AX88190A

Please refer to following circuit diagram that implement in AX88190 PWB and follow the following four steps.

1. Remove AX88190 and replace with AX88190A
2. Remove 2 pieces of buffer memory(32k*8 SRAM). Because they are not necessary anymore.
3. Remove 74F86 and 74F74 TTL IC
4. Shorten the jumper shown as below circuit diagram lable “Jumper for future use”

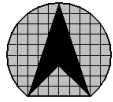




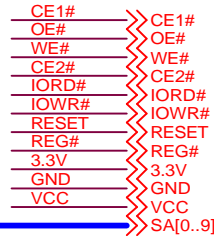
Errata of AX88190A Version ED2

1. SNI (Serial Network Interface) has bug for HomePNA application.

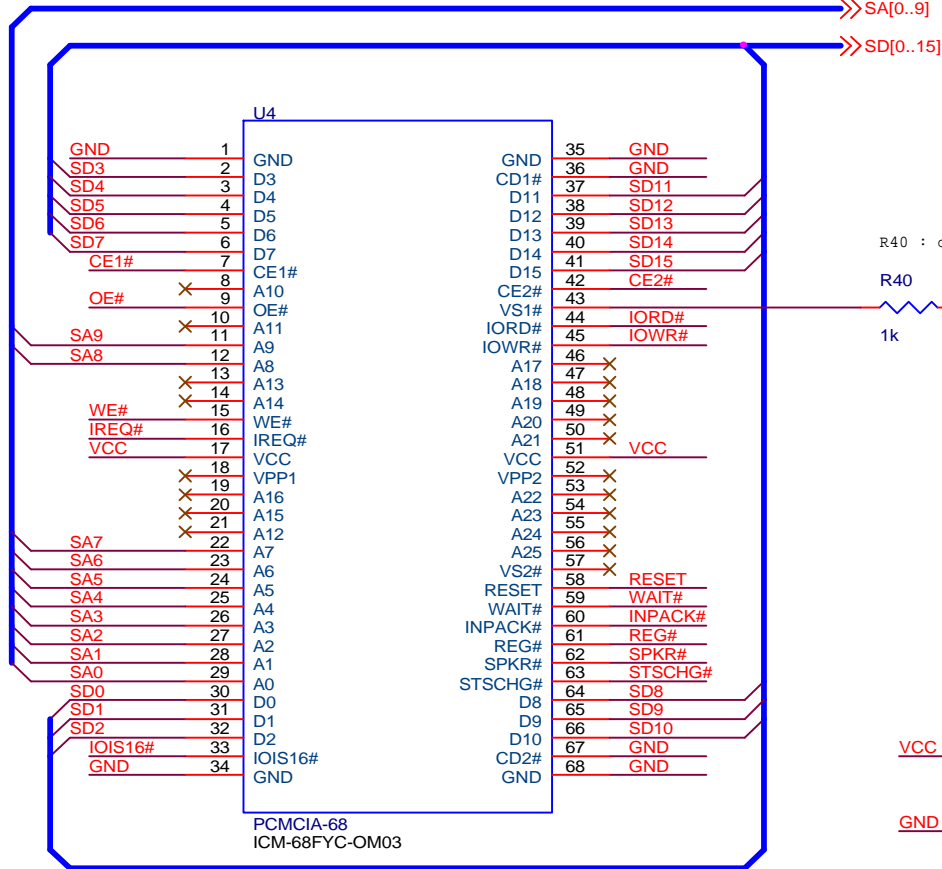
Solution: Using MII interface for HomePNA solution. Refer to “Demonstration Circuit” on page 39 to 44.



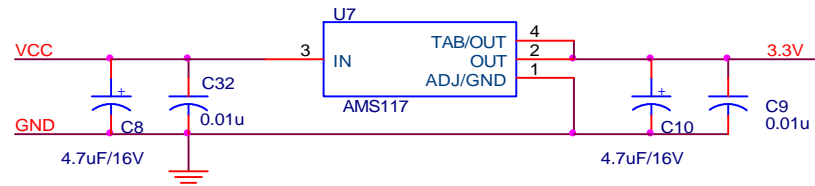
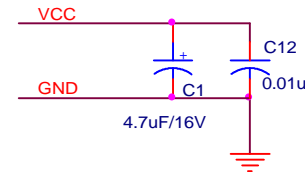
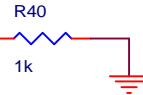
Demonstration Circuit : AX88190A + Ethernet PHY + HomePNA 1M8 PHY

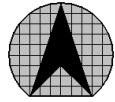


AX88190AL 10BASE-T/100BASE-TX & 1M HomePNA
 Application with DP83846A & DP83851 PHYceiver.
 (reference only)



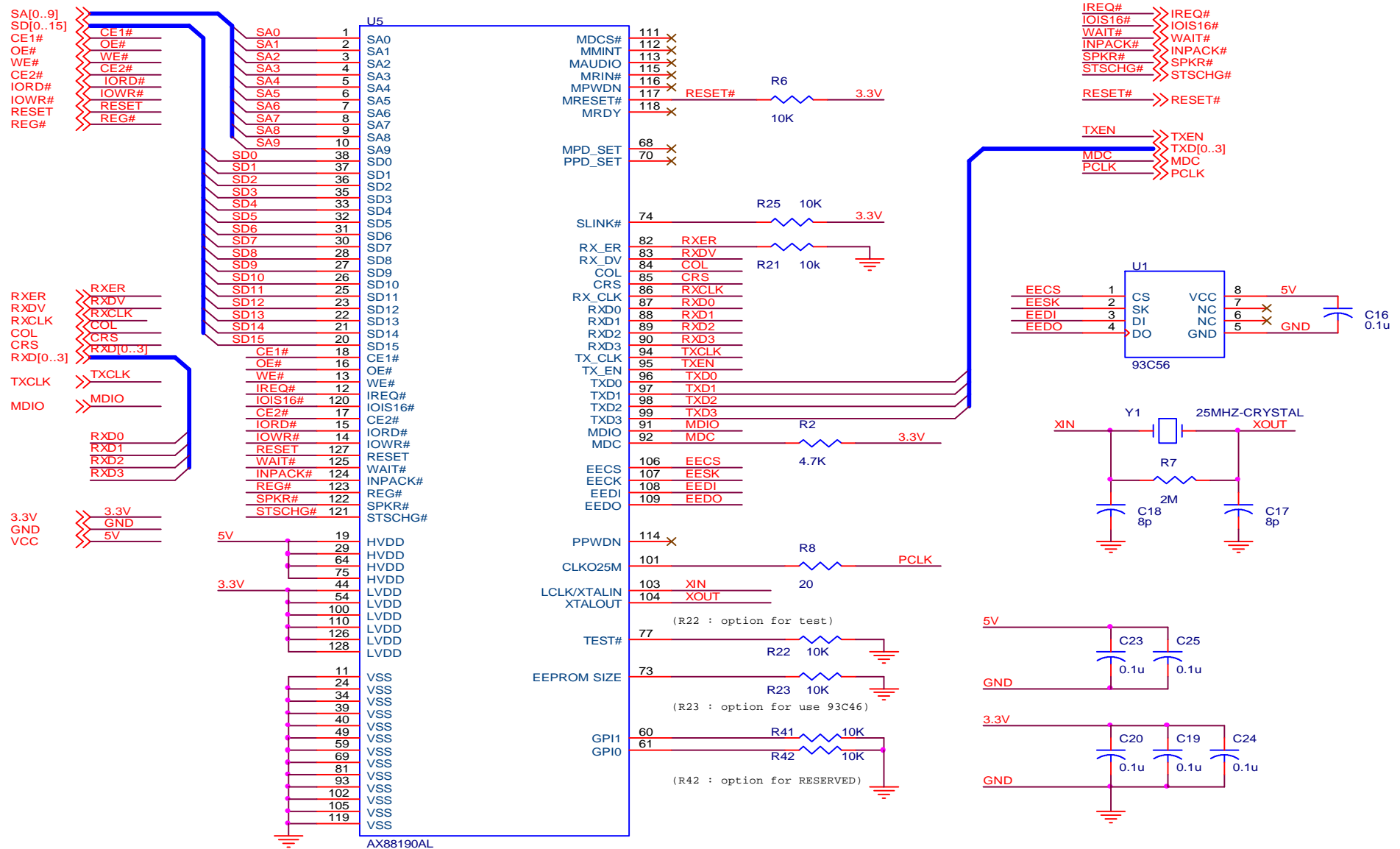
R40 : option for 3.3V card tpye.

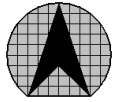




AX88190A

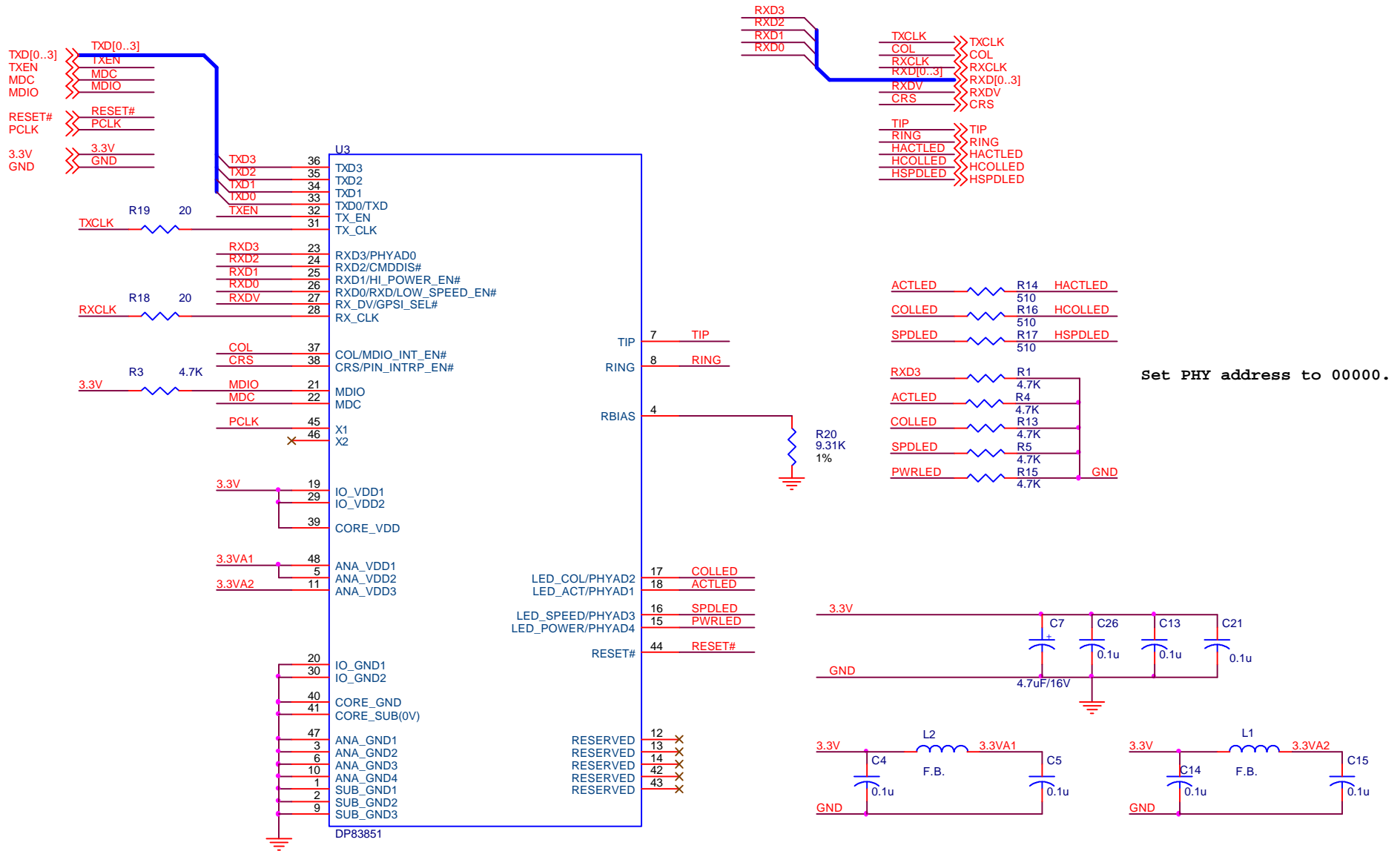
10/100Mbps PCMCIA Fast Ethernet MAC Controller

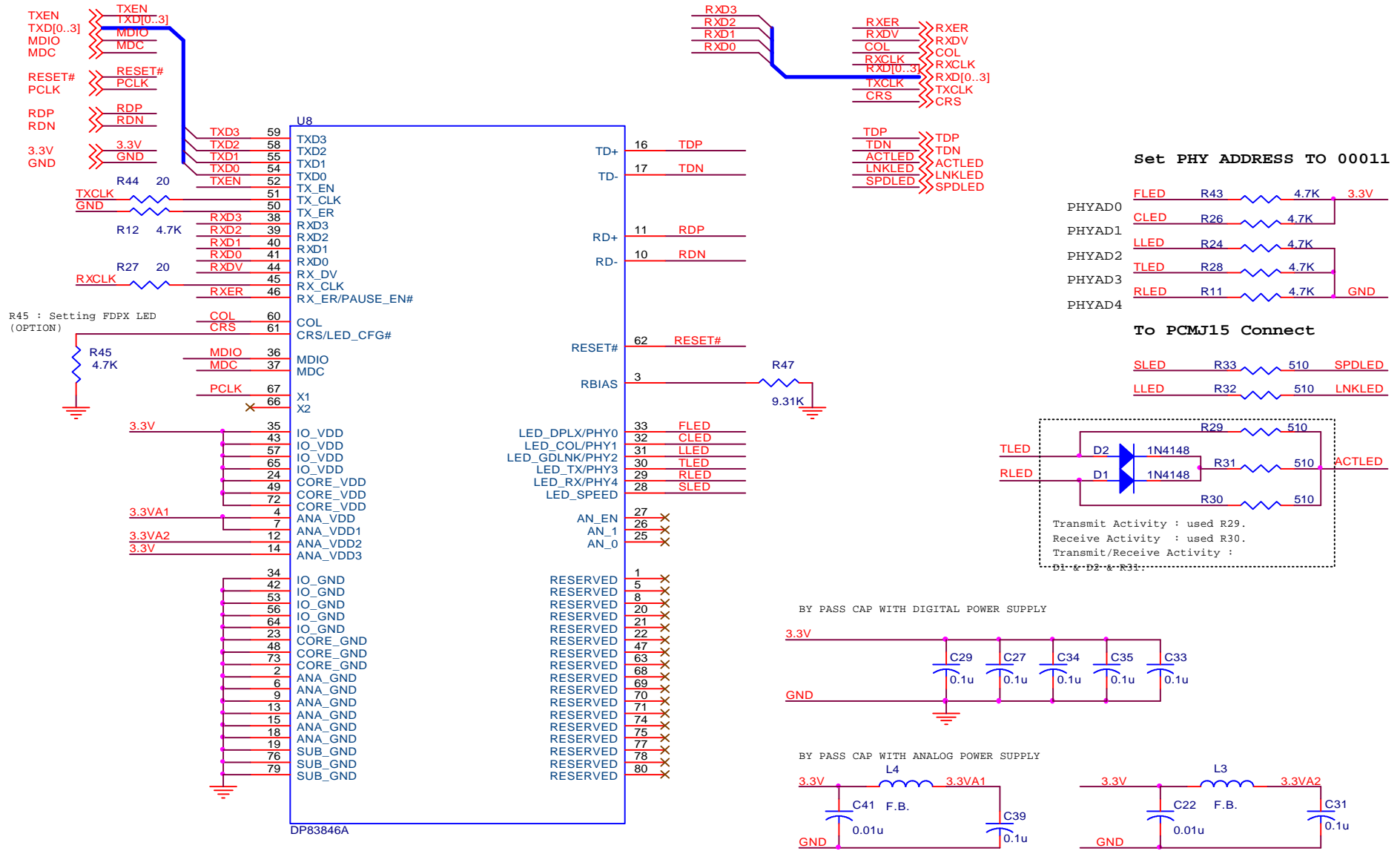
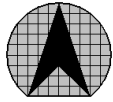




AX88190A

10/100Mbps PCMCIA Fast Ethernet MAC Controller

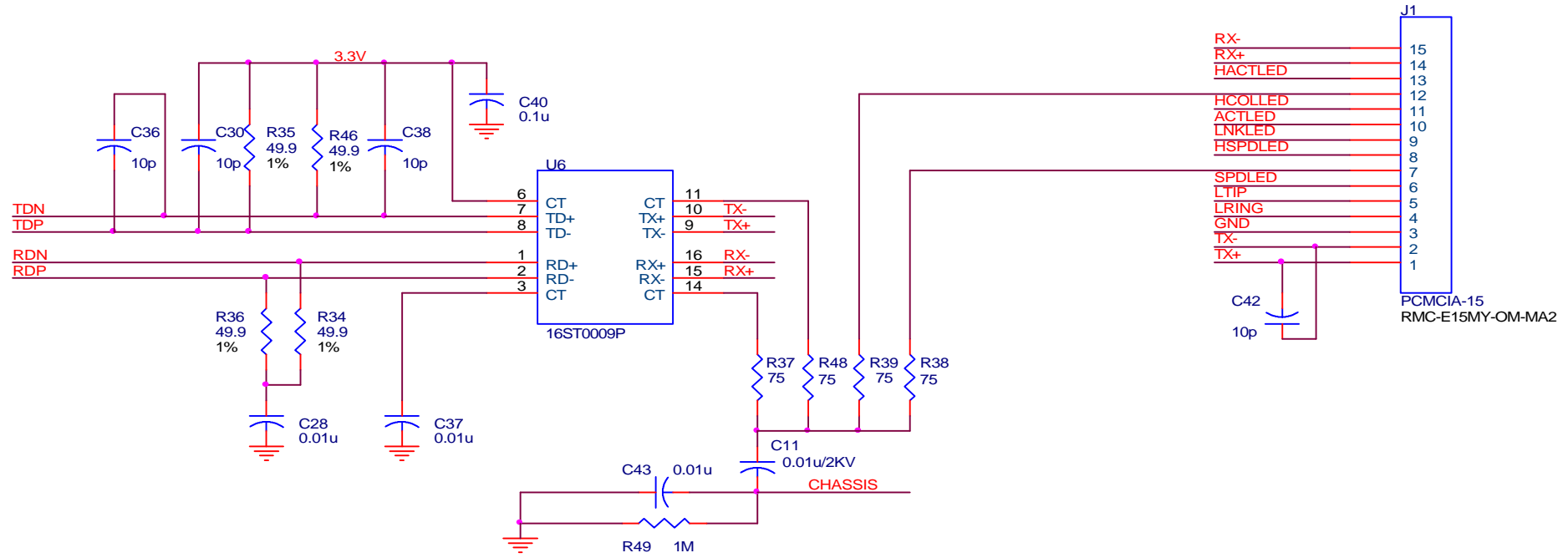
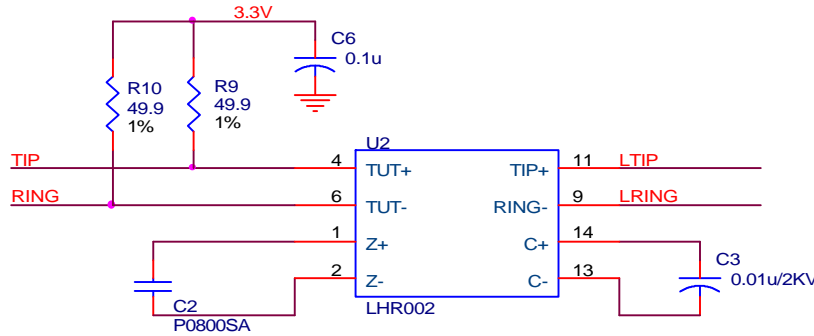
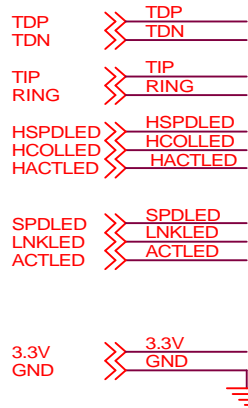


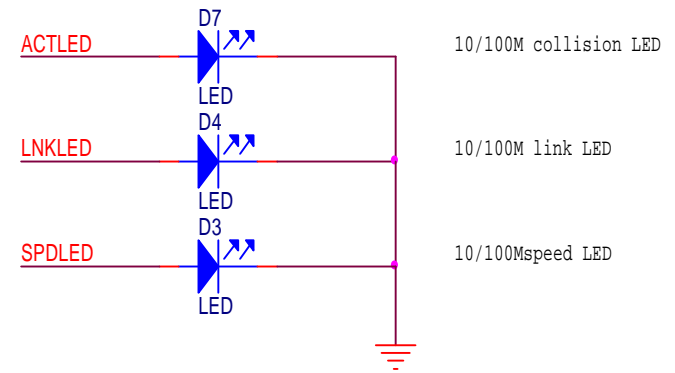
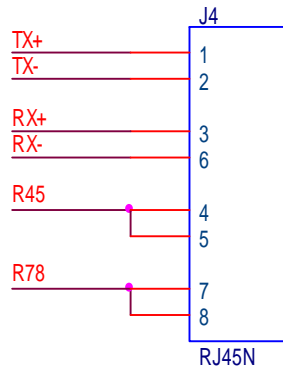
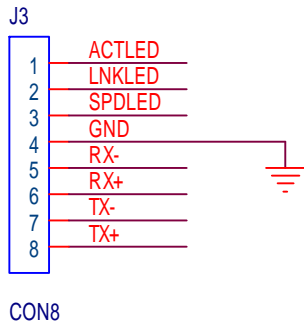
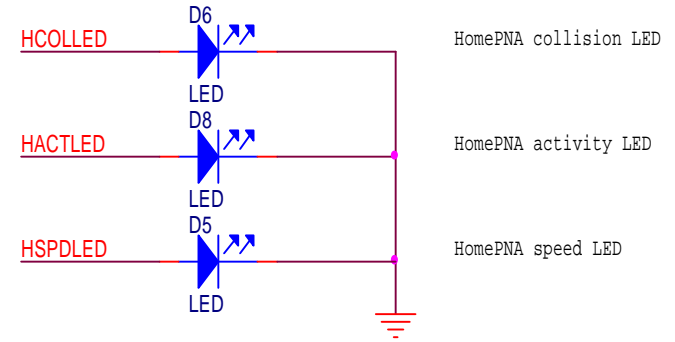
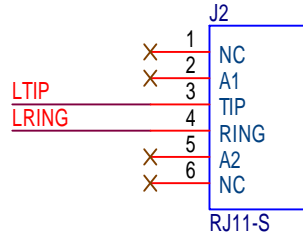
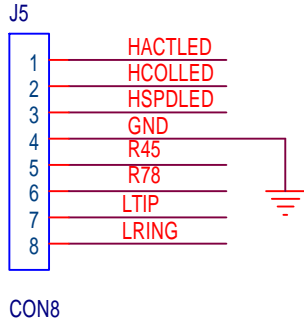
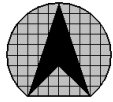


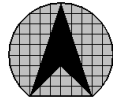


AX88190A

10/100Mbps PCMCIA Fast Ethernet MAC Controller

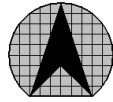




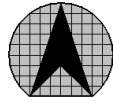


Reference Bill Of Materials

| Item | Quantity | Reference | Part | Reamrk |
|------|----------|--|---------------|--------|
| 1 | 2 | C18,C17 | 8p | 0603 |
| 2 | 4 | C30,C36,C38,C42 | 10p | 0603 |
| 3 | 8 | C9,C12,C22,C28,C32,C37,C41,C43 | 0.01uF | 0603 |
| 4 | 22 | C4,C5,C6,C13,C14,C15,C16,C19,C20,C21,C23,C24,C25,C26,C27,C29,C31,C33,C34,C35,C39,C40 | 0.1uF | 0603 |
| 5 | 4 | C1,C7,C8,C10 | 4.7uF/16V | 1206 |
| 6 | 2 | C11,C3 | 0.01u/2KV | 1206 |
| 7 | 1 | C2 | P0800SA | *1 |
| 8 | 2 | D2,D1 | 1N4148 | SMD |
| 9 | 6 | D3,D4,D5,D6,D7,D8 | LED | DIP |
| 10 | 4 | L1,L2,L3,L4 | F.B | 1206 |
| 11 | 5 | R8,R18,R19,R27,R44 | 20 | 0603 |
| 12 | 4 | R37,R38,R39,R48 | 75 | 0603 |
| 13 | 5 | R9,R10,R35,R46,R34,R36 | 49.9 1% | 0603 |
| 14 | 5 | R14,R16,R17,R32,R33 | 510 | 0603 |
| 14-1 | 1 | R31 | 330 | 0603 |
| 15 | 13 | R1,R2,R3,R4,R5,R11,R12,R13,R15,R24,R26,R28,R43 | 4.7K | 0603 |
| 16 | 2 | R47,R20 | 9.31K 1% | 0603 |
| 17 | 4 | R6,R21,R25,R42 | 10K | 0603 |
| 18 | 1 | R49 | 1M | 0603 |
| 19 | 1 | R7 | 2M | 0603 |
| 20 | 1 | U5 | AX88190AL | TQFP |
| 21 | 1 | U1 | 93C56 | SMD |
| 22 | 1 | U2 | LHR002 | *2 |
| 23 | 1 | U6 | 16ST0009P | *2 |
| 24 | 1 | U3 | DP83851 | *3 |
| 25 | 1 | U8 | DP83846A | *3 |
| 26 | 1 | U7 | AMS117 | SMD |
| 27 | 1 | Y1 | 25MHZ CRYSTAL | DIP |
| 28 | 1 | J2 | RJ11 | DIP |
| 39 | 2 | J3,J5 | CON8 | DIP |
| 30 | 1 | J4 | RJ45 | DIP |
| 31 | 1 | J1 | PCMCIA-15 | *4 |
| 32 | 1 | U4 | PCMCIA-68 | *4 |

**Sponsors of Components**

| Components | Company | Contact person | Telephone |
|----------------------------------|--------------------------|-----------------------|------------------|
| SIDACtor (P0800SA) | GID GLORIA INTERNATIONAL | Jason Hsu | 02-25068371 |
| TRANSFORMERS | BOTHHAND ENTERPRISE INC. | Dennis Fan | 03-3698237 |
| PHYceiver | National Semiconductor | Henry Chou | 02-25370217 |
| HONDA PCMCIA connectors & Frames | Yun Hui Ltd. | Zong-Ming Chen | 02-27669242 |



Sponsors of Components (Chinese)

| Components | Company | Contact person | Telephone |
|----------------------------------|---|-----------------------|-------------|
| SIDACTor (P0800SA) | GID GLORIA INTERNATIONAL ○ á _ e Ū s ¼ q | Jason Hsu ® P ø È | 02-25068371 |
| TRANSFORMERS | BOTHHAND ENTERPRISE INC. © o s N † s ¼ q | Dennis Fan - S φ " | 03-3698237 |
| PHYceiver | National Semiconductor | Henry Chou © P A i | 02-25370217 |
| HONDA PCMCIA connectors & Frames | ¼ ¶ * s ¼ q | s Á © ú | 02-27669242 |