Rad Hard 40V Quad Precision Low Power Operational Amplifiers

ISL70417SEH

The ISL70417SEH contains four very high precision amplifiers featuring the perfect combination of low noise vs power consumption. Low offset voltage, low I_{BIAS} current and low temperature drift making them the ideal choice for applications requiring both high DC accuracy and AC performance. The combination of high precision, low noise, low power and small footprint provides the user with outstanding value and flexibility relative to similar competitive parts.

Applications for these amplifiers include precision active filters, medical and analytical instrumentation, precision power supply controls, and industrial controls.

The ISL70417SEH is offered in a 14 lead hermetic ceramic flatpack package. The device is offered in an industry standard pin configuration and operates over the extended temperature range from -55°C to +125°C.

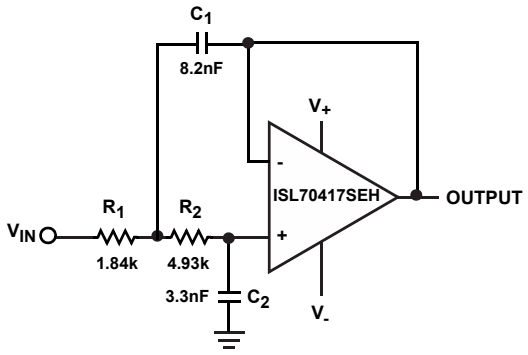
Applications

- Precision Instrumentation
- Spectral Analysis Equipment
- Active Filter Blocks
- Thermocouples and RTD Reference Buffers
- Data Acquisition
- Power Supply Control

Features

- **Electrically Screened to DLA SMD# 5962-12228**
- **Low Input Offset Voltage . . . . . ±110µV, Max.**
- **Superb Offset Temperature Coefficient . . . . . 1µV/°C, Max.**
- **Input Bias Current. . . . . ±5nA, Max.**
- **Input Bias Current TC . . . . . ±5pA/°C, Max.**
- **Low Current Consumption 440µA**
- Voltage Noise . . . . . 8nV/√Hz
- Wide Supply Range . . . . . 4.5V to 40V
- Operating Temperature Range. . . . . -55°C to +125°C
- Radiation Environment
  - SEL/SEB LET_{TH} (V_S = ±20V). . . . . 73.9 MeV•cm^2/mg
  - Total Dose, High Dose Rate . . . . . 300krad(Si)
  - Total Dose, Low Dose Rate . . . . . 100krad(Si) *

* Product capability established by initial characterization. The EH version is acceptance tested on a wafer by wafer basis to 50krad(Si) at low dose rate.



SALLEN-KEY LOW PASS FILTER (f_C = 10kHz)

FIGURE 1. TYPICAL APPLICATION

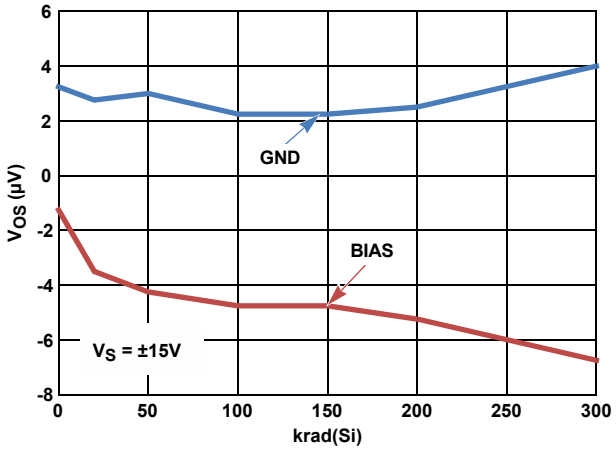


FIGURE 2. V_{OS} SHIFT vs HIGH DOSE RATE RADIATION

Ordering Information

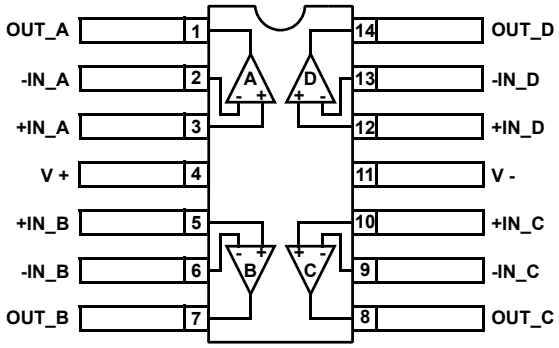
ORDERING NUMBER	PART NUMBER (Notes 2, 3)	TEMPERATURE RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
5962R1222801VXC	ISL70417SEHVF	-55 to +125	14 Ld Flatpack	K14.A
ISL70417SEHF/PROTO	ISL70417SEHF/PROTO	-55 to +125	14 Ld Flatpack	K14.A
5962R1222801V9AX	ISL70417SEHVX	-55 to +125	DIE	
ISL70417SEHX/SAMPLE	ISL70417SEHX/SAMPLE	-55 to +125	DIE	
ISL70417SEHEVAL1Z	Evaluation Board			

NOTES:

1. These Intersil Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.
2. For Moisture Sensitivity Level (MSL), please see device information page for ISL70417SEH. For more information on MSL please see tech brief TB363.

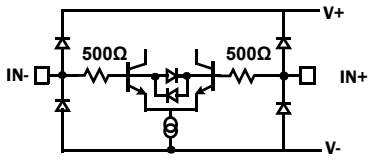
Pin Configuration

ISL70417SEH
(14 LD FLATPACK)
TOP VIEW

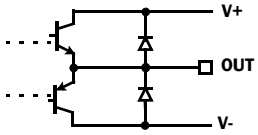


Pin Descriptions

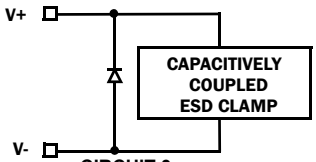
ISL70417SEH (14 LD FLATPACK)	PIN NAME	EQUIVALENT CIRCUIT	DESCRIPTION
1	OUT_A	Circuit 2	Amplifier A output
2	-IN_A	Circuit 1	Amplifier A inverting input
3	+IN_A	Circuit 1	Amplifier A non-inverting input
4	V+	Circuit 3	Positive power supply
5	+IN_B	Circuit 1	Amplifier B non-inverting input
6	-IN_B	Circuit 1	Amplifier B inverting input
7	OUT_B	Circuit 2	Amplifier B output
8	OUT_C	Circuit 2	Amplifier C output
9	-IN_C	Circuit 1	Amplifier C inverting input
10	+IN_C	Circuit 1	Amplifier C non-inverting input
11	V-	Circuit 3	Negative power supply
12	+IN_D	Circuit 1	Amplifier D non-inverting input
13	-IN_D	Circuit 1	Amplifier D inverting input
14	OUT_D	Circuit 2	Amplifier D output



CIRCUIT 1



CIRCUIT 2



CIRCUIT 3

Absolute Maximum Ratings

Maximum Supply Voltage 42V
Maximum Supply Voltage (LET = 73.9 MeV • cm^2/mg). 40V
Maximum Differential Input Current 20mA
Maximum Differential Input Voltage 20V
Min/Max Input Voltage ..... V- - 0.5V to V+ + 0.5V
Max/Min Input current for Input Voltage >V+ or <V- ..... ±20mA
Output Short-Circuit Duration (1 output at a time). ..... Indefinite
ESD Rating
Human Body Model (Tested per MIL-PRF-883 3015.7). 2kV
Machine Model (Tested per EIA/JESD22-A115-A) 300V
Charged Device Model (Tested per JESD22-C101D) 2kV

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
14 Ld Flatpack (Notes 3, 4).	105	15

Maximum Storage Temperature Range ..... -65°C to +150°C
Maximum Junction Temperature (T_{JMAX}) ..... +150°C
Pb-Free Reflow Profile ..... see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Recommended Operating Conditions

Ambient Operating Temperature Range ..... -55°C to +125°C
Maximum Operating Junction Temperature ..... +150°C
Supply Voltage ..... 4.5V (±2.25V) to 30V (±15V)

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

3. θ_{JA} is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
4. For θ_{JC}, the "case temp" location is the center of the ceramic on the package underside.

Electrical Specifications

V_S ± 15V, V_{CM} = 0, V_O = 0V, T_A = +25°C, unless otherwise noted. **Boldface limits apply over the operating temperature range, -55°C to +125°C; over a total ionizing dose of 300krad(Si) with exposure at a high dose rate of 50 - 300krad(Si)/s; and over a total ionizing dose of 50krad(Si) with exposure a low dose rate of <10mrad(Si)/s.**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 5)	TYP	MAX (Note 5)	UNIT
V_{OS}	Input Offset Voltage			10	75	µV
					110	µV
TCV_{OS}	Offset Voltage Drift			0.1	**1**	µV/°C
I_B	Input Bias Current		-1	0.08	1	nA
			-5		**5**	nA
TCI_B	Input Bias Current Temperature Coefficient		**-5**	**1**	**5**	pA/°C
I_{OS}	Input Offset Current		-1.5	0.08	1.5	nA
			-3		**3**	nA
TCI_{OS}	Input Offset Current Temperature Coefficient		**-3**	**0.42**	**3**	pA/°C
V_{CM}	Input Voltage Range	Guaranteed by CMRR test	**-13**		**13**	V
CMRR	Common-Mode Rejection Ratio	V_{CM} = -13V to +13V	120	145		dB
			120			dB
PSRR	Power Supply Rejection Ratio	V_S = ±2.25V to ±20V	120	145		dB
			120			dB
A_{VOL}	Open-Loop Gain	V_O = -13V to +13V, R_L = 10kΩ to ground	3,000	14,000		V/mV
V_{OH}	Output Voltage High	R_L = 10kΩ to ground	13.5	13.7		V
			13.2			V
		R_L = 2kΩ to ground	13.3	13.55		V
			13.0			V
V_{OL}	Output Voltage Low	R_L = 10kΩ to ground		-13.7	-13.5	V
					-13.2	V
		R_L = 2kΩ to ground		-13.55	-13.3	V
					-13.0	V

Electrical Specifications $V_S \pm 15V$, $V_{CM} = 0$, $V_O = 0V$, $T_A = +25°C$, unless otherwise noted. **Boldface limits apply over the operating temperature range, -55°C to +125°C; over a total ionizing dose of 300krad(Si) with exposure at a high dose rate of 50 - 300krad(Si)/s; and over a total ionizing dose of 50krad(Si) with exposure a low dose rate of <10mrad(Si)/s. (Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 5)	TYP	MAX (Note 5)	UNIT
I_S	Supply Current/Amplifier			0.44	0.53	mA
					0.68	mA
I_{SC}	Short-Circuit Current			43		mA
V_{SUPPLY}	Supply Voltage Range	Guaranteed by PSRR	**± 2.25**		**± 20**	V
AC SPECIFICATIONS						
GBWP	Gain Bandwidth Product	$A_V = 1k$, $R_L = 2k\Omega$		1.5		MHz
e_{nVp-p}	Voltage Noise V_{P-P}	0.1Hz to 10Hz		0.25		μV_{P-P}
e_n	Voltage Noise Density	f = 10Hz		10		$nV/\sqrt{Hz}$
e_n	Voltage Noise Density	f = 100Hz		8.2		$nV/\sqrt{Hz}$
e_n	Voltage Noise Density	f = 1kHz		8		$nV/\sqrt{Hz}$
e_n	Voltage Noise Density	f = 10kHz		8		$nV/\sqrt{Hz}$
in	Current Noise Density	f = 1kHz		0.1		$pA/\sqrt{Hz}$
THD + N	Total Harmonic Distortion	1kHz, G = 1, $V_O = 3.5V_{RMS}$, $R_L = 2k\Omega$		0.0009		%
		1kHz, G = 1, $V_O = 3.5V_{RMS}$, $R_L = 10k\Omega$		0.0005		%
TRANSIENT RESPONSE						
SR	Slew Rate, V_{OUT} 20% to 80%	$A_V = 11$, $R_L = 2k\Omega$, $V_O = 4V_{P-P}$	0.3	0.5		V/µs
			0.2			V/µs
t_r, t_f, Small Signal	Rise Time 10% to 90% of V_{OUT}	$A_V = 1$, $V_{OUT} = 50mV_{P-P}$, $R_L = 10k\Omega$ to V_{CM}		130	450	ns
					625	ns
	Fall Time 90% to 10% of V_{OUT}	$A_V = 1$, $V_{OUT} = 50mV_{P-P}$, $R_L = 10k\Omega$ to V_{CM}		130	600	ns
					700	ns
t_s	Settling Time to 0.1% 10V Step; 10% to V_{OUT}	$A_V = -1$, $V_{OUT} = 10V_{P-P}$, $R_L = 5k\Omega$ to V_{CM}		21		µs
	Settling Time to 0.01% 10V Step; 10% to V_{OUT}	$A_V = -1$, $V_{OUT} = 10V_{P-P}$, $R_L = 5k\Omega$ to V_{CM}		24		µs
	Settling Time to 0.1% 4V Step; 10% to V_{OUT}	$A_V = -1$, $V_{OUT} = 4V_{P-P}$, $R_L = 5k\Omega$ to V_{CM}		13		µs
	Settling Time to 0.01% 4V Step; 10% to V_{OUT}	$A_V = -1$, $V_{OUT} = 4V_{P-P}$, $R_L = 5k\Omega$ to V_{CM}		18		µs
t_{OL}	Output Positive Overload Recovery Time	$A_V = -100$, $V_{IN} = 0.2V_{P-P}$, $R_L = 2k\Omega$ to V_{CM}		5.6		µs
	Output Negative Overload Recovery Time	$A_V = -100$, $V_{IN} = 0.2V_{P-P}$, $R_L = 2k\Omega$ to V_{CM}		10.6		µs
OS+	Positive Overshoot	$A_V = 1$, $V_{OUT} = 10V_{P-P}$, $R_f = 0\Omega$ $R_L = 2k\Omega$ to V_{CM}		15		%
					33	%
OS-	Negative Overshoot	$A_V = 1$, $V_{OUT} = 10V_{P-P}$, $R_f = 0\Omega$ $R_L = 2k\Omega$ to V_{CM}		15		%
					33	%

Electrical Specifications

V_S ± 5V, V_{CM} = 0, V_O = 0V, T_A = +25°C, unless otherwise noted. **Boldface limits apply over the operating temperature range, -55°C to +125°C; over a total ionizing dose of 300krad(Si) with exposure at a high dose rate of 50 - 300krad(Si)/s; and over a total ionizing dose of 50krad(Si) with exposure a low dose rate of <10mrad(Si)/s.**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 5)	TYP	MAX (Note 5)	UNIT
V_{OS}	Input Offset Voltage			10	150	µV
					250	µV
TCV_{OS}	Offset Voltage Drift			0.1	**1**	µV/°C
I_B	Input Bias Current		-1	0.18	1	nA
			-5		**5**	nA
TCI_B	Input Bias Current Temperature Coefficient		**-5**	**1**	**5**	pA/°C
I_{OS}	Input Offset Current		-1.5	0.3	1.5	nA
			-3		**3**	nA
TCI_{OS}	Input Offset Current Temperature Coefficient		**-3**	**0.42**	**3**	pA/°C
V_{CM}	Input Voltage Range		**-3**		**3**	V
CMRR	Common-Mode Rejection Ratio	V_{CM} = -3V to +3V	120	145		dB
			120			dB
PSRR	Power Supply Rejection Ratio	V_S = ±2.25V to ±5V	120	145		dB
			120			dB
A_{VOL}	Open-Loop Gain	V_O = -3.0V to +3.0V R_L = 10kΩ to ground	3,000	14,000		V/mV
V_{OH}	Output Voltage High	R_L = 10kΩ to ground	3.5	3.7		V
			3.2			V
		R_L = 2kΩ to ground	3.3	3.55		V
			3.0			V
V_{OL}	Output Voltage Low	R_L = 10kΩ to ground		-3.7	-3.5	V
					-3.2	V
		R_L = 2kΩ to ground		-3.55	-3.3	V
					-3.0	V
I_S	Supply Current/Amplifier			0.44	0.53	mA
					0.68	mA
I_{SC}	Short-Circuit Current			43		mA
AC SPECIFICATIONS						
GBWP	Gain Bandwidth Product	A_V = 1k, R_L = 2kΩ		1.5		MHz
e_{np-p}	Voltage Noise	0.1Hz to 10Hz		0.25		$µV_{P-P}$
e_n	Voltage Noise Density	f = 10Hz		12		nV/√Hz
e_n	Voltage Noise Density	f = 100Hz		8.6		nV/√Hz
e_n	Voltage Noise Density	f = 1kHz		8		nV/√Hz
e_n	Voltage Noise Density	f = 10kHz		8		nV/√Hz
in	Current Noise Density	f = 1kHz		0.1		pA/√Hz
TRANSIENT RESPONSE						
SR	Slew Rate, V_{OUT} 20% to 80%	A_V = 11, R_L = 2kΩ, V_O = $4V_{P-P}$		0.5		V/µs

Electrical Specifications $V_S \pm 5V$, $V_{CM} = 0$, $V_O = 0V$, $T_A = +25°C$, unless otherwise noted. **Boldface limits apply over the operating temperature range, -55°C to +125°C; over a total ionizing dose of 300krad(Si) with exposure at a high dose rate of 50 - 300krad(Si)/s; and over a total ionizing dose of 50krad(Si) with exposure a low dose rate of <10mrad(Si)/s. (Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 5)	TYP	MAX (Note 5)	UNIT
t_r, t_f, Small Signal	Rise Time 10% to 90% of V_{OUT}	$A_V = 1$, $V_{OUT} = 50mV_{P-P}$, $R_L = 10k\Omega$ to V_{CM}		130		ns
	Fall Time 90% to 10% of V_{OUT}	$A_V = 1$, $V_{OUT} = 50mV_{P-P}$, $R_L = 10k\Omega$ to V_{CM}		130		ns
t_S	Settling Time to 0.1% 4V Step; 10% to V_{OUT}	$A_V = -1$, $V_{OUT} = 4V_{P-P}$, $R_L = 5k\Omega$ to V_{CM}		12		µs
	Settling Time to 0.01% 4V Step; 10% to V_{OUT}	$A_V = -1$, $V_{OUT} = 4V_{P-P}$, $R_L = 5k\Omega$ to V_{CM}		19		µs
t_{OL}	Output Positive Overload Recovery Time	$A_V = -100$, $V_{IN} = 0.2V_{P-P}$ $R_L = 2k\Omega$ to V_{CM}		7		µs
	Output Negative Overload Recovery Time	$A_V = -100$, $V_{IN} = 0.2V_{P-P}$ $R_L = 2k\Omega$ to V_{CM}		5.8		µs
OS+	Positive Overshoot	$A_V = 1$, $V_{OUT} = 10V_{P-P}$, $R_f = 0\Omega$ $R_L = 2k\Omega$ to V_{CM}		15		%
OS-	Negative Overshoot	$A_V = 1$, $V_{OUT} = 10V_{P-P}$, $R_f = 0\Omega$ $R_L = 2k\Omega$ to V_{CM}		15		%

NOTE:

5. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

Typical Performance Curves

V_S = ±15V, V_{CM} = 0V, R_L = Open, T_A = +25°C, unless otherwise specified.

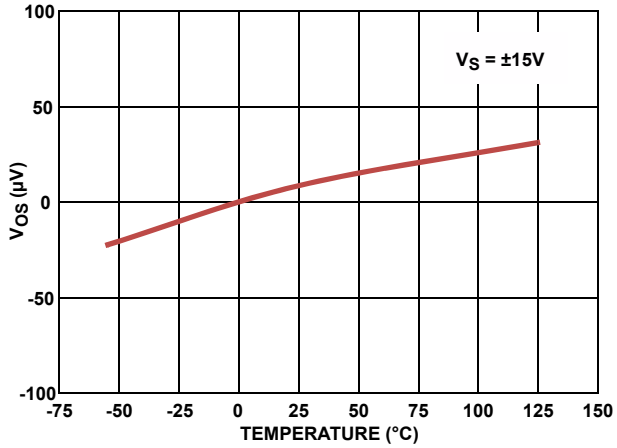


FIGURE 3. V_{OS} vs TEMPERATURE

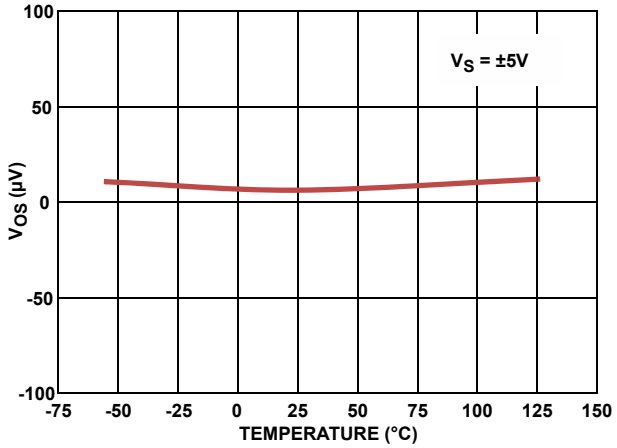


FIGURE 4. V_{OS} vs TEMPERATURE

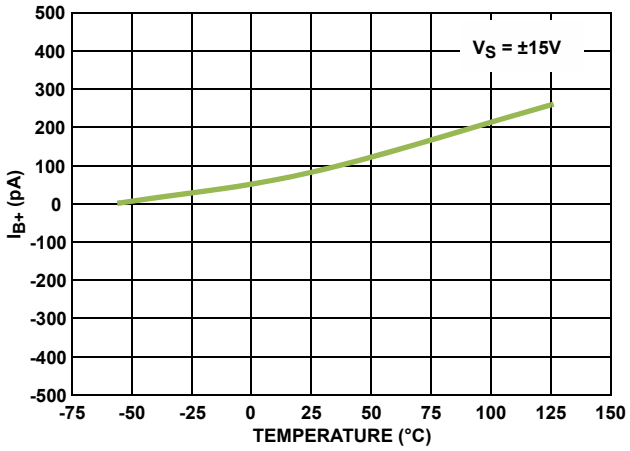


FIGURE 5. I_{B+} vs TEMPERATURE

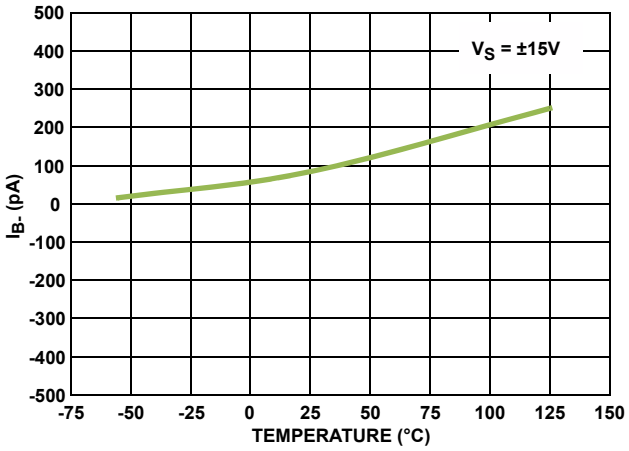


FIGURE 6. I_{B-} vs TEMPERATURE

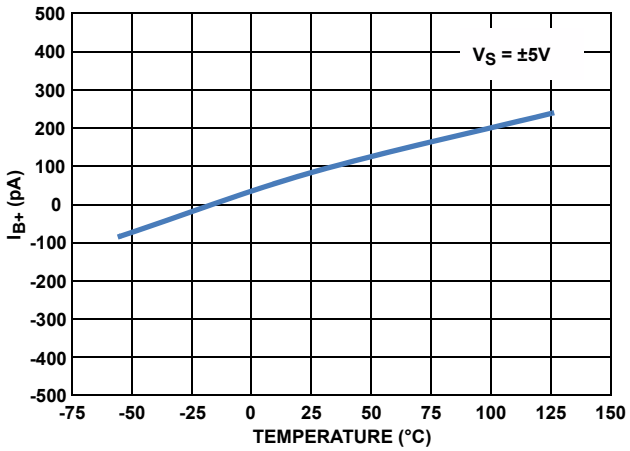


FIGURE 7. I_{B+} vs TEMPERATURE

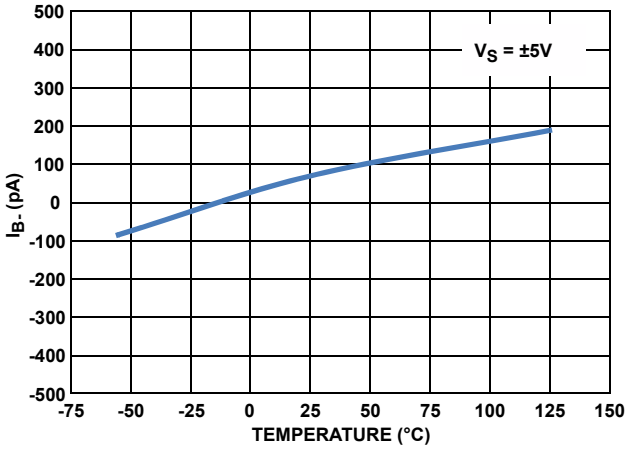


FIGURE 8. I_{B-} vs TEMPERATURE

Typical Performance Curves

V_S = ±15V, V_{CM} = 0V, R_L = Open, T_A = +25°C, unless otherwise specified. **(Continued)**

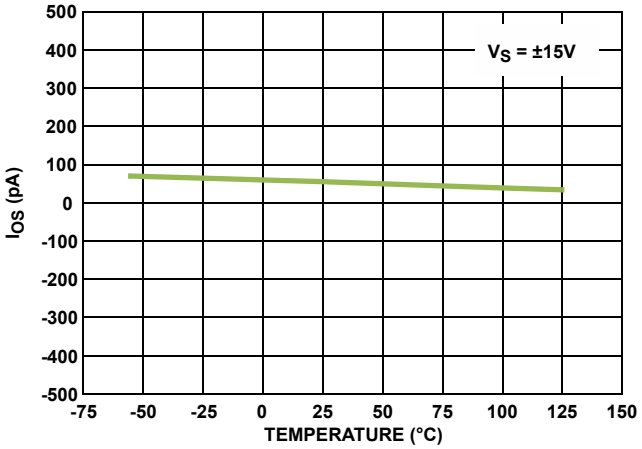


FIGURE 9. I_{OS} vs TEMPERATURE

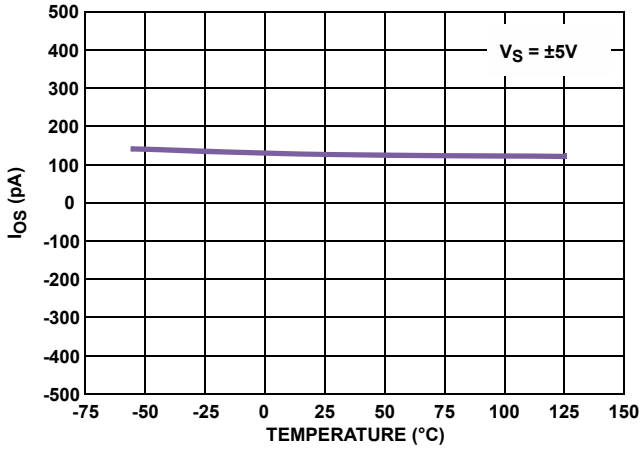


FIGURE 10. I_{OS} vs TEMPERATURE

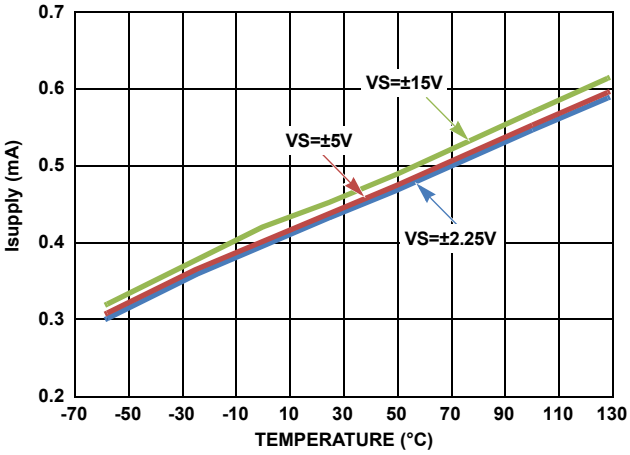


FIGURE 11. SUPPLY CURRENT PER AMP vs TEMPERATURE

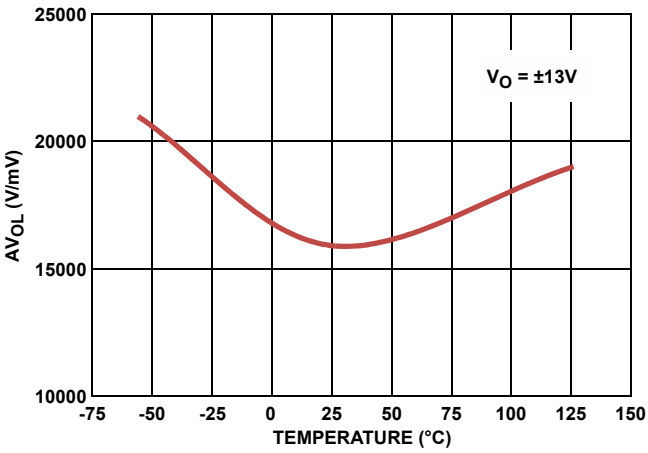


FIGURE 12. AV_{OL} vs TEMPERATURE

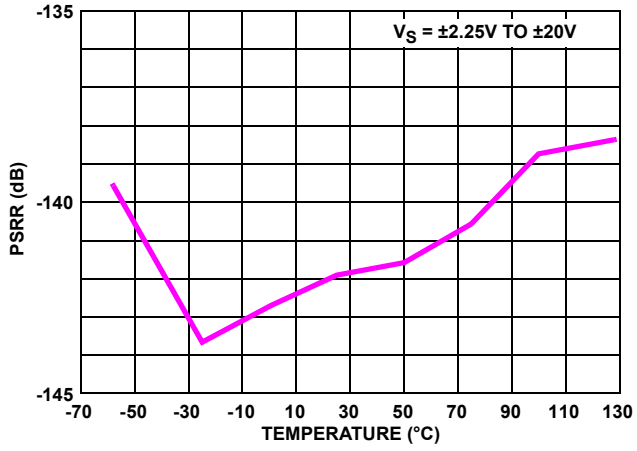


FIGURE 13. PSRR vs TEMPERATURE

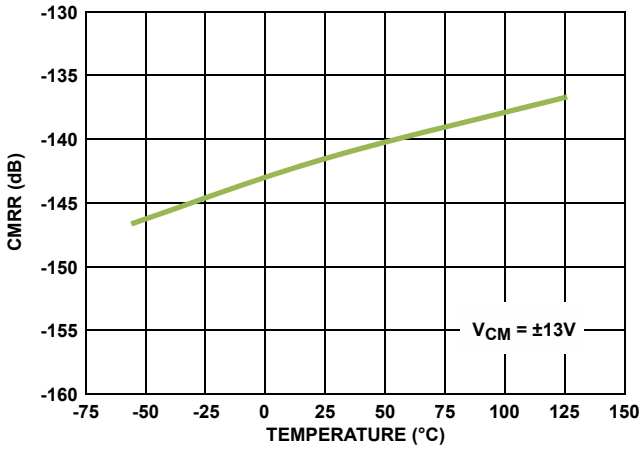


FIGURE 14. CMRR vs TEMPERATURE

Typical Performance Curves

V_S = ±15V, V_{CM} = 0V, R_L = Open, T_A = +25°C, unless otherwise specified. **(Continued)**

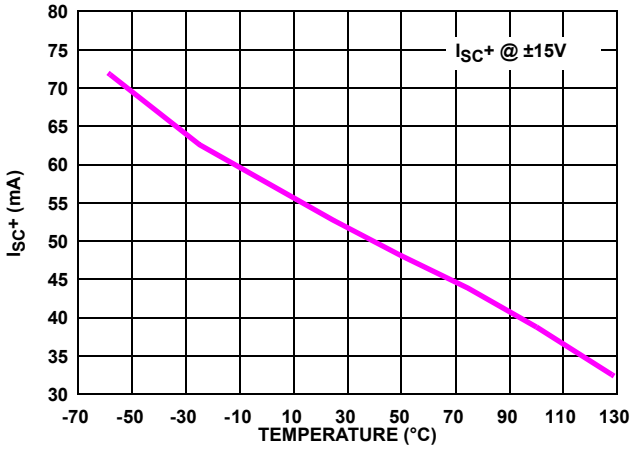


FIGURE 15. SHORT CIRCUIT CURRENT vs TEMPERATURE

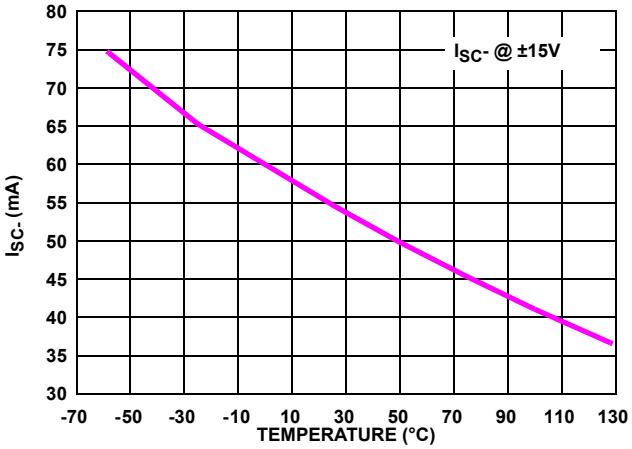


FIGURE 16. SHORT CIRCUIT CURRENT vs TEMPERATURE

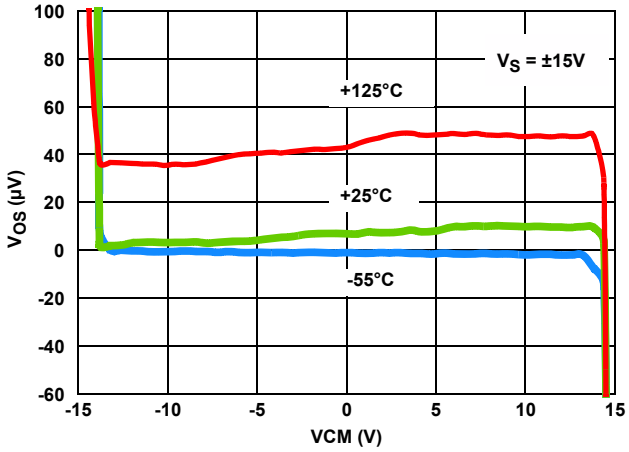


FIGURE 17. INPUT V_{OS} vs INPUT COMMON MODE VOLTAGE, V_S = ±15

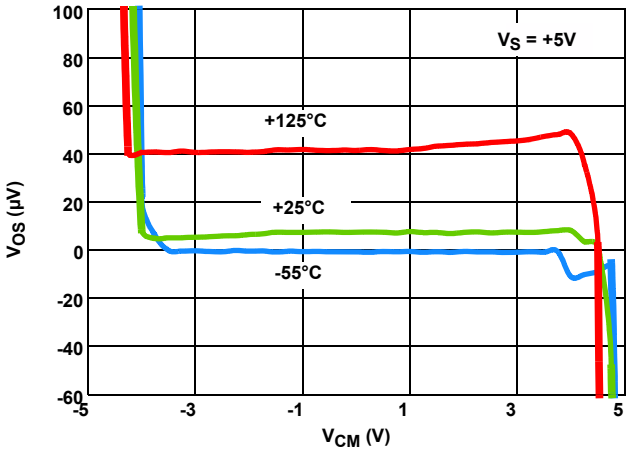


FIGURE 18. INPUT V_{OS} vs INPUT COMMON MODE VOLTAGE, V_S = ±5V

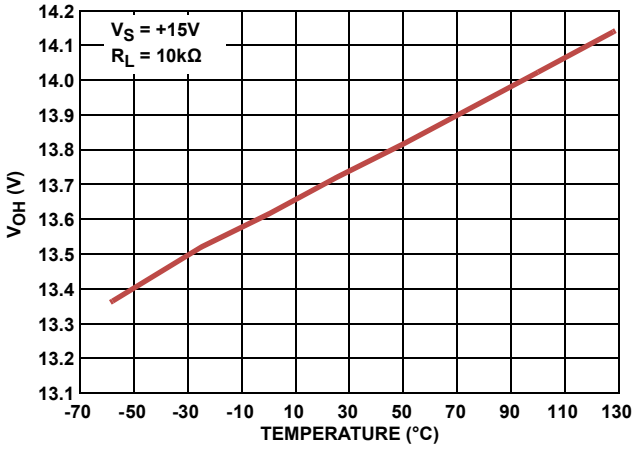


FIGURE 19. V_{OUT} vs TEMPERATURE

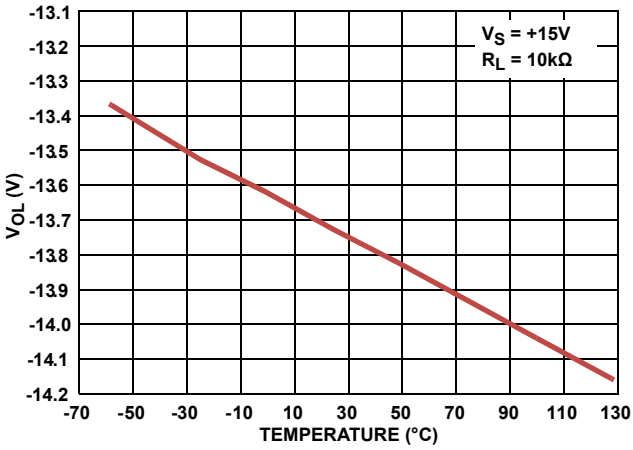


FIGURE 20. V_{OUT} vs TEMPERATURE

Typical Performance Curves

V_S = ±15V, V_{CM} = 0V, R_L = Open, T_A = +25°C, unless otherwise specified. **(Continued)**

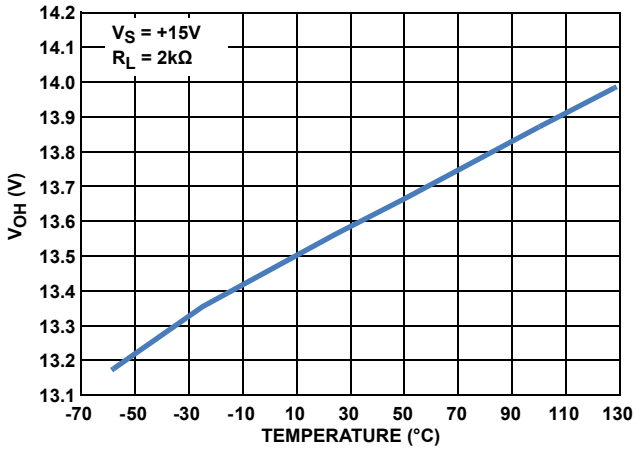


FIGURE 21. V_{OUT} vs TEMPERATURE

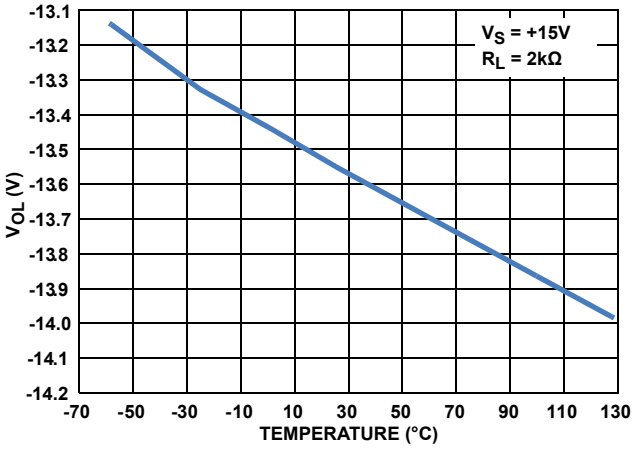


FIGURE 22. V_{OUT} vs TEMPERATURE

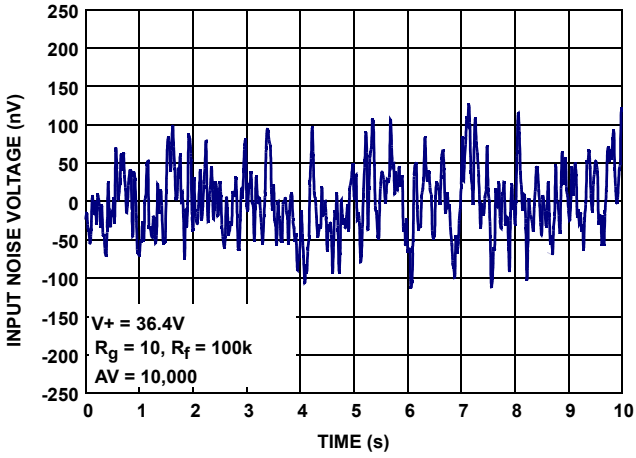


FIGURE 23. INPUT NOISE VOLTAGE 0.1Hz to 10Hz

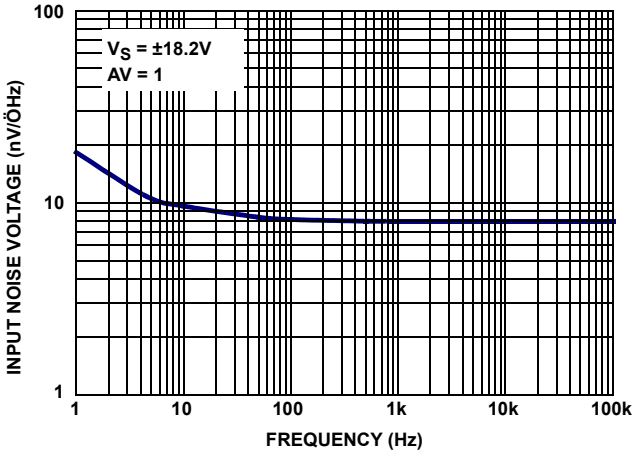


FIGURE 24. INPUT NOISE VOLTAGE SPECTRAL DENSITY

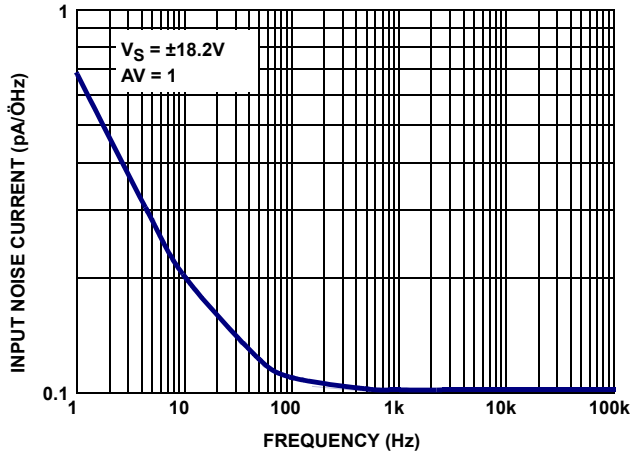


FIGURE 25. INPUT NOISE CURRENT SPECTRAL DENSITY

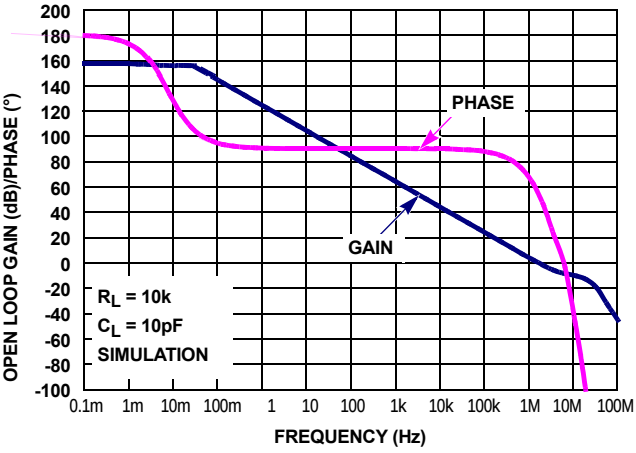


FIGURE 26. OPEN-LOOP GAIN, PHASE vs FREQUENCY, R_L = 10kΩ, C_L = 10pF

Typical Performance Curves

V_S = ±15V, V_{CM} = 0V, R_L = Open, T_A = +25°C, unless otherwise specified. **(Continued)**

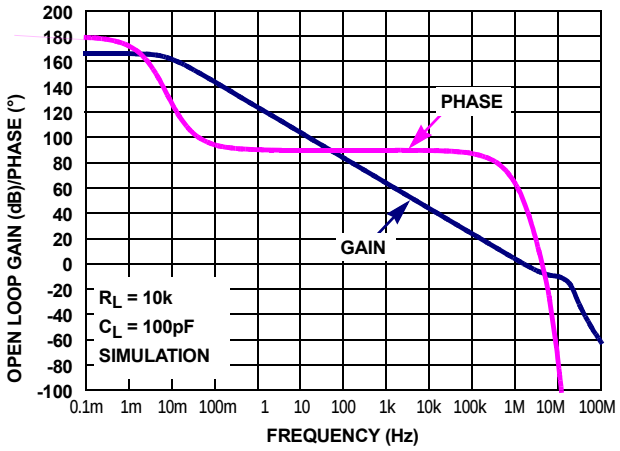


FIGURE 27. OPEN-LOOP GAIN, PHASE vs FREQUENCY, R_L = 10kΩ, C_L = 100pF

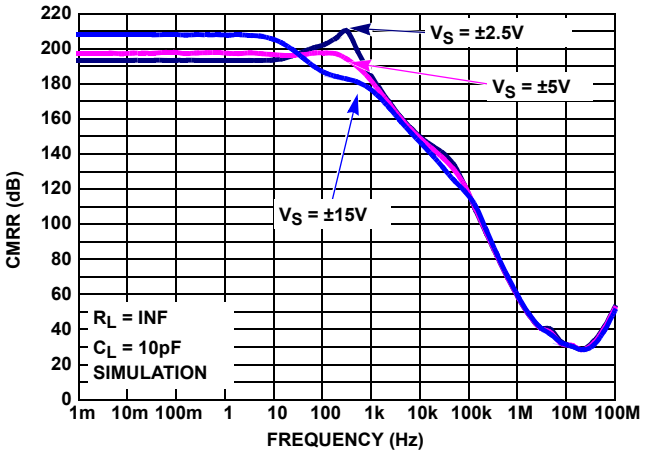


FIGURE 28. CMRR vs FREQUENCY, V_S = ±2.25, ±5V, ±15V

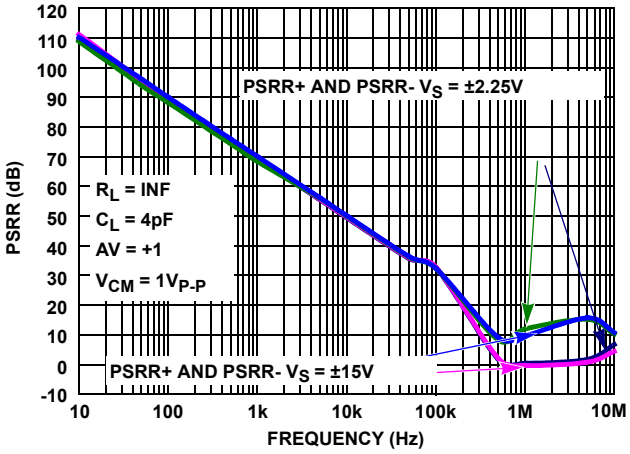


FIGURE 29. PSRR vs FREQUENCY, V_S = ±5V, ±15V

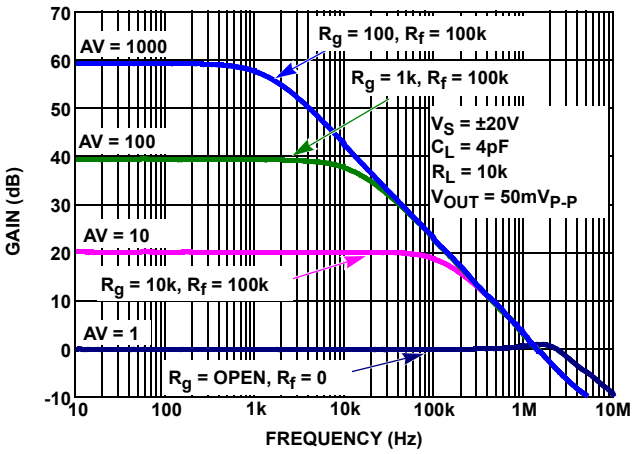


FIGURE 30. FREQUENCY RESPONSE vs CLOSED LOOP GAIN

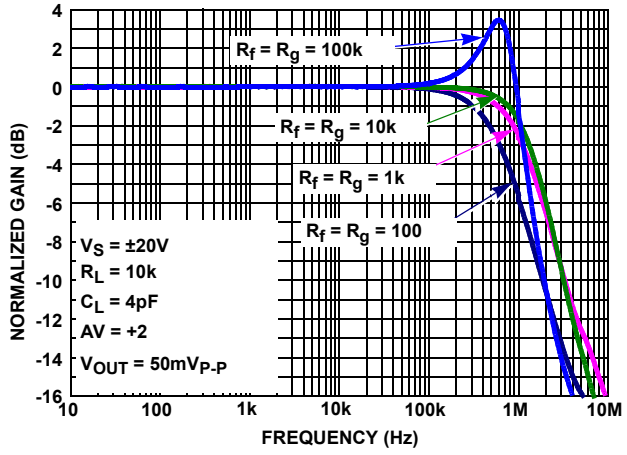


FIGURE 31. FREQUENCY RESPONSE vs FEEDBACK RESISTANCE R_f/R_g

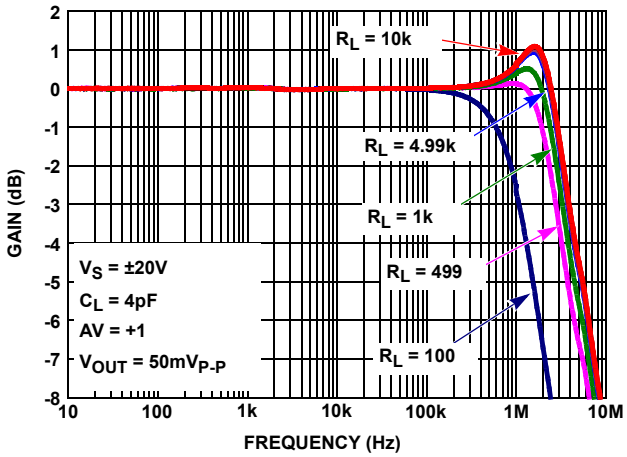


FIGURE 32. GAIN vs FREQUENCY vs R_L

Typical Performance Curves

V_S = ±15V, V_{CM} = 0V, R_L = Open, T_A = +25°C, unless otherwise specified. **(Continued)**

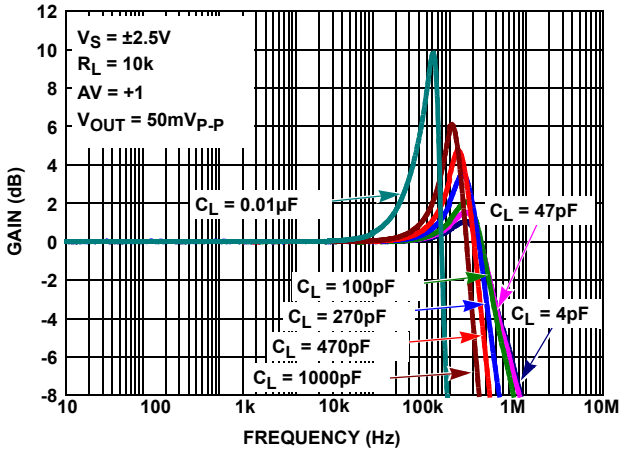


FIGURE 33. GAIN vs FREQUENCY vs C_L

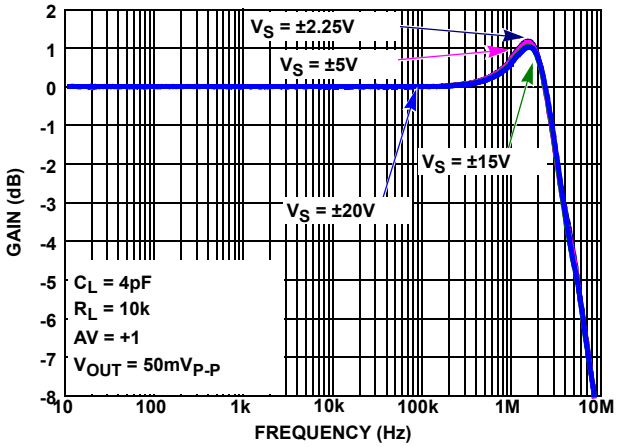


FIGURE 34. GAIN vs FREQUENCY vs SUPPLY VOLTAGE

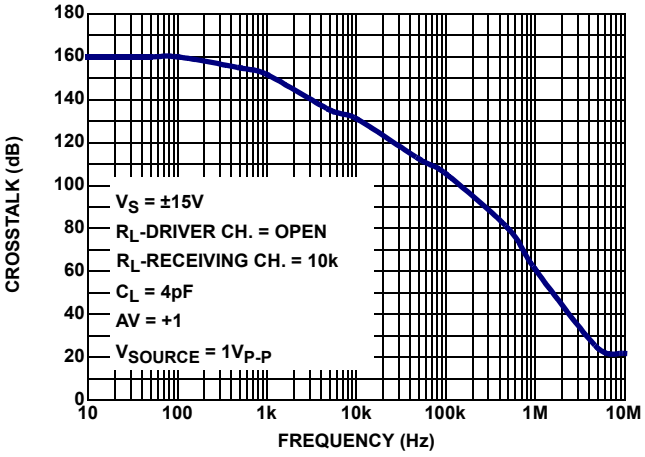


FIGURE 35. CROSSTALK, V_S = ±15V

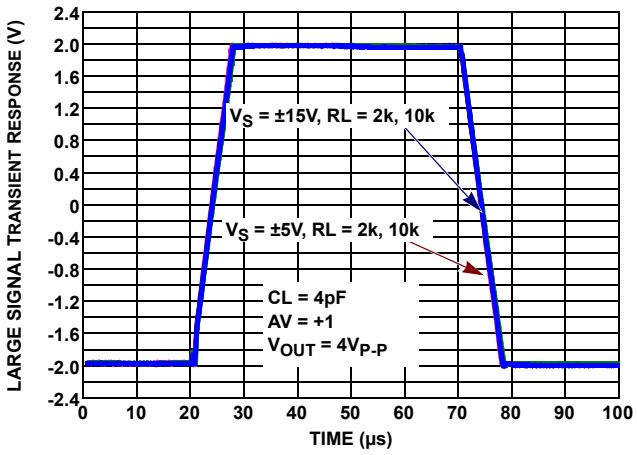


FIGURE 36. LARGE SIGNAL TRANSIENT RESPONSE vs R_L V_S = ±5V, ±15V

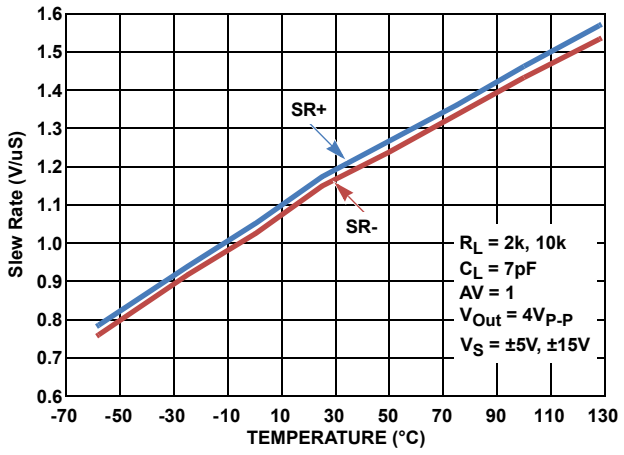


FIGURE 37. SLEW RATE vs TEMPERATURE V_S = ±5V, ±15V

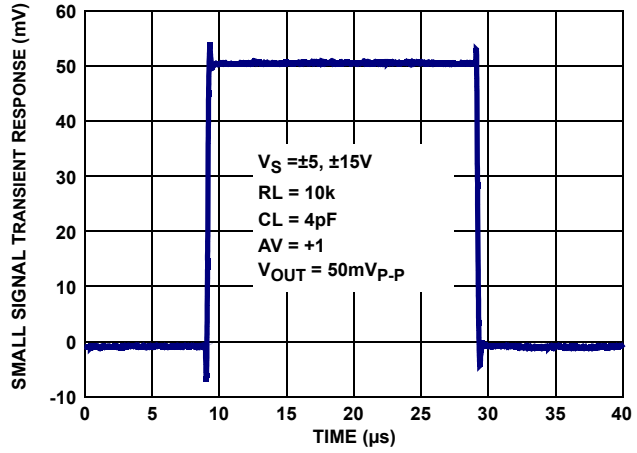


FIGURE 38. SMALL SIGNAL TRANSIENT RESPONSE, V_S = ±5V, ±15V

Typical Performance Curves

V_S = ±15V, V_{CM} = 0V, R_L = Open, T_A = +25°C, unless otherwise specified. **(Continued)**

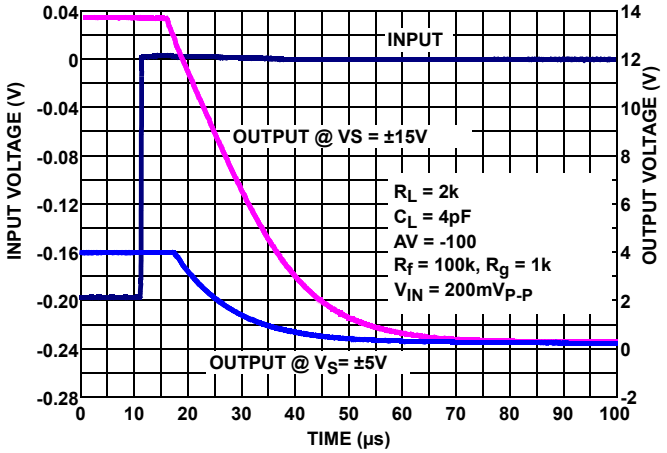


FIGURE 39. POSITIVE OUTPUT OVERLOAD RESPONSE TIME, V_S = ±5V, ±15V

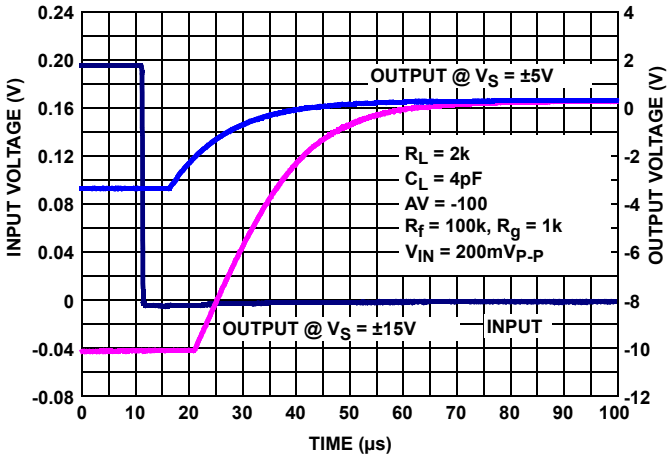


FIGURE 40. NEGATIVE OUTPUT OVERLOAD RESPONSE TIME, V_S = ±5V, ±15V

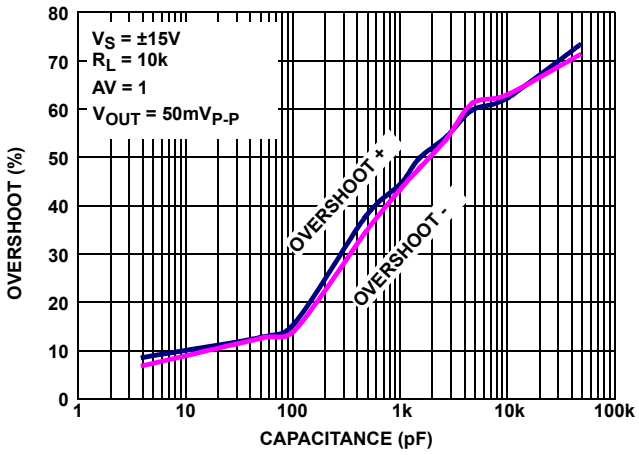


FIGURE 41. % OVERSHOOT vs LOAD CAPACITANCE, V_S = ±15V

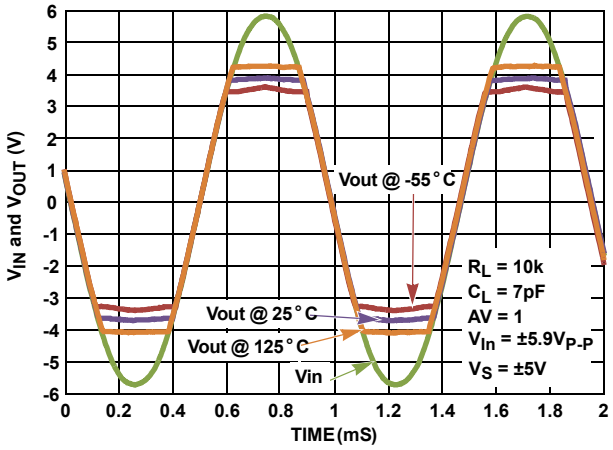


FIGURE 42. OUTPUT PHASE REVERSAL RESPONSE vs TEMPERATURE

Post High Dose Radiation Characteristics Unless otherwise specified, V_S ± 15V, V_{CM} = 0, V_O = 0V, T_A = +25°C. **This data is typical mean test data post radiation exposure at a high dose rate of 50 - 300rad(Si)/s. This data is intended to show typical parameter shifts due to high dose rate radiation. These are not limits nor are they guaranteed**

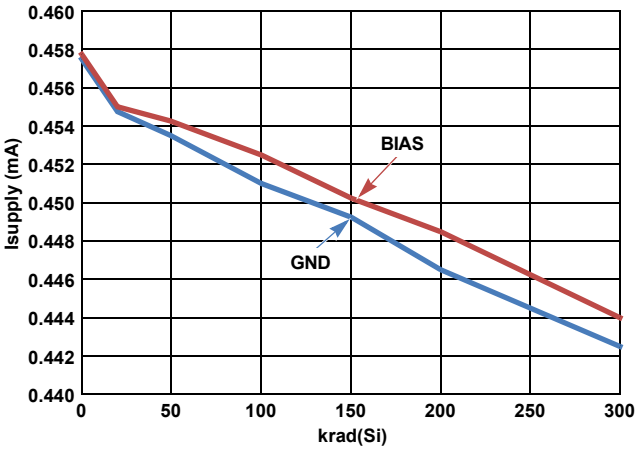


FIGURE 43. SUPPLY CURRENT PER AMP vs HIGH DOSE RATE RADIATION

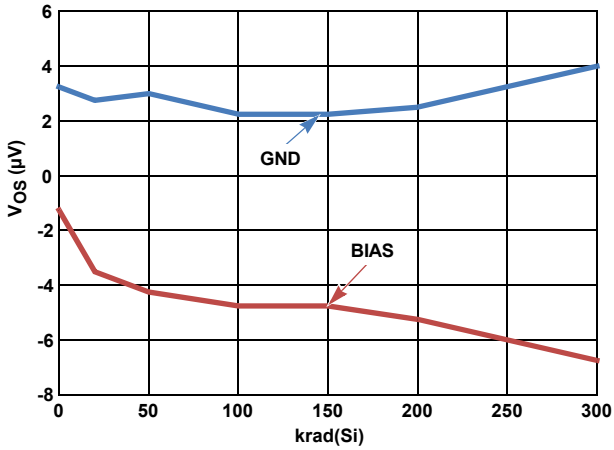


FIGURE 44. V_{OS} vs HIGH DOSE RATE RADIATION

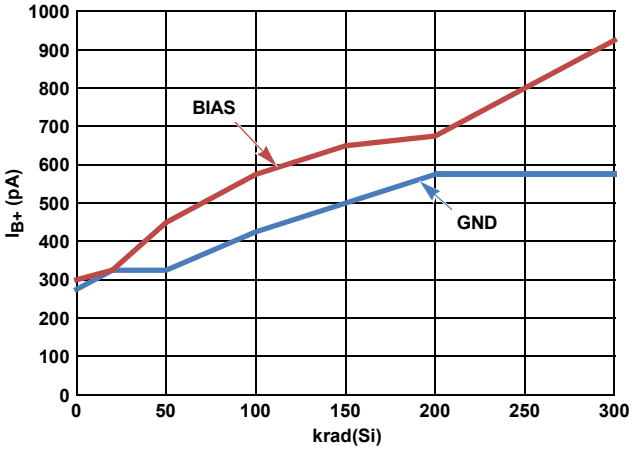


FIGURE 45. I_{B+} vs HIGH DOSE RATE RADIATION

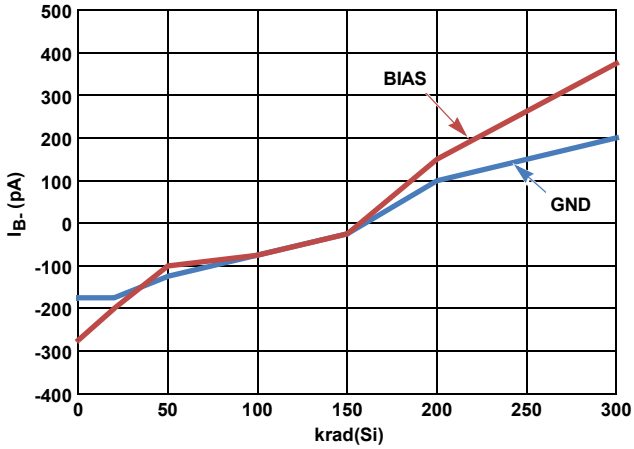


FIGURE 46. I_{B-} vs HIGH DOSE RATE RADIATION

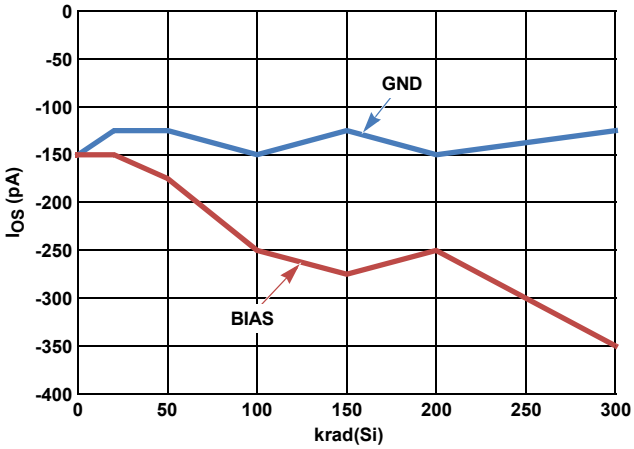


FIGURE 47. I_{OS} vs HIGH DOSE RATE RADIATION

Post Low Dose Radiation Characteristics Unless otherwise specified, V_S ± 15V, V_{CM} = 0, V_O = 0V, T_A = +25°C. **This data is typical mean test data post radiation exposure at a low dose rate of <10mrad(Si)/s. This data is intended to show typical parameter shifts due to low dose rate radiation. These are not limits nor are they guaranteed**

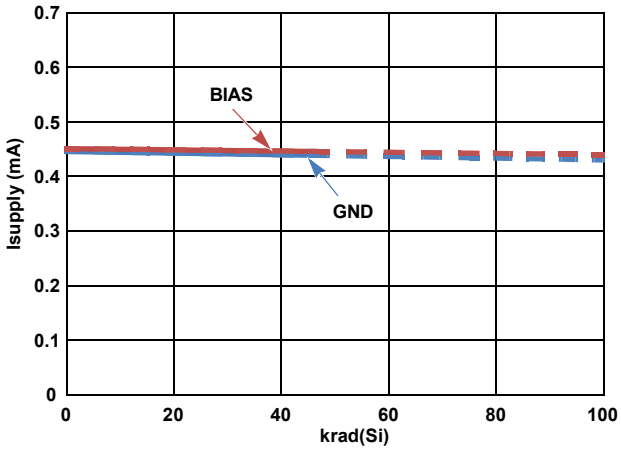


FIGURE 48. SUPPLY CURRENT PER AMP vs LOW DOSE RATE RADIATION

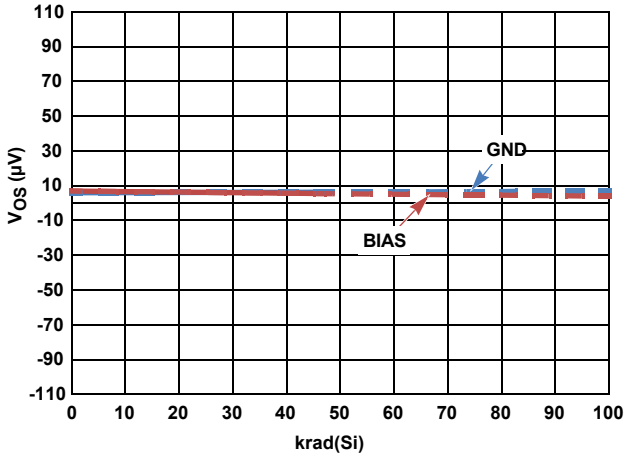


FIGURE 49. V_{OS} vs LOW DOSE RATE RADIATION

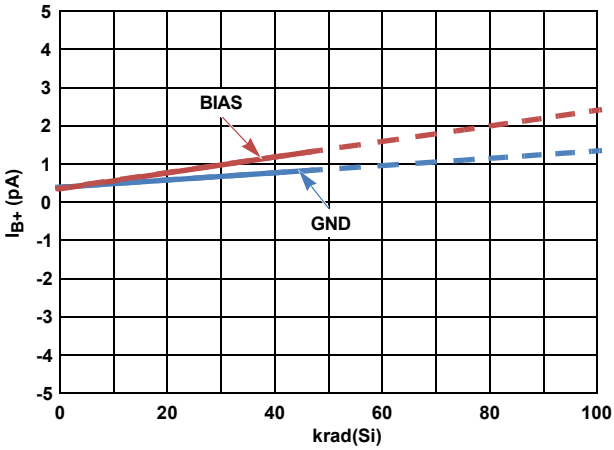


FIGURE 50. I_{B+} vs LOW DOSE RATE RADIATION

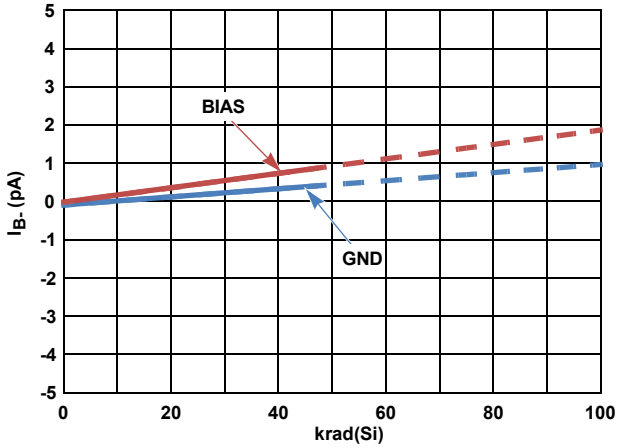


FIGURE 51. I_{B-} vs LOW DOSE RATE RADIATION

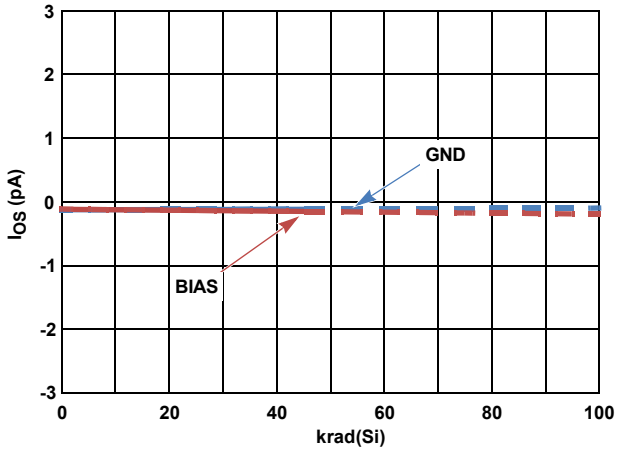


FIGURE 52. I_{OS} vs LOW DOSE RATE RADIATION

Applications Information

Functional Description

The ISL70417SEH contains four, low noise precision op amps. These devices are fabricated in a new precision 40V complementary bipolar DI process. A super-beta NPN input stage with input bias current cancellation provides low input bias current (180pA typical), low input offset voltage (13µV typical), low input noise voltage (8nV/√Hz), and low 1/f noise corner frequency (~8Hz). These amplifiers also feature high open loop gain (14kV/mV) for excellent CMRR (145dB) and THD+N performance (0.0005% @ 3.5V_{RMS}, 1kHz into 2kΩ). A complementary bipolar output stage enables high capacitive load drive without external compensation.

Operating Voltage Range

The devices are designed to operate over the 4.5V (±2.25V) to 40V (±20V) voltage range and are fully characterized at 10V (±5V) and 30V (±15V). The Power Supply Rejection Ratio typically exceeds 140dB over the full operating voltage range and 120dB minimum over the -55°C to +125°C temperature range. The worst case common mode input voltage range over temperature is 2V to each rail. With ±15V supplies, CMRR performance is typically >130dB over-temperature. The minimum CMRR performance over the -55°C to +125°C temperature range is >120dB for power supply voltages from ±5V (10V) to ±15V (30V).

Input Performance

The super-beta NPN input pair provides excellent frequency response while maintaining high input precision. High NPN beta (>1000) reduces input bias current while maintaining good frequency response, low input bias current and low noise. Input bias cancellation circuits provide additional bias current reduction to <5nA, and excellent temperature stabilization. Figures 6 through 8 show the high degree of bias current stability at ±5V and ±15V supplies that is maintained across the -55°C to +125°C temperature range. The low bias current TC also produces very low input offset current TC, which reduces DC input offset errors in precision, high impedance amplifiers.

The +25°C maximum input offset voltage (V_{OS}) is 75µV at ±15V supplies. Input offset voltage temperature coefficients ($V_{OS}TC$) is a maximum of ±1.0µV/°C. The V_{OS} temperature behavior is smooth (Figures 3 through 4) maintaining constant TC across the entire temperature range.

Input ESD Diode Protection

The input terminals (IN+ and IN-) have internal ESD protection diodes to the positive and negative supply rails, series connected 500Ω current limiting resistors and an anti-parallel diode pair across the inputs (Figure 53).

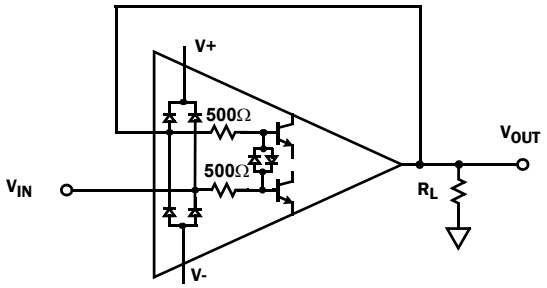


FIGURE 53. INPUT ESD DIODE CURRENT LIMITING- UNITY GAIN

The series resistors limit the high feed-through currents that can occur in pulse applications when the input dV/dT exceeds the 0.5V/µs slew rate of the amplifier. Without the series resistors, the input can forward-bias the anti-parallel diodes causing current to flow to the output resulting in severe distortion and possible diode failure.

Figure 36 provides an example of distortion free large signal response using a 4V_{P-P} input pulse with an input rise time of <1ns. The series resistors enable the input differential voltage to be equal to the maximum power supply voltage (40V) without damage.

In applications where one or both amplifier input terminals are at risk of exposure to high voltages beyond the power supply rails, current limiting resistors may be needed at the input terminal to limit the current through the power supply ESD diodes to 20mA max.

Output Current Limiting

The output current is internally limited to approximately ±45mA at +25°C and can withstand a short circuit to either rail as long as the power dissipation limits are not exceeded. This applies to only 1 amplifier at a time for the quad op amp. Continuous operation under these conditions may degrade long term reliability. Figures 15 and 16 show the current limit variation with temperature.

Output Phase Reversal

Output phase reversal is a change of polarity in the amplifier transfer function when the input voltage exceeds the supply voltage. The ISL70417SEH is immune to output phase reversal, even when the input voltage is 1V beyond the supplies.

Power Dissipation

It is possible to exceed the +150°C maximum junction temperatures under certain load and power supply conditions. It is therefore important to calculate the maximum junction temperature (T_{JMAX}) for all applications to determine if power supply voltages, load conditions, or package type need to be modified to remain in the safe operating area. These parameters are related using Equation 1:

$$T_{JMAX} = T_{MAX} + \theta_{JA} x PD_{MAXTOTAL} \quad \text{(EQ. 1)}$$

where:

- $P_{DMAXTOTAL}$ is the sum of the maximum power dissipation of each amplifier in the package (PD_{MAX})

- PD_{MAX} for each amplifier can be calculated using Equation 2:

$$PD_{MAX} = V_S \times I_{qMAX} + (V_S - V_{OUTMAX}) \times \frac{V_{OUTMAX}}{R_L} \quad \text{(EQ. 2)}$$

where:

- T_{MAX} = Maximum ambient temperature
- θ_{JA} = Thermal resistance of the package
- PD_{MAX} = Maximum power dissipation of 1 amplifier
- V_S = Total supply voltage
- I_{qMAX} = Maximum quiescent supply current of 1 amplifier
- V_{OUTMAX} = Maximum output voltage swing of the application

Package Characteristics

Weight of Packaged Device

0. 6043 Grams (Typical)

Lid Characteristics

Finish: Gold
Potential: Unbiased
Case Isolation to Any Lead: $20 \times 10^9\ \Omega$ (min)

Die Characteristics

Die Dimensions

2028µm x 2568µm (80mils x 101mils)
Thickness: 483µm ± 25µm (19mils ± 1 mil)

Interface Materials

GLASSIVATION

Type: Nitrox
Thickness: 15kÅ

TOP METALLIZATION

Type: AlCu (99.5%/0.5%)
Thickness: 30kÅ

BACKSIDE FINISH

Silicon

PROCESS

Dielectrically Isolated Complementary Bipolar - PR40

ASSEMBLY RELATED INFORMATION

SUBSTRATE POTENTIAL

Floating

ADDITIONAL INFORMATION

WORST CASE CURRENT DENSITY

$< 2 \times 10^5\ A/cm^2$

Metallization Mask Layout

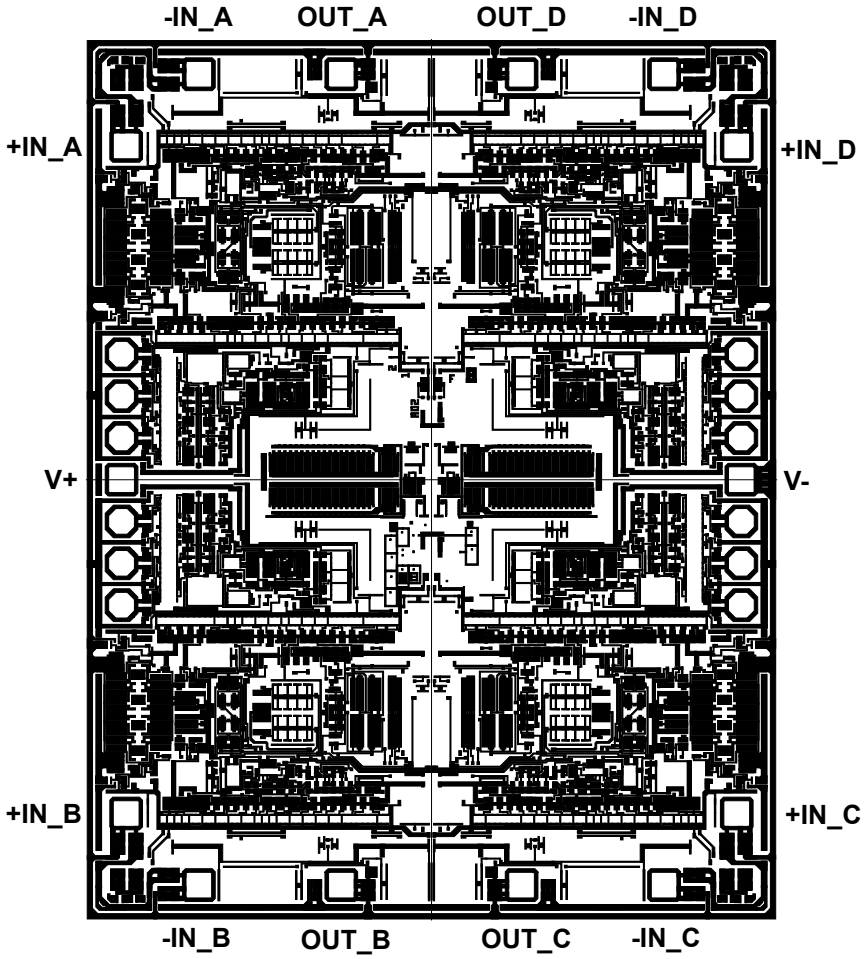


TABLE 1. DIE LAYOUT X-Y COORDINATES

PAD NAME	PAD NUMBER	X (µm)	Y (µm)	dX (µm)	dY (µm)	BOND WIRES PER PAD
OUT_A	3	-256	1152	70	70	1
-IN_A	4	-661	1152	70	70	1
+IN_A	5	-867.5	948.5	70	70	1
V+	9	-880.5	0	70	70	1
+IN_B	13	-867.5	-948.5	70	70	1
-IN_B	14	-661	-1152	70	70	1
OUT_B	15	-256	-1152	70	70	1
OUT_C	16	256	-1152	70	70	1
-IN_C	17	661	-1152	70	70	1
+IN_C	18	867.5	-948.5	70	70	1
V-	22	880.5	0	70	70	1
+IN_D	26	867.5	948.5	70	70	1
-IN_D	1	661	1152	70	70	1
OUT_D	2	256	1152	70	70	1

NOTE:

6. Origin of coordinates is the center of die.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Revision.

DATE	REVISION	CHANGE
July 2, 2012	FN7962.0	Initial Release

Products

Intersil Corporation is a leader in the design and manufacture of high-performance analog semiconductors. The Company's products address some of the industry's fastest growing markets, such as, flat panel displays, cell phones, handheld products, and notebooks. Intersil's product families address power management and analog signal processing functions. Go to www.intersil.com/products for a complete list of Intersil product families.

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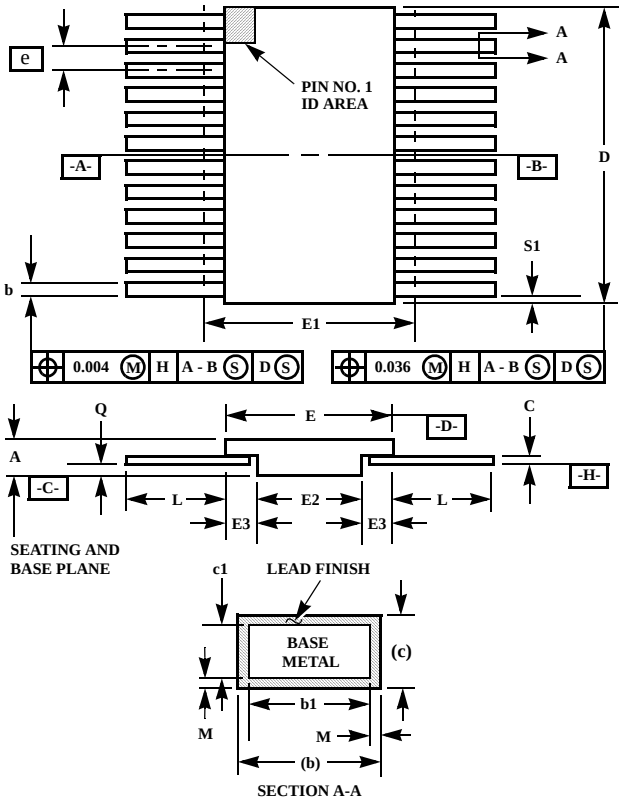
FITs are available from our website at http://rel.intersil.com/reports/search.php

Package Outline Drawing

Ceramic Metal Seal Flatpack Packages (Flatpack)



K14.A **MIL-STD-1835 CDFP3-F14 (F-2A, CONFIGURATION B)**
14 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.045	0.115	1.14	2.92	-
b	0.015	0.022	0.38	0.56	-
b1	0.015	0.019	0.38	0.48	-
c	0.004	0.009	0.10	0.23	-
c1	0.004	0.006	0.10	0.15	-
D	-	0.390	-	9.91	3
E	0.235	0.260	5.97	6.60	-
E1	-	0.290	-	7.11	3
E2	0.125	-	3.18	-	-
E3	0.030	-	0.76	-	7
e	0.050 BSC		1.27 BSC		-
k	0.008	0.015	0.20	0.38	2
L	0.270	0.370	6.86	9.40	-
Q	0.026	0.045	0.66	1.14	8
S1	0.005	-	0.13	-	6
M	-	0.0015	-	0.04	-
N	14		14		-

Rev. 0 5/18/94

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab (dimension k) may be used to identify pin one.
2. If a pin one identification mark is used in addition to a tab, the limits of dimension k do not apply.
3. This dimension allows for off-center lid, meniscus, and glass overrun.
4. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
5. N is the maximum number of terminal positions.
6. Measure dimension S1 at all four corners.
7. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
8. Dimension Q shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension Q minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.