M54970P

9-BIT SERIAL-INPUT,LATCHED DRIVER

DESCRIPTION

The M54970P is a semiconductor integrated circuit of I^2L structure containing a serial input to serial/parallel output 9-bit shift register and latch as well as a bipolar 9-bit parallel-output driver.

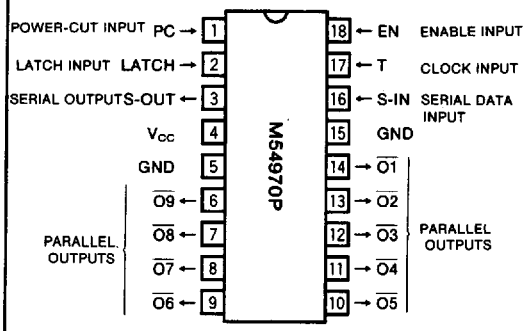
FEATURES

- Serial input to serial/parallel output
- Cascade connections possible through serial output
- Enable input for output control
- Power-cut input
- Driver : Withstand voltage ····· $BV_{CEO} \geqq 20V$
  Large drive current ····· ($I_{O(max)}$=300mA)
- Wide operating temperature range ···· T_a=−20∼+75℃

APPLICATION

Thermal printer head dot driver, Serial-to-parallel conversion, Relay and Solenoid driver

PIN CONFIGURATION (TOP VIEW)



Outline 18P4

FUNCTION

The M54970P consists of a 9bit D-type flip-flop, the output of which is connected to 9 latches.

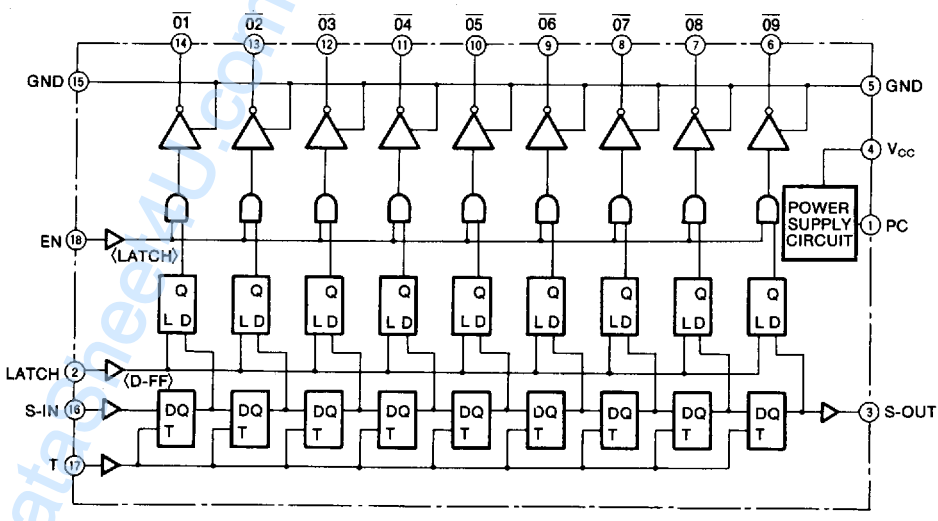
When data is applied to the serial data input (S-IN) and a clock pulse is applied to clock input (T), an "L" to "H" change of the clock will cause the data input signals to enter the internal shift registers and the data in the shift registers will be shifted in order.

Using a number of M54970P units for bit expansion in series will entail connecting serial output (S-OUT) to S-IN of the next-stage M54970P.

In parallel output, when the power-cut input and latch input are set to "H" and the output-control input (enable input EN) is "H", a clock pulse changing from "L" to "H" will cause the serial data input signal to appear at output $\overline{01}$, and the data will be shifted in order at outputs $\overline{02}$∼$\overline{09}$.

The parallel output will yield a signal that is inverted with respect to the serial data input.

BLOCK DIAGRAM



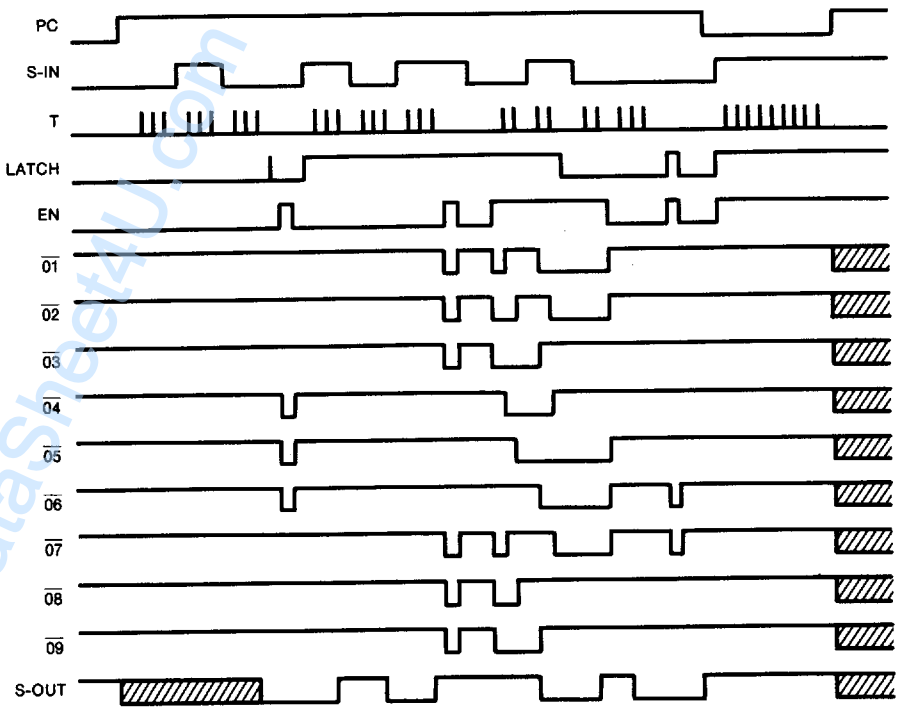
MITSUBISHI ELECTRIC

Setting the LATCH input to "L" will prevent data from entering the latch.

When the EN input is set to "L", all outputs ($\overline{01}$~$\overline{09}$) will be set to OFF. Since the internal logic state of the IC is uncertain at power-on time, set the EN input to "L" (and outputs $\overline{01}$~$\overline{09}$ will be set to OFF) until the input data is set and the internal logic state has been detrmined.

The power will be cut when the power-cut input is set to "L", and since the data of the shift registers and latches are not maintained in this state, it will be necessary to input data again in order to set the output following a change of PC input from "L" to "H".

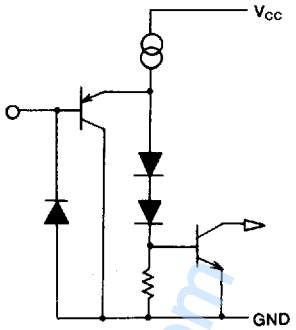
TIMING CHART



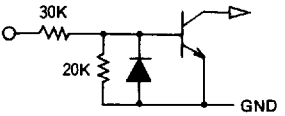
*The state of the shaded areas is uncertain.

INPUT/OUTPUT EQUIVALENT CIRCUIT SCHEMATICS

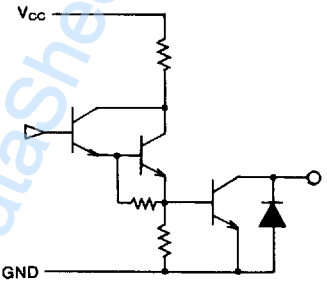
1 T, S-IN, LATCH INPUTS



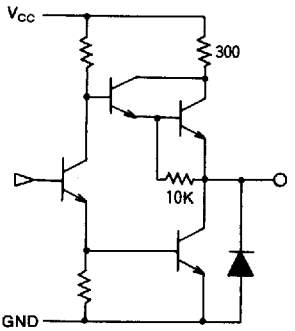
2 PC, EN INPUTS



3 $\overline{O1}$~$\overline{O9}$ OUTPUTS



4 S-OUT OUTPUT



ABSOLUTE MAXIMUM RATINGS (T_a=−20℃∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+8	V
V_I	Input voltage		−0.5∼+10	V
V_O	Output voltage	Output is OFF	−0.5∼+20	V
I_O	Output current		350	mA
P_d	Power dissipation	T_a=25℃	1.25	W
Topr	Operating temperature		−20∼+75	℃
Tstg	Storage temperature		−55∼+125	℃

RECOMMENDED OPERATING CONDITIONS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_O	Applied output voltage	When output is OFF			20	V
I_O	Output current (per circuit)	All outputs ON simultaneously Duty cycle less than 30%			300	mA

ELECTRICAL CHARACTERISTICS (T_a=+25℃, unless otherwise noted)

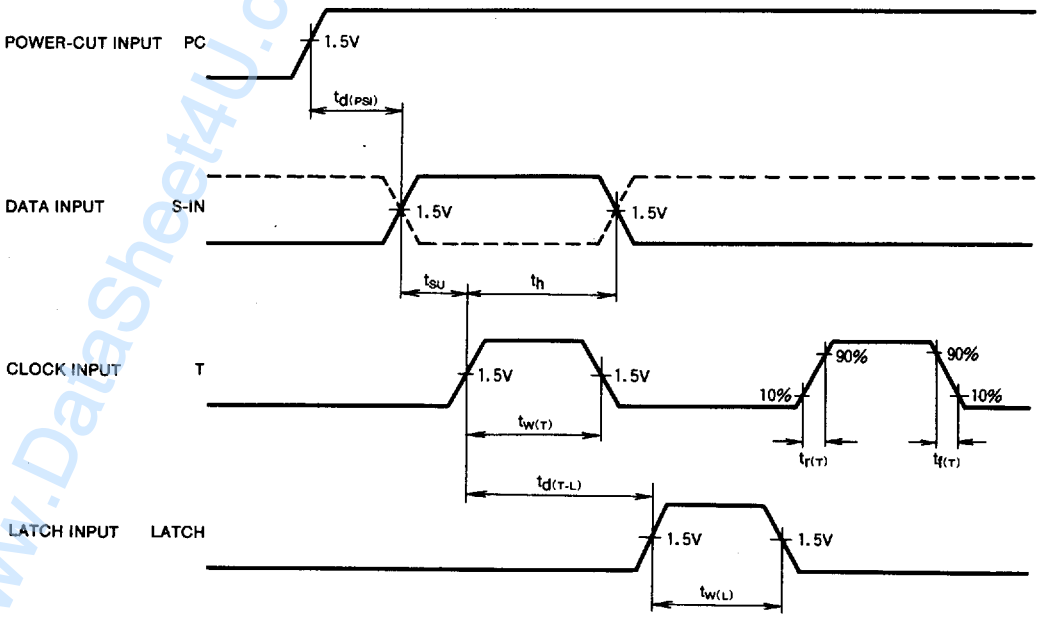
Symbol	Parameter	Test pin	Test conditions	Limits			Unit
				Min	Typ*	Max	
V_{IH}	High-level input voltage	2, 16, 17	T_a=−20∼+75℃	2.2		V_{CC}	V
V_{IL}	Low-level input voltage			0		0.8	V
V_{IH}	High-level input voltage	1, 18	T_a=−20∼+75℃	2.2		V_{CC}	V
V_{IL}	Low-level input voltage			0		0.8	V
I_{IH}	High-level input current	2, 16, 17	V_{CC}=5.5V, V_{IH}=2.4V			10	μA
I_{IL}	Low-level input current		V_{CC}=5.5V, V_{IL}=0.4V			−50	μA
I_{IH}	High-level input current	1, 18	V_{CC}=5.5V, V_{IH}=5.5V			250	μA
			V_{CC}=5.5V, V_{IH}=2.4V			100	
I_{IL}	Low-level input current		V_{CC}=5.5V, V_{IL}=0V			−10	μA
V_{OH}	High-level output voltage	3	V_{CC}=4.5V, I_{OH}=−400μA	2.4			V
V_{OL}	Low-level output voltage		V_{CC}=4.5V, I_{OL}=8mA			0.4	V
V_{OL}	Low-level output voltage	6∼14	V_{CC}=4.5V, I_{OL}=300mA			0.6	V
I_{CC1}	Supply current	4	V_{CC}=5.5V, power-cut is ON			10	μA
I_{CC2}			V_{CC}=5.5V, EN is "L"		10	15	mA
I_{CC3}			V_{CC}=5.5V, all outputs are ON		90	130	mA
$I_{O(leak)}$	Output leakage current	6∼14	V_{CC}=5.5V, V_{OH}=20V			100	μA

* : Typical values are at T_a = 25℃.

REQUIRED TIMING CONDITIONS (T_a=−20~+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
$f_{(T)}$	Clock frequency	Input duty cycle 40~60%			1	MHz
$t_{W(T)}$	Clock pulse width		0.4			μS
$t_{W(L)}$	Latch pulse width		0.4			μS
t_{SU}	Data setup time		0.2			μS
t_h	Data hold time		0.3			μS
$t_{d(T-L)}$	Clock-latch time		1			μS
$t_{r(T)}$	Clock pulse rise time				0.5	μS
$t_{f(T)}$	Clock pulse fall time				0.5	μS
$t_{d(P-SI)}$	Power-cut input → data input setting tiwe	Hold EN input at "L" when PC input is changed from "L" to "H"	2			μS

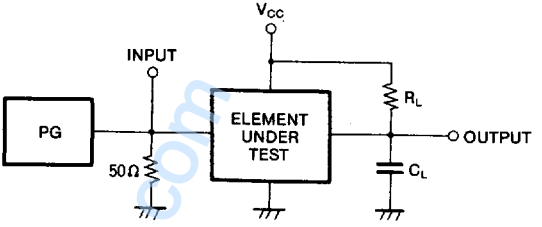
TIMING DIAGRAM



SWITCHING CHARACTERISTICS (T_a=25℃, V_{CC}=5V)

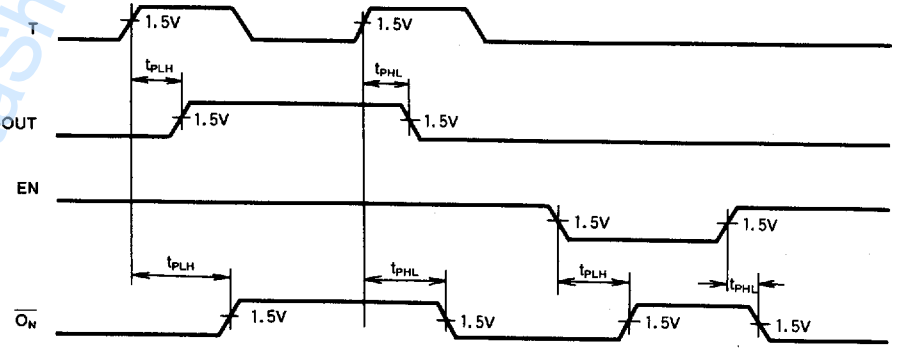
Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
t_{PLH}	Low to high-level output propagation time (Input T to output S-OUT)	V_{IH}=3V V_{IL}=0V R_L : S_{-OUT}=2KΩ R_L : $\overline{O_N}$=100Ω (N=1~9) C_L=15pF (Note 1)			0.7	μS
t_{PHL}	High to low-level output propagation time (Input T to output S-OUT)				0.8	μS
t_{PLH}	Low to high-level output propagation time (Input T to output $\overline{O_N}$)				5	μS
t_{PHL}	High to low-level output propagation time (Input T to output $\overline{O_N}$)				1	μS
t_{PLH}	Low to high-level output propagation time (Input EN to output $\overline{O_N}$)				10	μS
t_{PHL}	High to low-level output propagation time (Input EN to output $\overline{O_N}$)				1	μS

(Note 1) TEST CIRCUIT



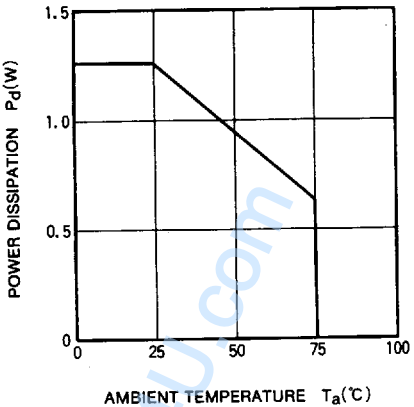
Input waveform is taken as t_r≦50ns and t_f≦50ns

TIMING DIAGRAM

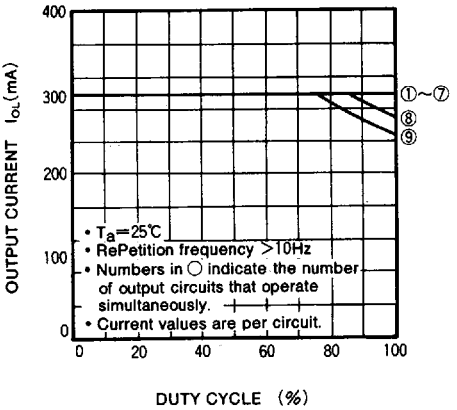


TYPICAL CHARACTERISTICS

THERMAL DERATING



DUTY CYCLE VS PERMISSIBIE OUTPUT CURRENT



DUTY CYCLE VS PERMISSIBLE OUTPUT CURRENT