

NCE N-Channel Enhancement Mode Power MOSFET

DESCRIPTION

The NCE0160S uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. This device is suitable for use in PWM, load switching and general purpose applications.

GENERAL FEATURES

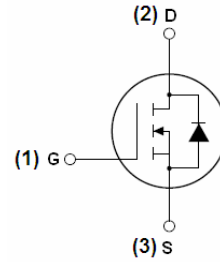
- $V_{DS} = 100V, I_D = 60A$
 $R_{DS(ON)} < 14m\Omega @ V_{GS}=10V$
- Special designed for Convertors and power controls
- High density cell design for ultra low R_{dson}
- Fully characterized Avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation

Application

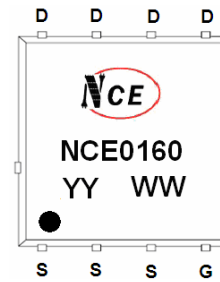
- Power switching application
- Hard Switched and High Frequency Circuits
- Uninterruptible Power Supply

100% UIS TESTED!

100% ΔV_{ds} TESTED!



Schematic diagram



Marking and pin Assignment



PowerPAK SO-8 Bottom view

Package Marking And Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
NCE0160	NCE0160S	PowerPAK SO-8	-	-	-

Absolute Maximum Ratings (TA=25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 25	V
Drain Current-Continuous	I_D	60	A
Drain Current-Continuous($T_C=70^\circ C$)	$I_D(70^\circ C)$	50	A
Pulsed Drain Current	I_{DM}	80	A
Maximum Power Dissipation	P_D	105	W
Peak diode recovery voltage	dv/dt		V/ns
Derating factor		0.84	W/°C
Single pulse avalanche energy (Note 5)	E_{AS}	550	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	°C

Thermal Characteristic

Thermal Resistance, Junction-to- Case (Note 2)	$R_{\theta jc}$	1.19	$^{\circ}\text{C/W}$
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Electrical Characteristics (TA=25 $^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	100			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=100V, V_{GS}=0V$			1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 25V, V_{DS}=0V$			± 100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	2.5	3.7	4.5	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=30A$			14	m Ω
Forward Transconductance	g_{FS}	$V_{DS}=15V, I_D=10A$		30		S
Dynamic Characteristics (Note4)						
Input Capacitance	C_{iss}	$V_{DS}=50V, V_{GS}=0V,$ $F=1.0\text{MHz}$		2850		PF
Output Capacitance	C_{oss}			220		PF
Reverse Transfer Capacitance	C_{rss}			90		PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=30V, I_D=5A, R_L=10\Omega$ $V_{GS}=10V, R_G=1\Omega$		17		nS
Turn-on Rise Time	t_r			10		nS
Turn-Off Delay Time	$t_{d(off)}$			26		nS
Turn-Off Fall Time	t_f			10		nS
Total Gate Charge	Q_g	$V_{DS}=50V, I_D=10A,$ $V_{GS}=10V$		47		nC
Gate-Source Charge	Q_{gs}			13		nC
Gate-Drain Charge	Q_{gd}			12.5		nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	$V_{GS}=0V, I_S=4A$			1.2	V
Diode Forward Current (Note 2)	I_S				60	A
Reverse Recovery Time	t_{rr}	$T_J = 25^{\circ}\text{C}, I_F = 10A$ $di/dt = 100A/\mu s(\text{Note3})$			60	nS
Reverse Recovery Charge	Q_{rr}				200	nC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

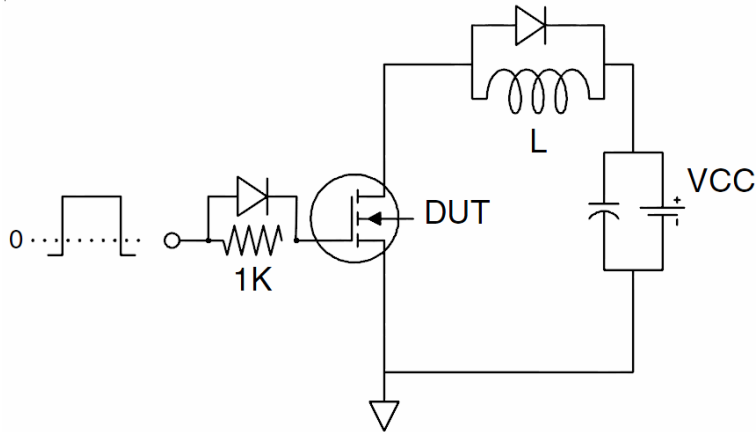
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. EAS condition: $T_J=25^{\circ}\text{C}, V_{DD}=50V, V_G=10V, L=0.5\text{mH}, R_g=25\Omega$

Test circuit

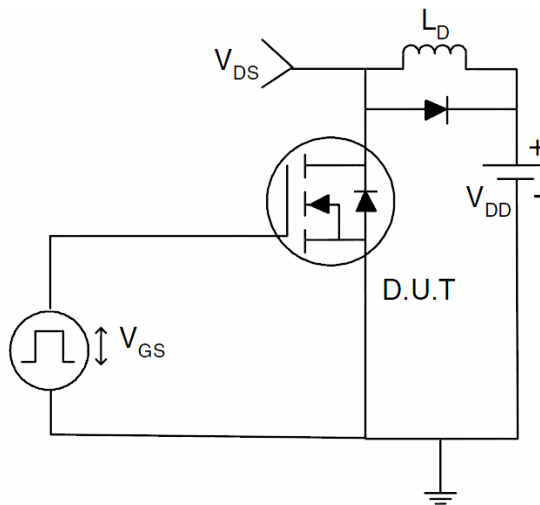
1) E_{AS} test Circuits



2) Gate charge test Circuit:



3) Switch Time Test Circuit:



TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS (curves)

Figure1. Safe operating area

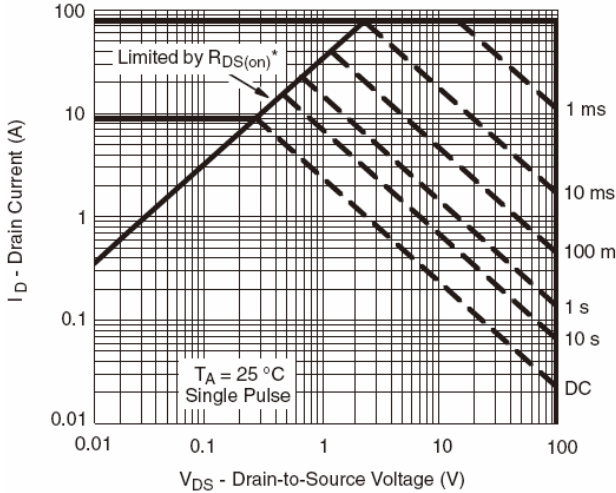


Figure2. Source-Drain Diode Forward Voltage

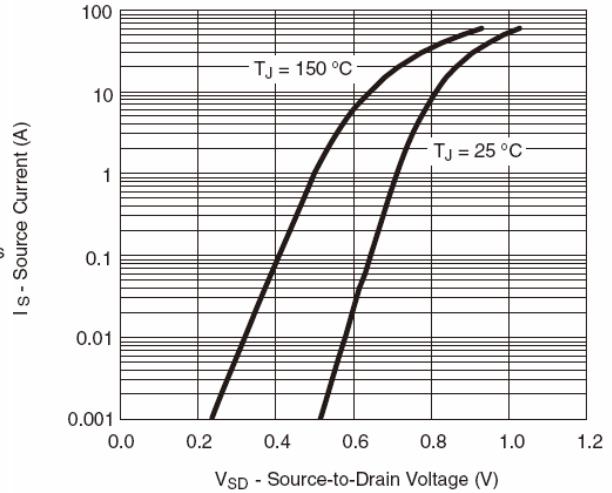


Figure3. Output characteristics

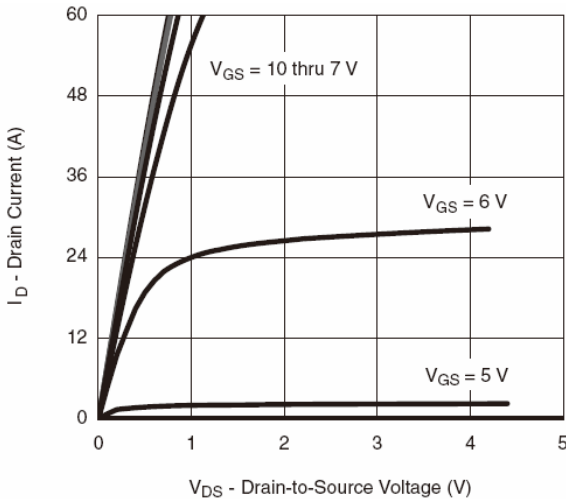


Figure4. Transfer characteristics

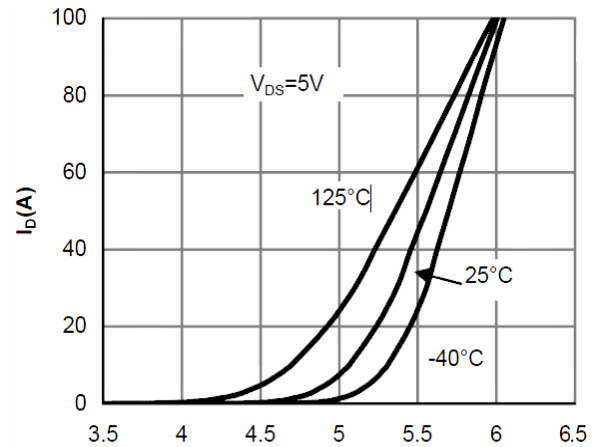


Figure5. Static drain-source on resistance

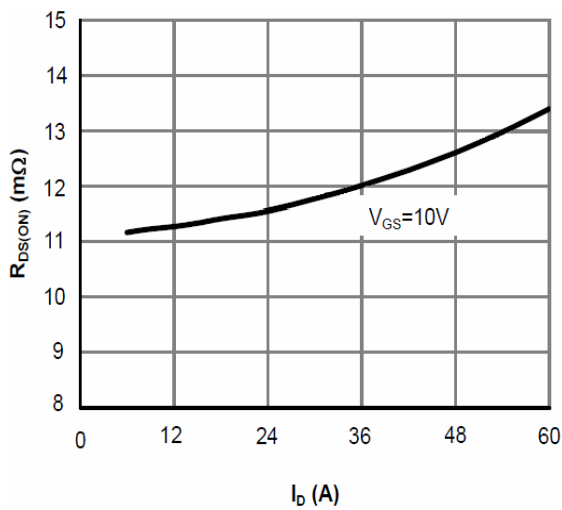


Figure6. $R_{DS(ON)}$ vs Junction Temperature

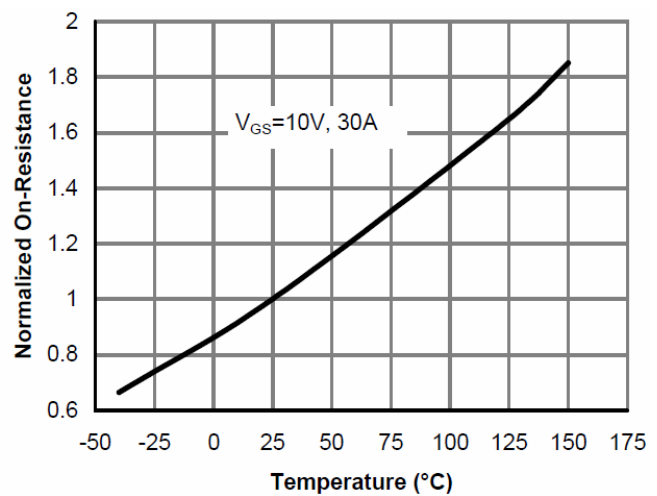


Figure7. BV_{DSS} vs Junction Temperature

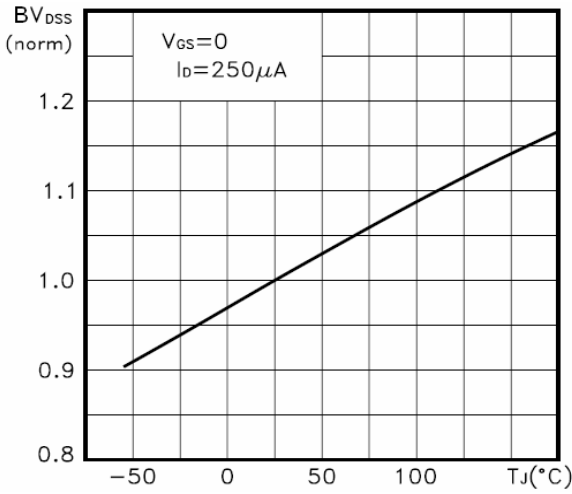


Figure8. $V_{GS(th)}$ vs Junction Temperature

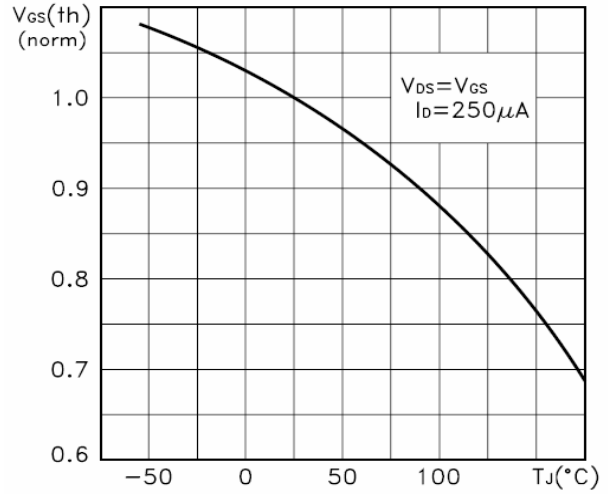


Figure9. Gate charge waveforms

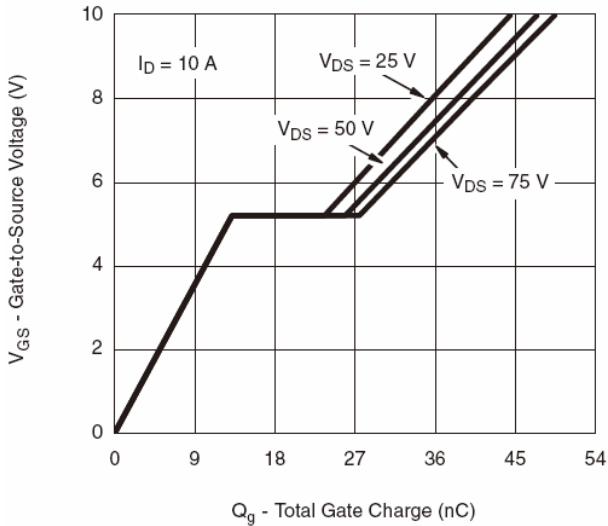


Figure10. Capacitance

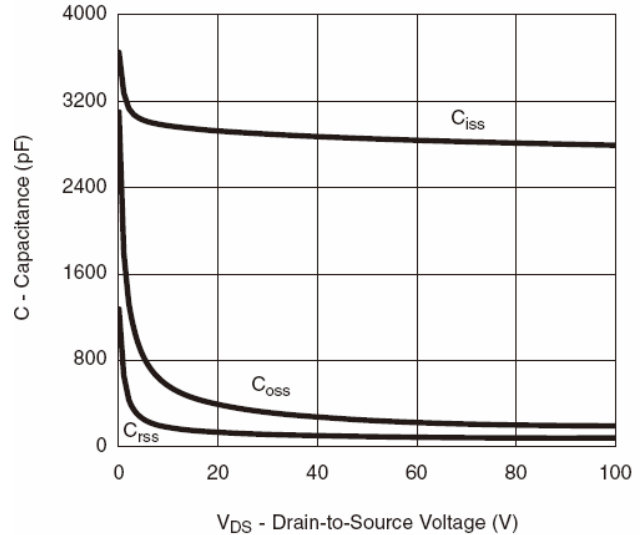
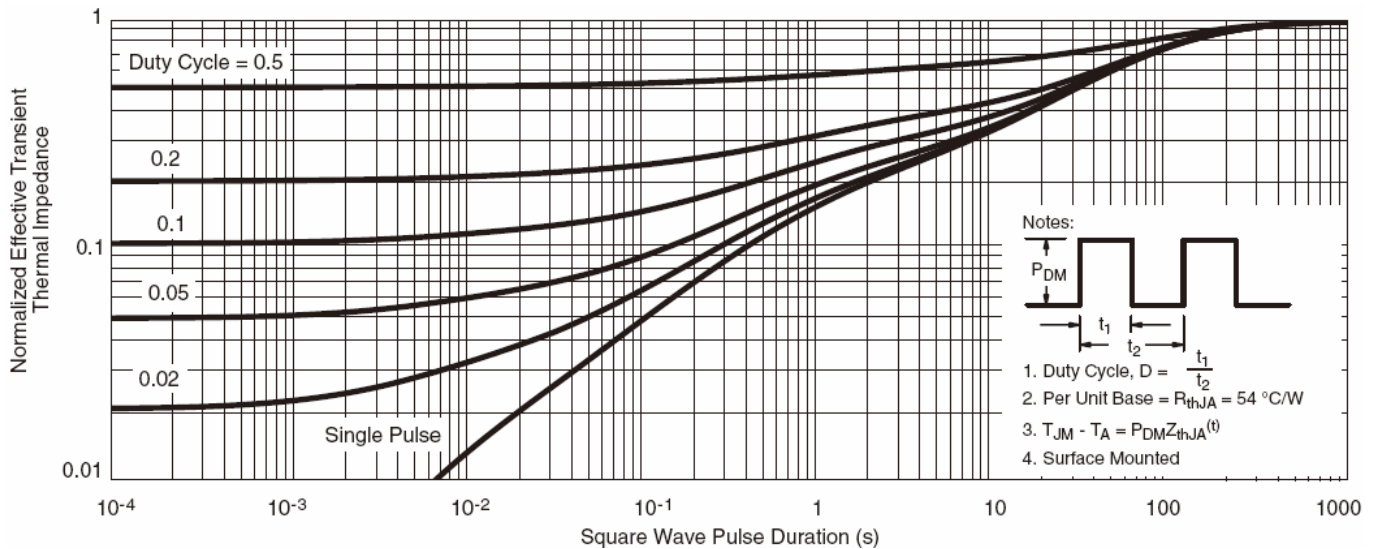
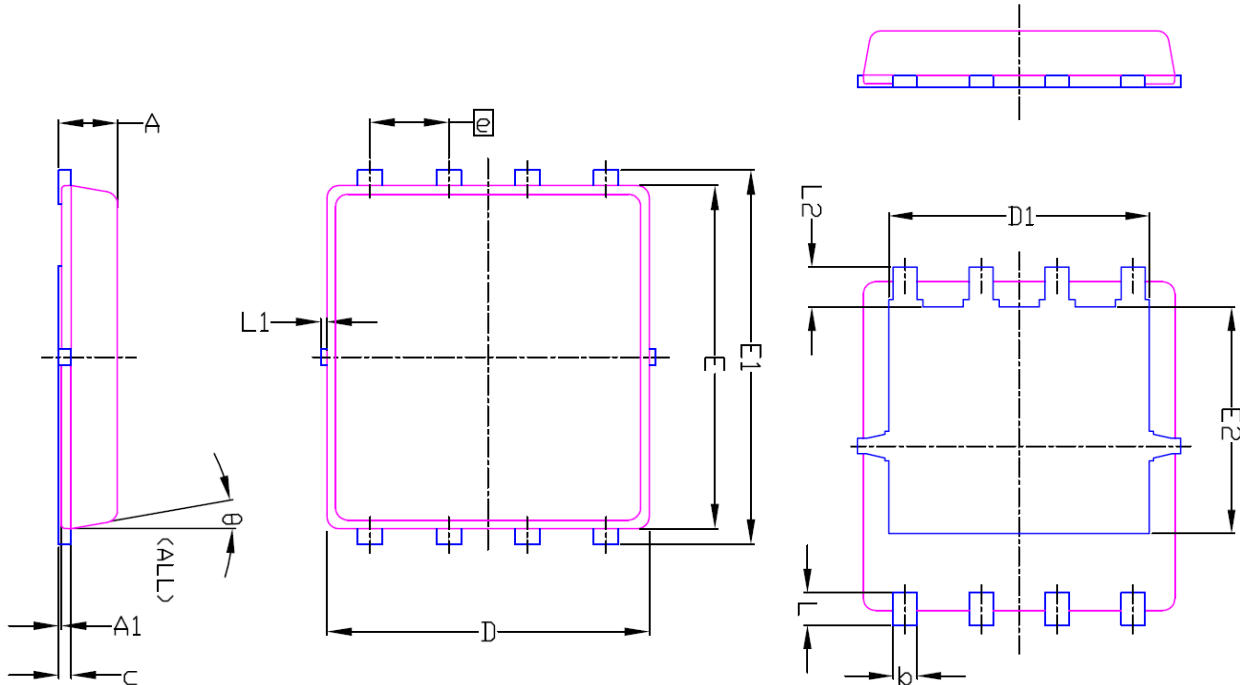


Figure11. Normalized Maximum Transient Thermal Impedance



PowerPAK SO-8 PACKAGE INFORMATION



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.85	0.95	1.00	0.033	0.037	0.039
A1	0.00	---	0.05	0.000	---	0.002
b	0.30	0.40	0.50	0.012	0.016	0.020
c	0.15	0.20	0.25	0.006	0.008	0.010
D	5.20 BSC			0.205 BSC		
D1	4.35 BSC			0.171 BSC		
E	5.55 BSC			0.219 BSC		
E1	6.05 BSC			0.238 BSC		
E2	3.82 BSC			0.150 BSC		
e	1.27 BSC			0.050 BSC		
L	0.45	0.55	0.65	0.018	0.022	0.026
L1	0	---	0.15	0	---	0.006
L2	0.68 REF			0.027 REF		
θ	0°	---	10°	0°	---	10°

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