Analog Power AM4934N

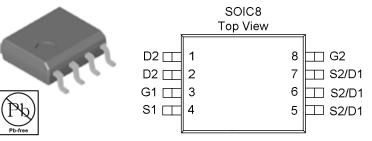
Dual N-Channel 30-V (D-S) MOSFET

These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $r_{DS(on)}$ and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordletelephones.

•	Low r _{DS(on)} provides higher efficiency
	extends battery life

- Low thermal impedance copper leadfr SOIC-8 saves board space
- Fast switching speed
- High performance trench technology

PRODUCT SUMMARY					
FET#	$r_{DS(on)} m(\Omega)$ $I_D (A)$				
1	$19 @ V_{GS} = 4.5V$	8.4			
1	$15 @ V_{GS} = 10V$	9.5			
2	$23 @ V_{GS} = 4.5V$	7.7			
2	$15 @ V_{GS} = 10V$	9.5			



	COMPLIANT HALOGEN FREE
SSOLUTE MAXIMUM RATINGS (T _a	= 25 °C U
Danamatan	·

ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C UNLESS OTHERWISE NOTED)						
Parameter		Symbol	FET#1	FET#1	Units	
Drain-Source Voltage	V_{DS}	30	30	V		
Gate-Source Voltage	V_{GS}	20	20	V		
Continue David Consult ^a	T _A =25°C	ĭ	9.5	9.5		
Continuous Drain Current ^a	$\begin{array}{c} T_{A}=25^{\circ}C \\ T_{A}=70^{\circ}C \end{array} I_{D}$		7.7	7.7	A	
Pulsed Drain Current ^b		I_{DM}	40	40		
Continuous Source Current (Diode Conduction) ^a		I_S	4.5	4.5	A	
D	$T_A=25^{\circ}C$	D	2.1	2.1	W	
Power Dissipation ^a	$T_A=25^{\circ}C$ $T_A=70^{\circ}C$	l D	1.3	1.3	VV	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150		°C	

THERMAL RESISTANCE RATINGS						
Parameter	Symbol	Maximum	Units			
M	t <= 10 sec	D	62.5	°C/W		
Maximum Junction-to-Ambient ^a	Steady-State	$ m R_{\theta JA}$	110	°C/W		

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Notes

- a. Surface Mounted on 1" x 1" FR4 Board.
- b. Pulse width limited by maximum junction temperature

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SPECIFICATIONS (T _A = 25°C UNLESS OTHERWISE NOTED)							
Parameter	Symbol	Test Conditions	FET#	Lim Min	its Typ	Max	Unit
Static							
Gate-Threshold Voltage	$V_{GS(th)}$	VGS = VDS, $ID = 250 uA$	1	1			V
Gate-Tiffeshold Voltage	▼ GS(th)	VGS = VDS, $ID = 250 uA$	2	1			•
Gate-Body Leakage	I_{GSS}	$V_{GS} = 20 \text{ V}, V_{DS} = 0 \text{ V}$	1			±100	nA
Oute Body Leakage	-055	$V_{GS} = 20 \text{ V}, V_{DS} = 0 \text{ V}$	2			±100	112 1
Zero Gate Voltage Drain Current	$I_{ m DSS}$	$V_{DS} = 24 \text{ V}, V_{GS} = 0 \text{ V}$	1			1	uA
Zero Gate Voltage Drain Current	DSS	$V_{DS} = 24 \text{ V}, V_{GS} = 0 \text{ V}$	2			1	
O C A	ī	$V_{DS} = 5 \text{ V}, V_{GS} = 10 \text{ V}$	1	40			Α
On-State Drain Current ^A	$I_{D(on)}$	$V_{DS} = -5 \text{ V}, V_{GS} = -10 \text{ V}$	2	40			Α
		VGS = 10 V, ID = 2 A	1			15	mΩ
Drain-Source On-Resistance ^A	r	VGS = 4.5 V, ID = 2 A	1			19	
Diani-Source On-Resistance	r _{DS(on)}	VGS = 10 V, ID = 2 A	2			15	
		VGS = 4.5 V, ID = 2 A				23	
Diode Forward Voltage	V_{SD}	$I_S = 2A$	1		0.8		V
210 de 1 of ward y ortage	▼ SD	$I_S = -2A$	2		0.8		·
Forward Tranconductance ^A	g.	$V_{DS} = 15 \text{ V}, I_{D} = 2 \text{ A}$	1		64		S
Polward Tranconductance	g_{fs}	$V_{DS} = 15 \text{ V}, I_{D} = 2 \text{ A}$	2		64		3
Dynamic							
Total Gate Charge	Q_{g}		1		3		
	₹g		2 1		3		
Gate-Source Charge	Q_{gs}	V_{DS} =15V, V_{GS} =4.5V, I_{D} =2A	2		1		nC
Cata Drain Changa	0		1		1		
Gate-Drain Charge	Q_{gd}		2		1		
Turn-On Delay Time	$t_{d(on)}$	N-Chaneel	1		5		
-	u(on)	V_{DD} =15V, VGS=10V,	2		5		
Rise Time	t_r	ID=1A , R_{GEN} =25 Ω ,	2		5		<i>a</i>
Turn-Off Delay Time	f	P-Channel	1		16		nS
Tuni-On Delay Tille	$t_{d(off)}$	VDD=-15V, VGS=-10V,	2		16		.
Fall-Time	t_{f}	ID=-1A RGEN=15 Ω	2		7		
NT-4					/		

Notes

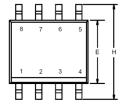
- a. Pulse test: $PW \le 300$ us duty cycle $\le 2\%$.
- b. Guaranteed by design, not subject to production testing.

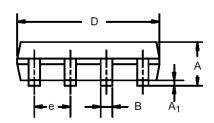
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Package Information

SO-8: 8LEAD





	MILLIMETERS		INC	HES	
Dim	Min	Max	Min	Max	
Α	1.35	1.75	0.053	0.069	
A ₁	0.10	0.20	0.004	0.008	
В	0.35	0.51	0.014	0.020	
С	0.19	0.25	0.0075	0.010	
D	4.80	5.00	0.189	0.196	
E	3.80	4.00	0.150	0.157	
е	1.27	BSC	0.050 BSC		
Н	5.80	6.20	0.228	0.244	
h	0.25	0.50	0.010	0.020	
L	0.50	0.93	0.020	0.037	
q	0°	8°	0°	8°	

