

### Description

The EN2360QI is a Power System on a Chip (PowerSoC) DC-DC converter. It integrates MOSFET switches, small-signal control circuits, compensation and an integrated inductor in an advanced 8x11x3mm QFN module. It offers high efficiency, excellent line and load regulation over temperature. The EN2360QI operates over a wide input voltage range and is specifically designed to meet the precise voltage and fast transient requirements of high-performance products. The EN2360QI features frequency synchronization to an external clock, power OK output voltage monitor, programmable soft-start along with thermal and over current protection. The device's advanced circuit design, ultra high switching frequency and proprietary integrated inductor technology delivers high-quality, ultra compact, non-isolated DC-DC conversion.

The Enpirion solution significantly helps in system design and productivity by offering greatly simplified board design, layout and manufacturing requirements. In addition, overall system level reliability is improved given the small number of components required with the Enpirion solution.

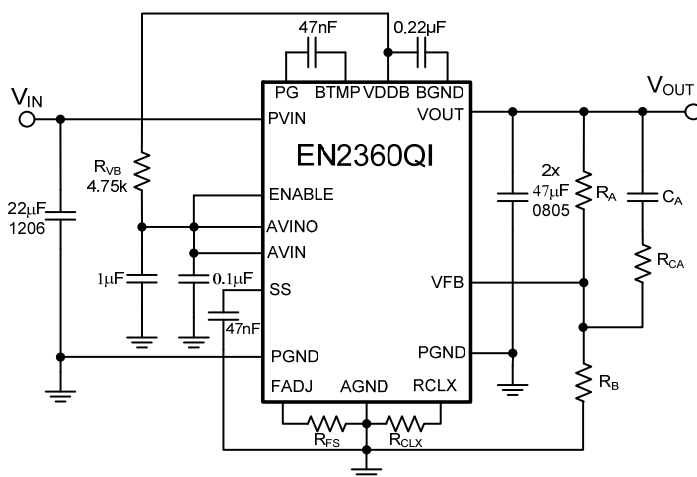
All Enpirion products are RoHS compliant and lead-free manufacturing environment compatible.

### Features

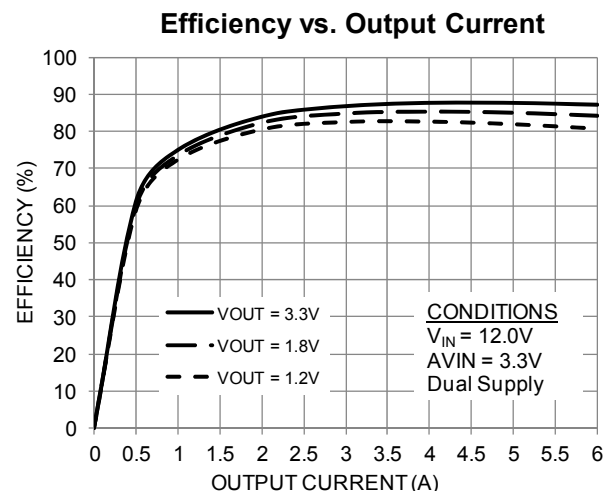
- Integrated Inductor, MOSFETs, Controller
- Wide Input Voltage Range: 4.5V – 14V
- Total Solution Size Estimate: 185mm<sup>2</sup>
- Frequency Synchronization (External Clock)
- 2% V<sub>OUT</sub> Accuracy (Over Line/Load/Temperature)
- Output Enable Pin and Power OK signal
- Programmable Soft-Start Time
- Can be Pin Compatible with the EN2340QI (4A)
- Under Voltage Lockout Protection (UVLO)
- Programmable Over Current Protection
- Thermal Shutdown and Short Circuit Protection
- RoHS Compliant, MSL Level 3, 260°C Reflow

### Applications

- Space Constrained Applications
- Distributed Power Architectures
- Output Voltage Ripple Sensitive Applications
- Beat Frequency Sensitive Applications
- Servers, Embedded Computing Systems, LAN/SAN Adapter Cards, RAID Storage Systems, Industrial Automation, Test and Measurement, and Telecommunications



**Figure 1.** Simplified Applications Circuit (Footprint Optimized)



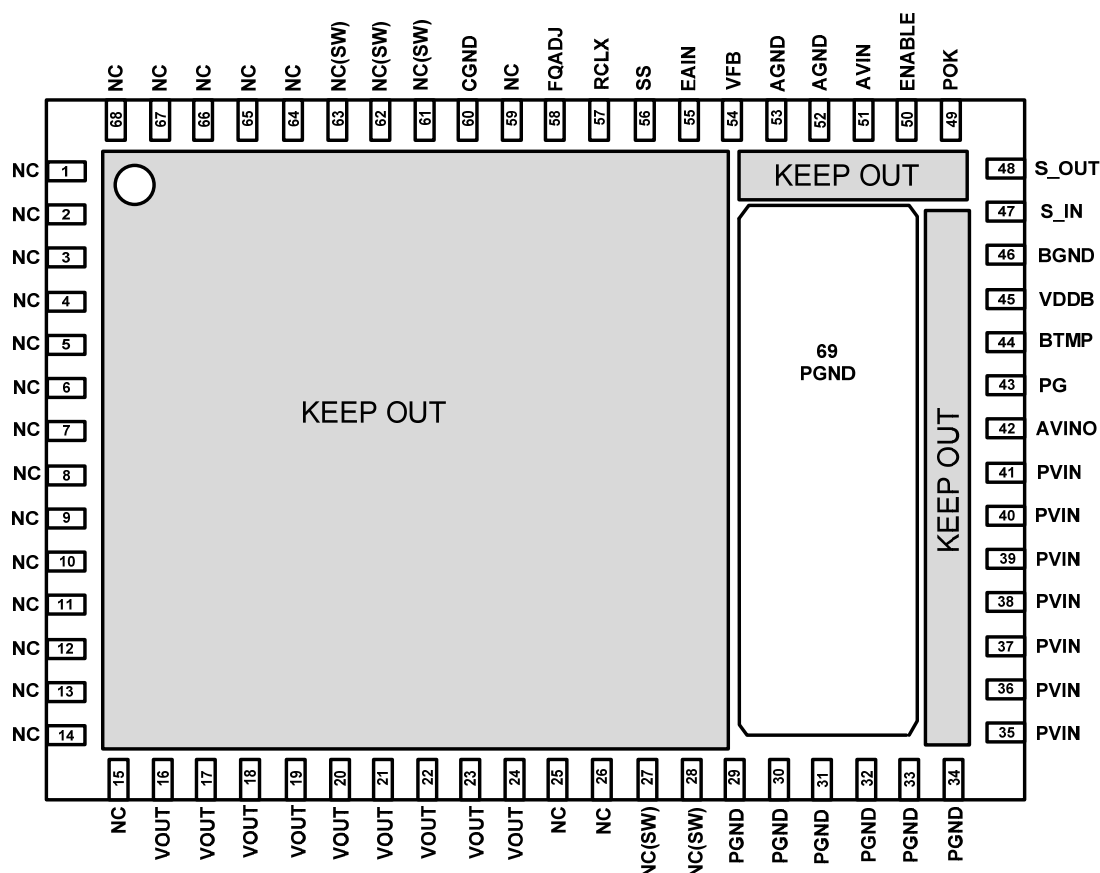
**Figure 2.** Highest Efficiency in Smallest Solution Size

## Ordering Information

Part Number	Package Markings	Temp Rating (°C)	Package Description
EN2360QI	EN2360QI	-40 to +85	68-pin (8mm x 11mm x 3mm) QFN T&R
EN2360QI-E	EN2360QI		QFN Evaluation Board

Packing and Marking Information: <http://www.enpirion.com/resource-center-packing-and-marking-information.htm>

## Pin Assignments (Top View)



**Figure 3:** Pin Out Diagram (Top View)

**NOTE A:** NC pins are not to be electrically connected to each other or to any external signal, ground, or voltage. However, they must be soldered to the PCB. Failure to follow this guideline may result in part malfunction or damage.

**NOTE B:** Shaded area highlights exposed metal below the package that is not to be mechanically or electrically connected to the PCB. Refer to Figure 12 for details.

**NOTE C:** White 'dot' on top left is pin 1 indicator on top of the device package.

## Pin Description

**I/O Legend:** P=Power G=Ground NC=No Connect I=Input O=Output I/O=Input/Output

PIN	NAME	I/O	FUNCTION
1-15, 25-26, 59, 64- 68	NC	NC	NO CONNECT – These pins may be internally connected. Do not connect them to each other or to any other electrical signal. Failure to follow this guideline may result in device damage.

PIN	NAME	I/O	FUNCTION
16-24	VOUT	O	Regulated converter output. Connect these pins to the load and place output capacitor between these pins and PGND pins 29-31.
27-28, 61-63	NC(SW)	NC	NO CONNECT – These pins are internally connected to the common switching node of the internal MOSFETs. They are not to be electrically connected to any external signal, ground, or voltage. Failure to follow this guideline may result in damage to the device.
29-34	PGND	G	Input/Output power ground. Connect these pins to the ground electrode of the input and output filter capacitors. See VOUT and PVIN pin descriptions for more details.
35-41	PVIN	P	Input power supply. Connect to input power supply. Decouple with input capacitor to PGND pins 32-34.
42	AVINO	O	Internal 3.3V linear regulator output. Connect this pin to AVIN (Pin 51) for applications where operation from a single input voltage (PVIN) is required. If AVINO is being used, place a 1 $\mu$ F, X5R, capacitor between AVINO and AGND as close as possible to AVINO.
43	PG	I/O	Place a 47nF, X5R, capacitor between this pin and BTMP.
44	BTMP	I/O	See pin 43 description.
45	VDDDB	O	Internal regulated voltage used for the internal control circuitry. Place a 0.22 $\mu$ F, X5R, capacitor between this pin and BGND.
46	BGND	G	See pin 45 description.
47	S_IN	I	Digital Input. This pin accepts either an input clock to phase lock the internal switching frequency or a S_OUT signal from another EN2360QI. Leave this pin floating if not used.
48	S_OUT	O	Digital Output. PWM signal is output on this pin. Leave this pin floating if not used.
49	POK	O	Power OK is an open drain transistor (pulled up to AVIN or similar voltage) used for power system state indication. POK is logic high when VOUT is within -10% of VOUT nominal. Leave this pin floating if not used.
50	ENABLE	I	Input Enable. Applying a logic high to this pin enables the output and initiates a soft-start. Applying a logic Low disables the output. Do not leave floating.
51	AVIN	P	3.3V Input power supply for the controller. Place a 0.1 $\mu$ F, X5R, capacitor between AVIN and AGND.
52, 53	AGND	G	Analog Ground. This is the ground return for the controller. All AGND pins need to be connected to a quiet ground.
54	VFB	I/O	External Feedback Input. The feedback loop is closed through this pin. A voltage divider at VOUT is used to set the output voltage. The mid-point of the divider is connected to VFB. A phase lead capacitor from this pin to VOUT is also required to stabilize the loop.
55	EAIN	O	Optional Error Amplifier Input. Allows for customization of the control loop for performance optimization. Leave this pin floating if not used.
56	SS	I/O	Soft-start node. The soft-start capacitor is connected between this pin and AGND. The value of this capacitor determines the startup time. See Soft-Start Operation in the Functional Description section for details.
57	RCLX	I/O	Programmable over-current protection. Placement of a resistor on this pin will adjust the over-current protection threshold. See Table 2 for the recommended RCLX Value to set OCP at the nominal value specified in the Electrical Characteristics table. No current limit protection when this pin is left floating.
58	FADJ	I/O	Adding a resistor ( $R_{FS}$ ) to this pin will adjust the switching frequency of the EN2360QI. See Table 1 for suggested resistor values on $R_{FS}$ for various PVIN/VOUT combinations to maximize efficiency. Do not leave this pin floating.
60	CGND		Test pin. For Enpirion Internal Use Only. Connect to GND plane at all times.
69	PGND		Not a perimeter pin. Device thermal pad to be connected to the system GND plane for heat-sinking purposes.

## Absolute Maximum Ratings

**CAUTION:** Absolute Maximum ratings are stress ratings only. Functional operation beyond the recommended operating conditions is not implied. Stress beyond the absolute maximum ratings may impair device life. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

PARAMETER	SYMBOL	MIN	MAX	UNITS
Voltages on – PVIN, VOUT	$V_{IN}$	-0.5	15	V
Pin Voltages – AVINO, AVIN, ENABLE, POK, S_IN, S_OUT, M/S		2.5	6.0	V
Pin Voltages – VFB, SS, EAIN, RCLX, FADJ		-0.5	2.75	V
PVIN Slew Rate		0.3	3	V/ms
Storage Temperature Range	$T_{STG}$	-65	150	°C
Maximum Operating Junction Temperature	$T_{J-ABS Max}$		150	°C
Reflow Temp, 10 Sec, MSL3 JEDEC J-STD-020A			260	°C
ESD Rating - all pins (based on Human Body Model)			2000	V
ESD Rating (based on CDM)			500	V

## Recommended Operating Conditions

PARAMETER	SYMBOL	MIN	MAX	UNITS
PVIN: Input Voltage Range	PVIN	4.5	14.0	V
AVIN: Controller Supply Voltage	AVIN	2.5	5.5	V
Output Voltage Range (Note 1)	$V_{OUT}$	0.6	5.0	V
Output Current	$I_{OUT}$		6.0	A
Operating Junction Temperature	$T_{J-OP}$	- 40	125	°C
Operating Ambient Temperature	$T_{AMB}$	- 40	85	°C

## Thermal Characteristics

PARAMETER	SYMBOL	TYP	UNITS
Thermal Resistance: Junction to Ambient (0 LFM) (Note 2)	$\theta_{JA}$	16	°C/W
Thermal Resistance: Junction to Case (0 LFM)	$\theta_{JC}$	2	°C/W
Thermal Shutdown	$T_{SD}$	160	°C
Thermal Shutdown Hysteresis	$T_{SDH}$	35	°C

**Note 1:** RCLX resistor value may need to be raised for  $V_{OUT} > V_{IN} - 2.5V$  to increase current limit threshold. Contact [techsupport@enpirion.com](mailto:techsupport@enpirion.com) for details.

**Note 2:** Based on 2oz. external copper layers and proper thermal design in line with EIJ/JEDEC JESD51-7 standard for high thermal conductivity boards.

## Electrical Characteristics

NOTE:  $V_{IN}=12V$ , Minimum and Maximum values are over operating ambient temperature range unless otherwise noted. Typical values are at  $T_A = 25^\circ C$ .

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Operating Input Voltage	PVIN		4.5		14.0	V
Controller Input Voltage	AVIN		2.5		5.5	V
PVIN Under Voltage Lock-out	UVLO <sub>PVIN</sub>	Voltage above which UVLO is not asserted		2		V
AVIN Under Voltage Lock-out rising	AVIN <sub>UVLOR</sub>	Voltage above which UVLO is not asserted		2.3		V
AVIN Under Voltage Lock-out falling	AVIN <sub>OVLOF</sub>	Voltage below which UVLO is asserted		2.1		V
AVIN Pin Input Current	I <sub>AVIN</sub>			9		mA
Internal Linear Regulator Output Voltage	AVINO			3.3		V
Shut-Down Supply Current	IPVINS	PVIN=12V, AVIN=3.3, ENABLE=0V		300		$\mu A$
	I <sub>AVINS</sub>	PVIN=12V, AVIN=3.3, ENABLE=0V		50		$\mu A$
Feedback Pin Voltage	V <sub>FB</sub>	Feedback node voltage at: $V_{IN} = 12V$ , ILOAD = 0, $T_A = 25^\circ C$	0.594	0.60	0.606	V
Feedback Pin Voltage	V <sub>FB</sub>	Feedback node voltage at: $4.5V \leq V_{IN} \leq 14V$ $0A \leq ILOAD \leq 6A$ , $T_A = -40$ to $85^\circ C$	0.588	0.60	0.612	V
Feedback pin Input Leakage Current	I <sub>FB</sub>	VFB pin input leakage current (Note 3)	-5		5	nA
V <sub>OUT</sub> Rise Time	t <sub>RISE</sub>	C <sub>SS</sub> = 47nF (Note 3, Note 4 and Note 5)	1.96	2.8	3.64	ms
Soft Start Capacitor Range	C <sub>SS_RANGE</sub>			47		nF
Maximum Continuous Output Current	I <sub>OUT_CONT</sub>		0		6	A
Over Current Trip Level	I <sub>OCF</sub>	Reference Table 2		9		A
ENABLE Logic High	V <sub>ENABLE_HIGH</sub>	$4.5V \leq V_{IN} \leq 14V$ ;	1.8		AV <sub>IN</sub>	V
ENABLE Logic Low	V <sub>ENABLE_LOW</sub>	$4.5V \leq V_{IN} \leq 14V$ ;	0		0.6	V
ENABLE Lockout Time	T <sub>ENLOCKOUT</sub>			8		ms
ENABLE pin Input Current	I <sub>ENABLE</sub>	180k $\Omega$ pull down (Note 3)		4		$\mu A$
Switching Frequency	F <sub>SW</sub>	RFADJ =3k $\Omega$		1.0		MHz
External SYNC Clock Frequency Lock Range	F <sub>PLL_LOCK</sub>	Range of SYNC clock frequency	0.8		1.6	MHz
S_IN Threshold – Low	V <sub>S_IN_LO</sub>	S_IN Clock Logic Low Level (Note 3)			0.8	V
S_IN Threshold – High	V <sub>S_IN_HI</sub>	S_IN Clock Logic High Level (Note 3)	1.8		2.5	V
S_OUT Threshold – Low	V <sub>S_OUT_LO</sub>	S_OUT Clock Logic Low Level (Note 3)			0.8	V
S_OUT Threshold – High	V <sub>S_OUT_HI</sub>	S_OUT Clock Logic High Level (Note 3)	1.8		2.5	V

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
POK Lower Threshold	$POK_{LT}$	Percentage of Nominal Output Voltage for POK to be Low		90		%
POK Output low Voltage	$V_{POKL}$	With 4mA Current Sink into POK			0.4	V
POK Output Hi Voltage	$V_{POKH}$	PVIN range: $4.5V \leq V_{IN} \leq 14V$			AVIN	V
POK pin $V_{OH}$ leakage current	$I_{POKL}$	POK High (Note 3)			1	$\mu A$
M/S Pin Logic Low	$V_{T-LOW}$	Tie Pin to GND			0.8V	V
M/S Pin Logic High	$V_{T-HIGH}$	Pull up to AVIN Through an External Resistor REXT	1.8V			V
M/S Pin Input Current	$I_{M/S}$	$V_{IN} = 5.0V$ , $R_{EXT} = 24.9k\Omega$		100		$\mu A$

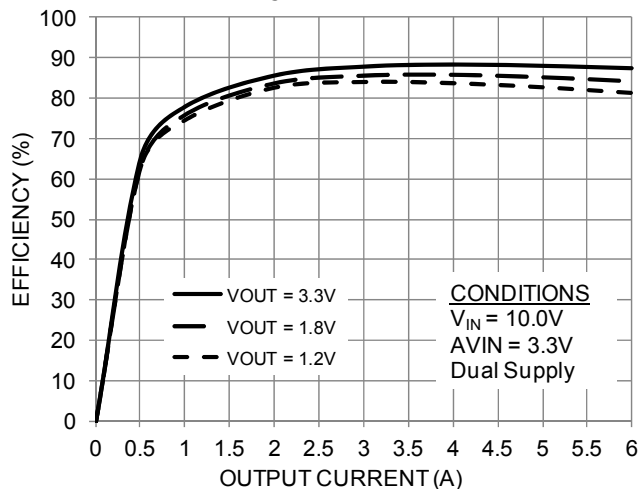
**Note 3:** Parameter not production tested but is guaranteed by design.

**Note 4:** Rise time calculation begins when  $AVIN > V_{UVLO}$  and  $ENABLE = HIGH$ .

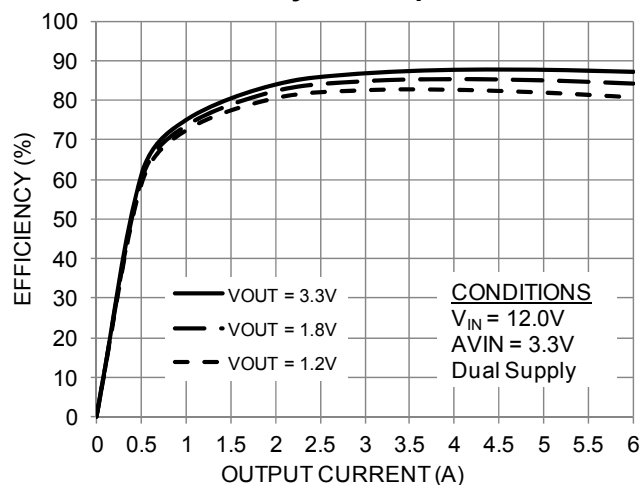
**Note 5:**  $V_{OUT}$  Rise Time Accuracy does not include soft-start capacitor tolerance.

Typical Performance Curves

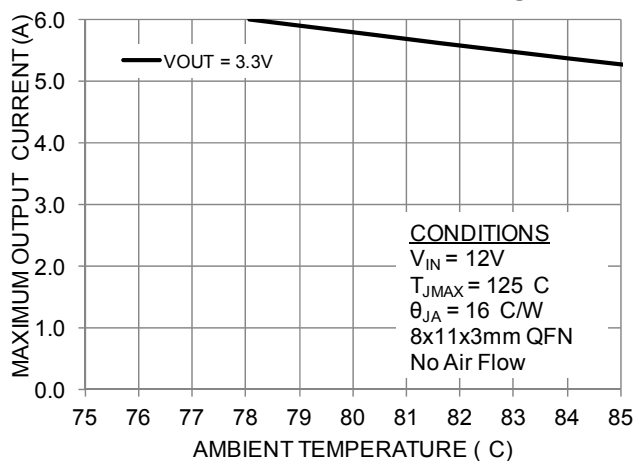
Efficiency vs. Output Current



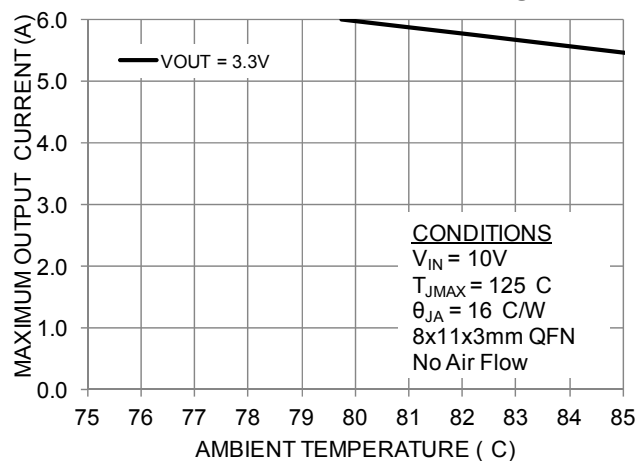
Efficiency vs. Output Current



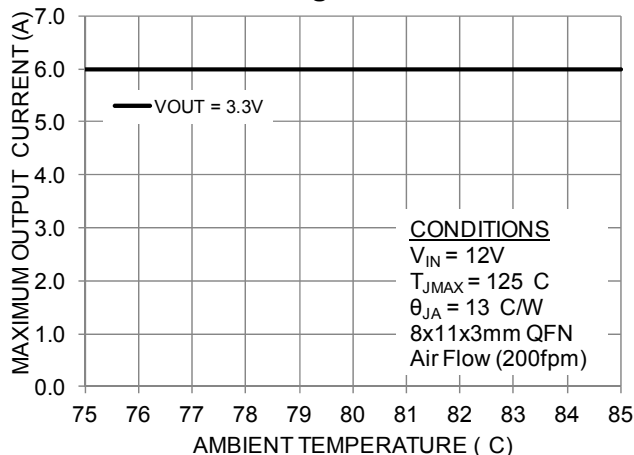
Output Current De-rating



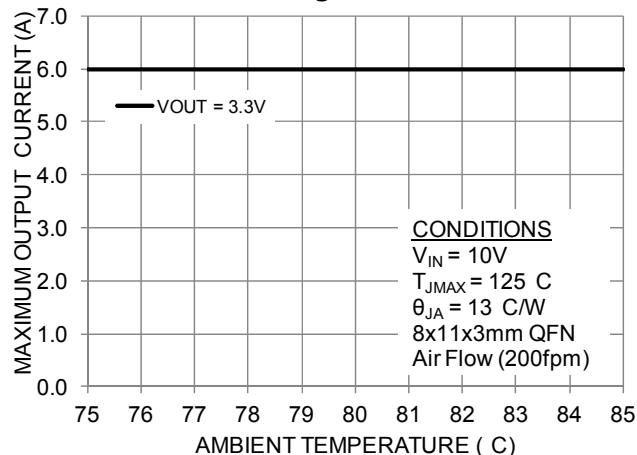
Output Current De-rating



No De-rating with Air Flow

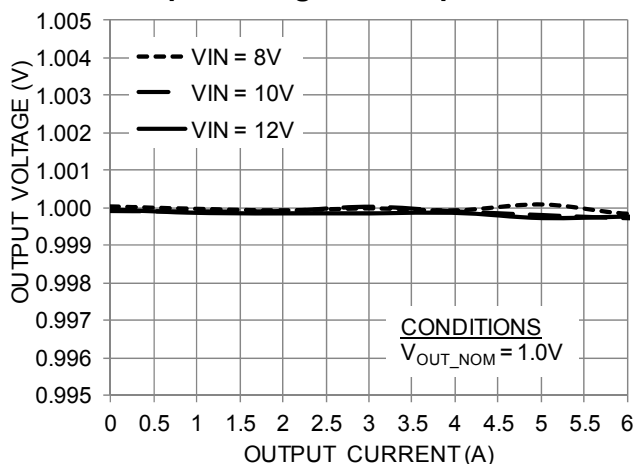


No De-rating with Air Flow

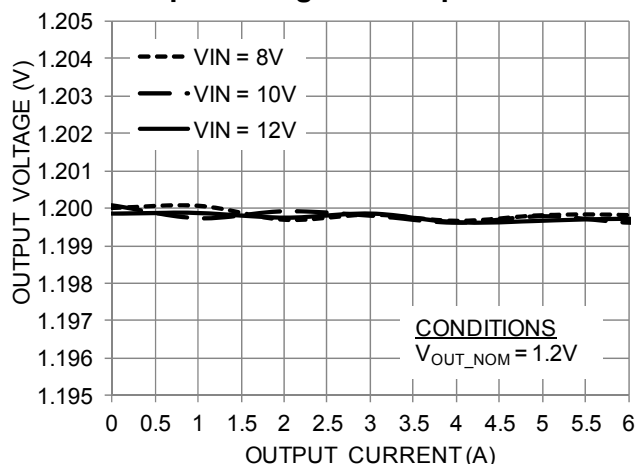


# Typical Performance Curves

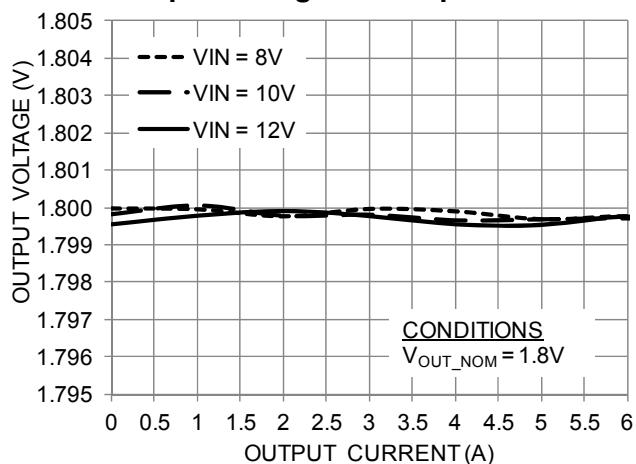
**Output Voltage vs. Output Current**



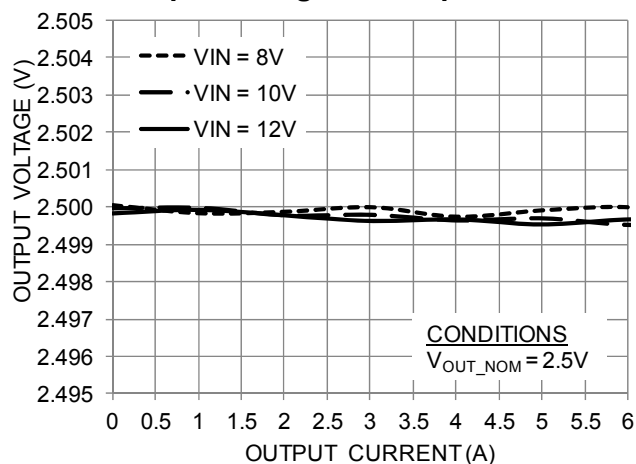
**Output Voltage vs. Output Current**



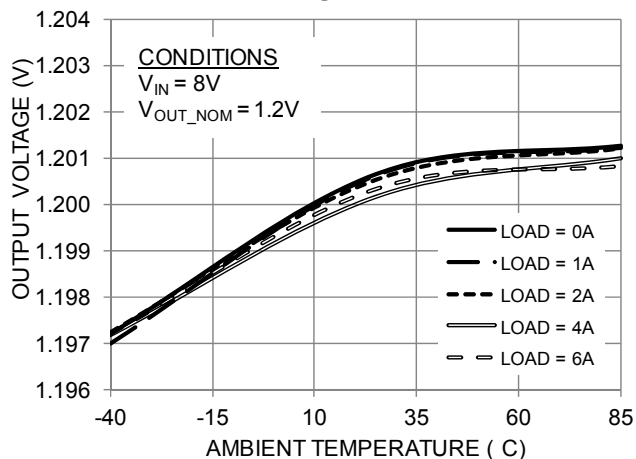
**Output Voltage vs. Output Current**



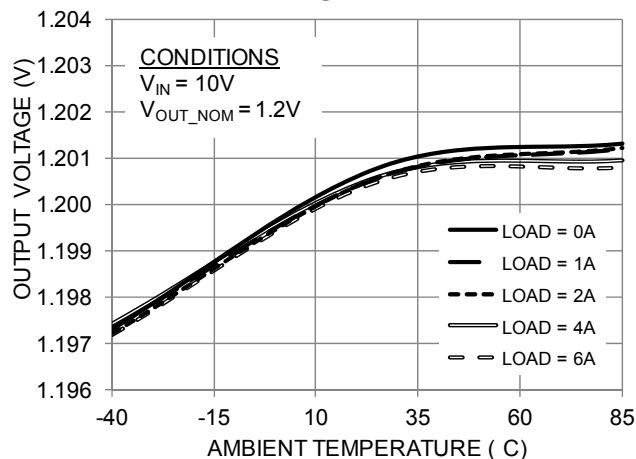
**Output Voltage vs. Output Current**



**Output Voltage vs. Temperature**

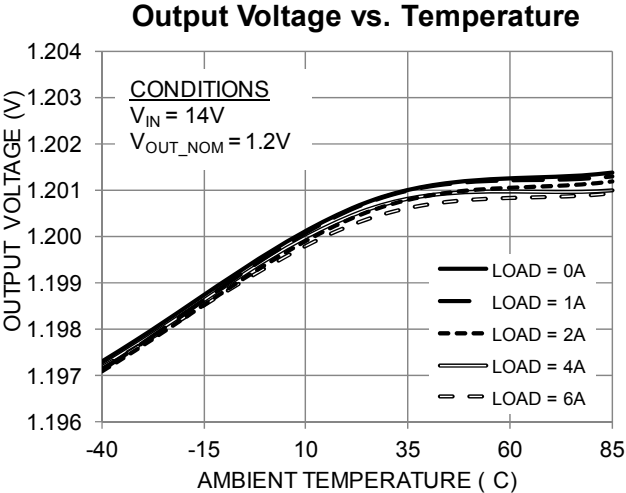
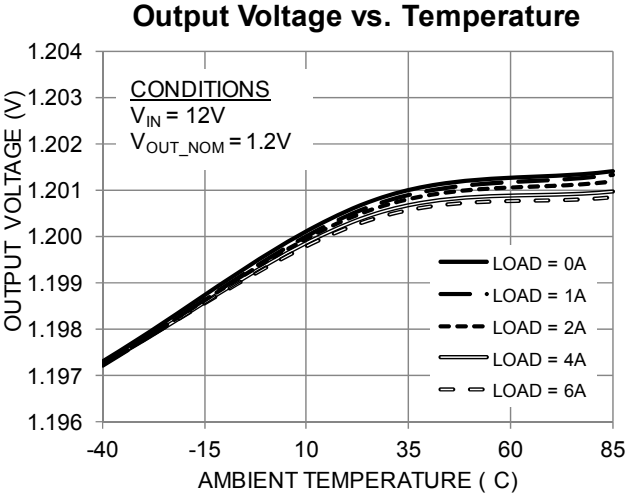


**Output Voltage vs. Temperature**



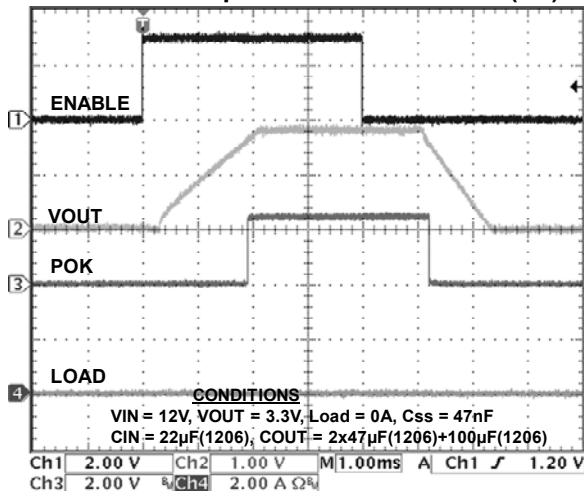


Typical Performance Curves

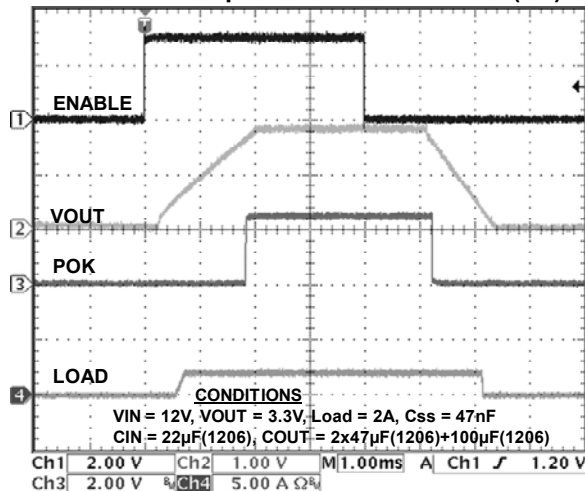


# Typical Performance Characteristics

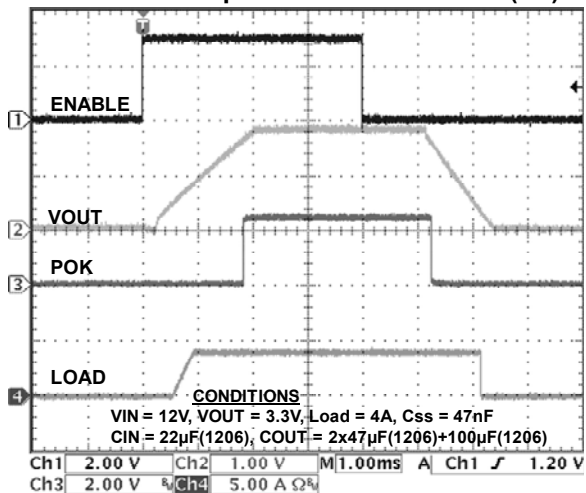
Enable Startup/Shutdown Waveform (0A)



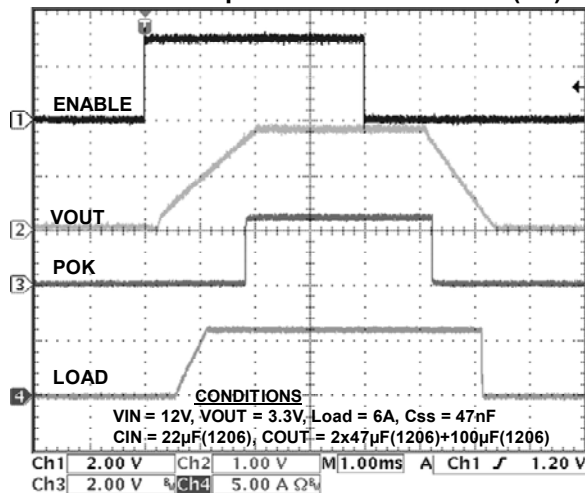
Enable Startup/Shutdown Waveform (2A)



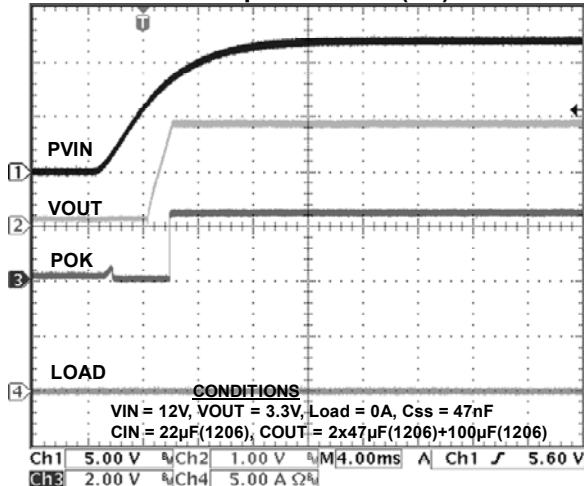
Enable Startup/Shutdown Waveform (4A)



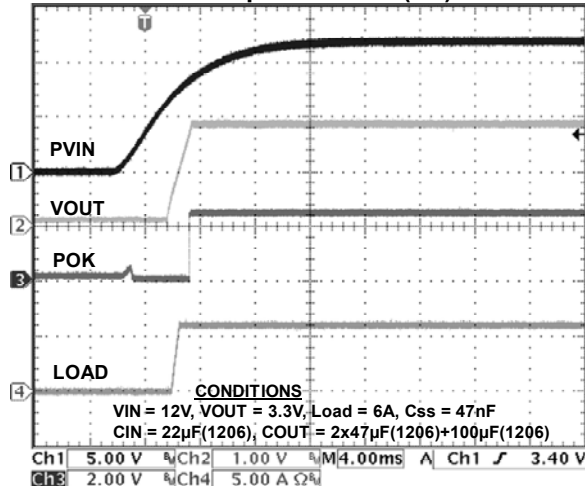
Enable Startup/Shutdown Waveform (6A)



Power Up Waveform (0A)

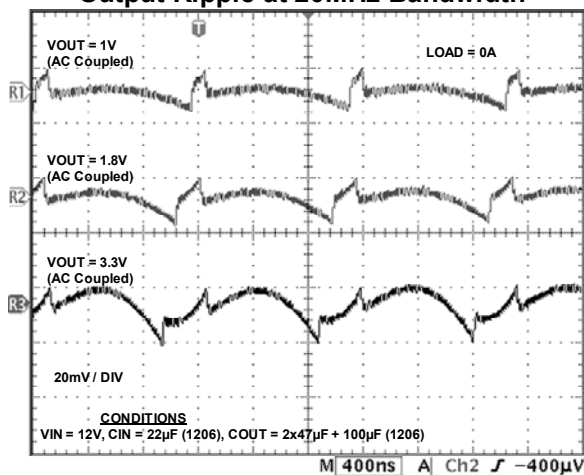


Power Up Waveform (6A)



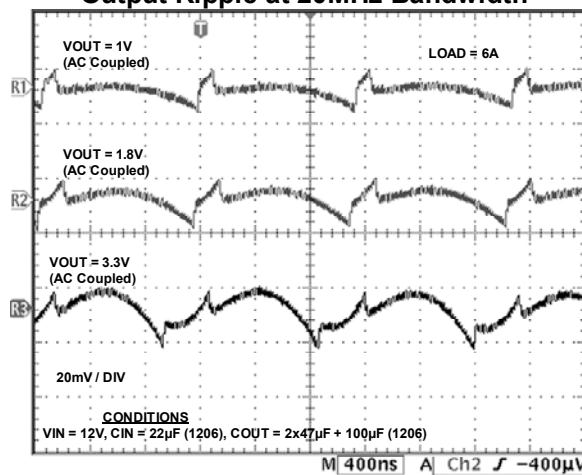
# Typical Performance Characteristics

Output Ripple at 20MHz Bandwidth



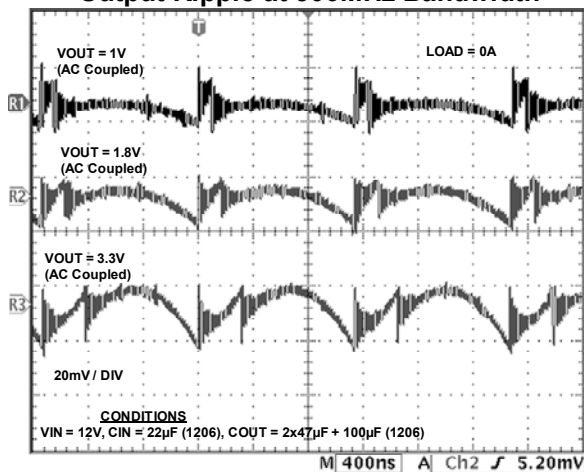
Ref 3 20.0mV 400ns 30.20 %

Output Ripple at 20MHz Bandwidth



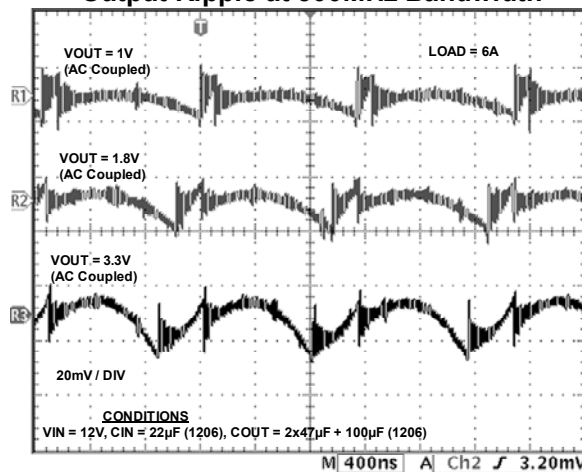
Ref 3 20.0mV 400ns 30.20 %

Output Ripple at 500MHz Bandwidth



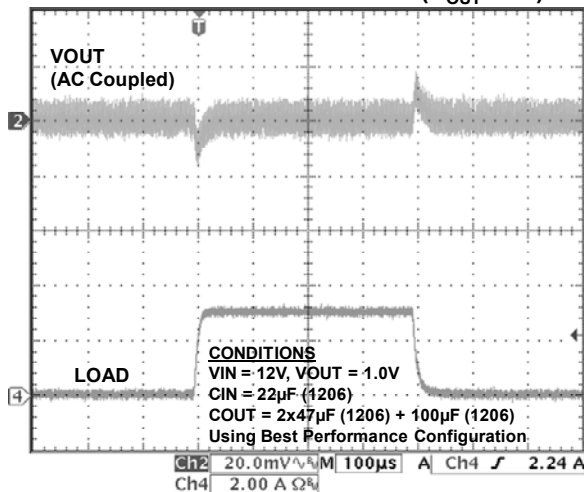
Ref 1 20.0mV 400ns 30.20 %

Output Ripple at 500MHz Bandwidth

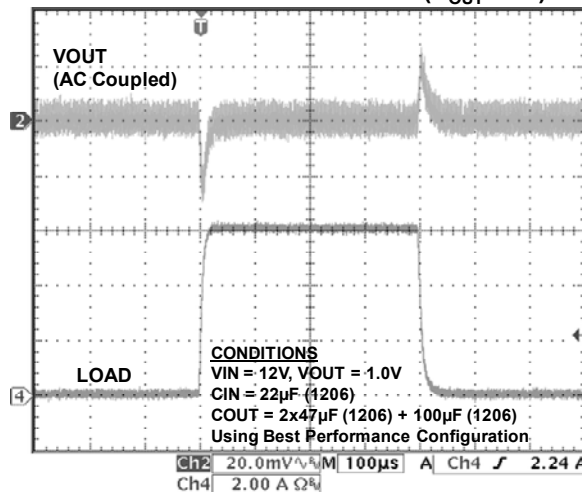


Ref 3 20.0mV 400ns 30.20 %

Load Transient from 0 to 3A ( $V_{OUT} = 1V$ )

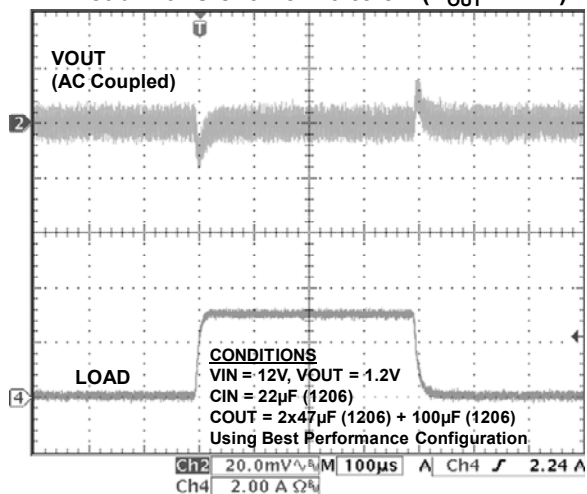


Load Transient from 0 to 6A ( $V_{OUT} = 1V$ )

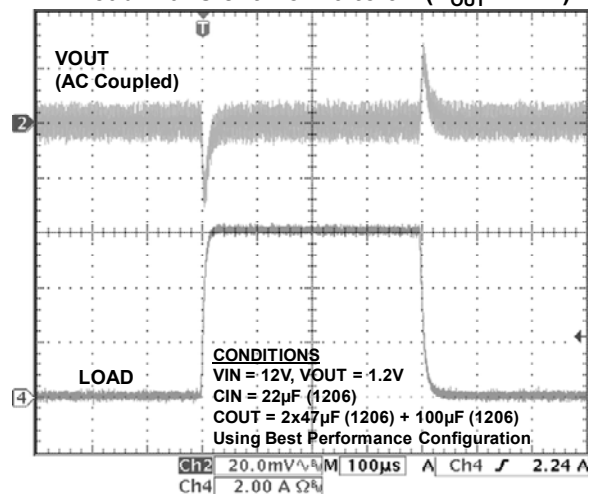


# Typical Performance Characteristics

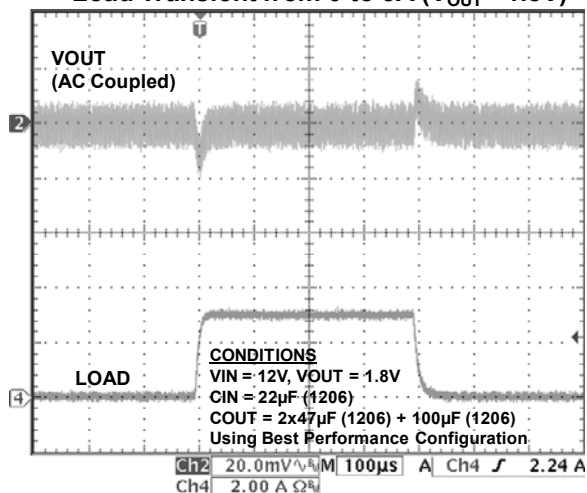
### Load Transient from 0 to 3A ( $V_{OUT} = 1.2V$ )



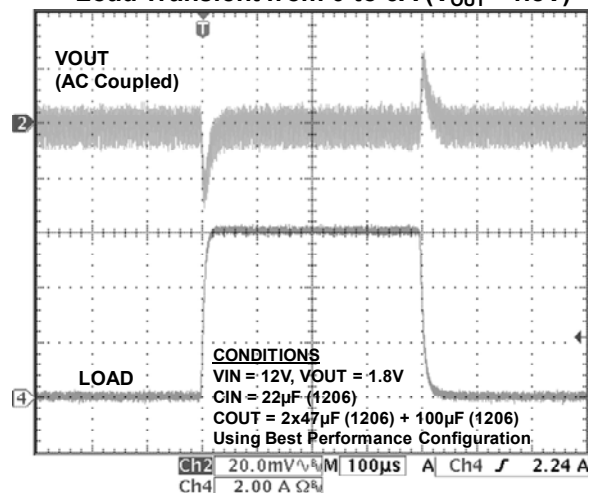
### Load Transient from 0 to 6A ( $V_{OUT} = 1.2V$ )



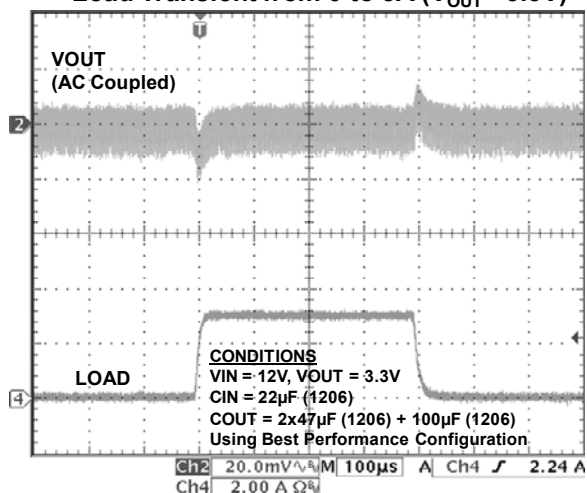
### Load Transient from 0 to 3A ( $V_{OUT} = 1.8V$ )



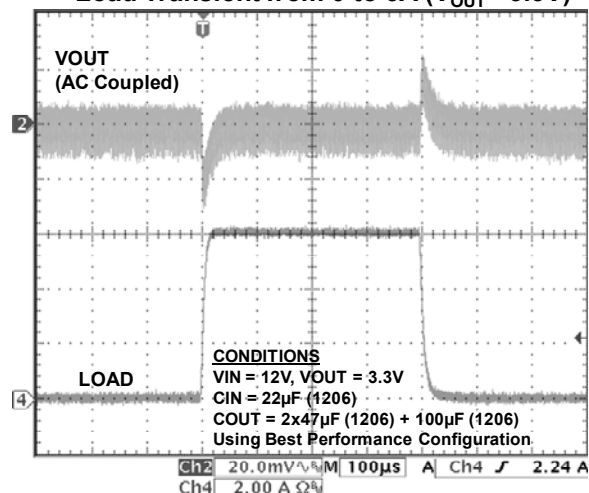
### Load Transient from 0 to 6A ( $V_{OUT} = 1.8V$ )



### Load Transient from 0 to 3A ( $V_{OUT} = 3.3V$ )



### Load Transient from 0 to 6A ( $V_{OUT} = 3.3V$ )



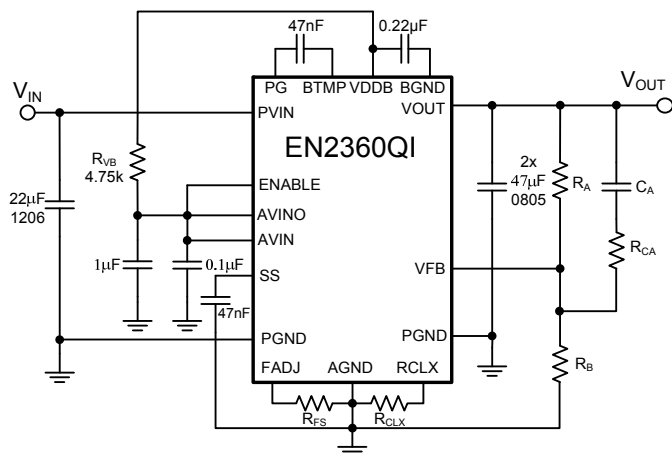




## Power Power Up Sequence

The EN2360QI is designed to be powered by either a single input supply (PVIN) or two separate supplies: one for PVIN and the other for AVIN.

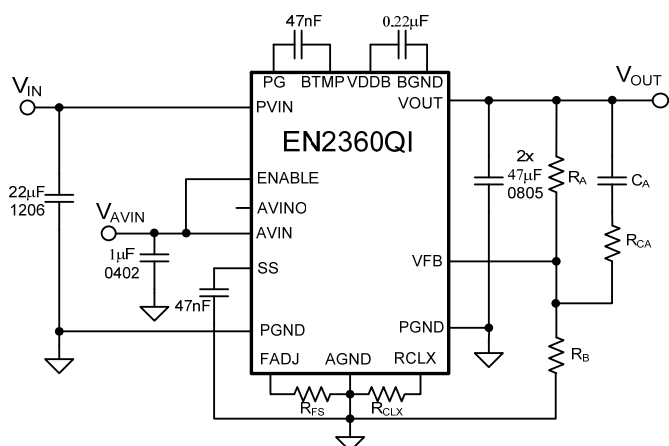
### Single Input Supply Application (PVIN):



**Figure 5.** Single Supply Applications Circuit

The EN2360QI has an internal linear regulator that converts PVIN to 3.3V. The output of the linear regulator is provided on the AVINO pin once the device is enabled. AVINO should be connected to AVIN on the EN2360QI. In this application, the following external components are required: Place a 1µF, X5R/X7R, capacitor between AVINO and AGND as close as possible to AVINO. Place a 0.1µF, X5R/X7R, capacitor between AVIN and AGND as close as possible to AVIN. In addition, place a resistor ( $R_{VB}$ ) between VDDDB and AVIN, as shown in Figure 5. Enpirion recommends  $R_{VB}=4.75k\Omega$ . In this application, ENABLE cannot be asserted before PVIN. If no external enable signal is used, tying ENABLE to AVIN meets this requirement.

### Dual Input Supply Application (PVIN and AVIN):



**Figure 6:** Dual Input Supply Application Circuit

In this application, place a 0.1µF, X7R, capacitor between AVIN and AGND as close as possible to AVIN. Refer to Figure 6 for a recommended schematic for a dual input supply application.

For dual input supply applications, the sequencing of the two input supplies, PVIN and AVIN, is very important. There are two common acceptable turn-on sequences for the device. AVIN can always come up before PVIN. If PVIN comes up before AVIN, then ENABLE should be toggled last, after AVIN is asserted. During turn-off, the ENABLE should be toggled low before AVIN or PVIN is disabled.

## Enable Operation

The ENABLE pin provides a means to enable normal operation or to shut down the device. A logic high will enable the converter into normal operation. When the ENABLE pin is asserted (high) the device will undergo a normal soft-start, allowing the output voltage to rise monotonically into regulation. A logic low will disable the converter and the device will power down in a controlled manner. The ENABLE signal has to be low for at least the ENABLE Lockout Time (8ms) in order for the device to be re-enabled.

## Pre-Bias Precaution

The EN2360QI is not designed to be turned on into a pre-biased output voltage. Be sure the output capacitors are not charged or the output of the EN2360QI is not pre-biased when the EN2360QI is first enabled.

## Frequency Synchronization

The switching frequency of the EN2360QI can be phase-locked to an external clock source to move unwanted beat frequencies out of band. The internal switching clock of the EN2360QI can be phase locked to a clock signal applied to the S\_IN pin. An activity detector recognizes the presence of an external clock signal and automatically phase-locks the internal oscillator to this external clock. Phase-lock will occur as long as the input clock frequency is in the range of 0.8MHz to 1.6MHz. When no clock is present, the device reverts to the free running frequency of the internal oscillator. Adding a resistor ( $R_{FS}$ ) to the FADJ pin will adjust the switching frequency. If a 3kΩ resistor is placed on FADJ the nominal switching frequency of the EN2360QI is 1MHz. Figure 7 shows the typical  $R_{FS}$  resistor value versus switching frequency.

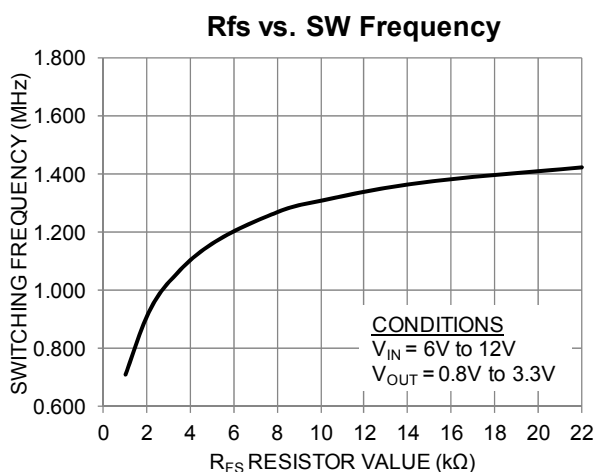


Figure 7. R<sub>FS</sub> versus Switching Frequency

The efficiency performance of the EN2360QI for various V<sub>OUT</sub>s can be optimized by adjusting the switching frequency. Table 1 shows recommended R<sub>FS</sub> values for various V<sub>OUT</sub>s in order to optimize performance of the EN2360QI.

PVIN	VOUT	R <sub>FS</sub>
12V	1.0V	3k
	1.2V	3.3k
	1.8V	4.87k
	2.5V	10k
	3.3V	15k
	5.0V	22k

Table 1: Recommended R<sub>FS</sub> Values

## Spread Spectrum Mode

The external clock frequency may be swept between 0.8MHz and 1.6MHz at repetition rates of up to 10 kHz in order to reduce EMI frequency components.

## Soft-Start Operation

Soft start is a means to ramp the output voltage gradually upon start-up. The output voltage rise time is controlled by the choice of soft-start capacitor, which is placed between the SS pin (pin 56) and the AGND pin (pin 52).

$$\text{Rise Time (ms): } T_R \approx C_{SS} [\text{nF}] \times 0.06$$

During start-up of the converter, the reference voltage to the error amplifier is linearly increased to its final level by an internal current source of approximately 10μA. Typical soft-start rise time is ~2.8ms with SS capacitor value of 47nF. The rise time is measured from when V<sub>IN</sub> > V<sub>UVLOR</sub> and ENABLE pin voltage crosses its logic high

threshold to when V<sub>OUT</sub> reaches its programmed value.

## POK Operation

The POK signal is an open drain signal (requires a pull up resistor to AVIN or similar voltage) from the converter indicating the output voltage is within the specified range. Typically, a 100kΩ or lower resistance is used as the pull-up resistor. The POK signal will be logic high (AVIN) when the output voltage is above 90% of the programmed voltage level. If the output voltage is below this point, the POK signal will be a logic low. The POK signal can be used to sequence down-stream converters by tying to their enable pins.

## Over-Current Protection (OCP)

The current limit function is achieved by sensing the current flowing through a sense PFET. When the sensed current exceeds the current limit, both power FETs are turned off for the rest of the switching cycle. If the over-current condition is removed, the over-current protection circuit will re-enable PWM operation. If the over-current condition persists, the circuit will continue to protect the load. The OCP trip point is nominally set as specified in the Electrical Characteristics table. In the event the OCP circuit trips consistently in normal operation, the device enters a hiccup mode. While in hiccup mode, the device is disabled for a short while and restarted with a normal soft-start. The hiccup time is approximately 32ms. This cycle can continue indefinitely as long as the over current condition persists.

The OCP trip point can be programmed to trip at a lower level via the RCLX pin. The value of the resistor connected between RCLX and ground will determine the OCP trip point. Generally, the higher the RCLX value, the higher the current limit threshold. Note that if RCLX pin is left open the output current will be unlimited and the device will not have current limit protection. Reference Table 2 for a list of recommended resistor values on RCLX that will set the OCP trip point at the typical value of 9A, also specified in the Electrical Characteristics table.

V <sub>OUT</sub> Range	R <sub>CLX</sub> Value
0.6V < V <sub>OUT</sub> ≤ 0.9V	36.5k
0.9V < V <sub>OUT</sub> ≤ 1.2V	38.4k
1.2V < V <sub>OUT</sub> ≤ 2.0V	40.2k
2.0V < V <sub>OUT</sub> ≤ 5.0V	45.3k

Table 2: Recommended R<sub>CLX</sub> Values vs. V<sub>OUT</sub>

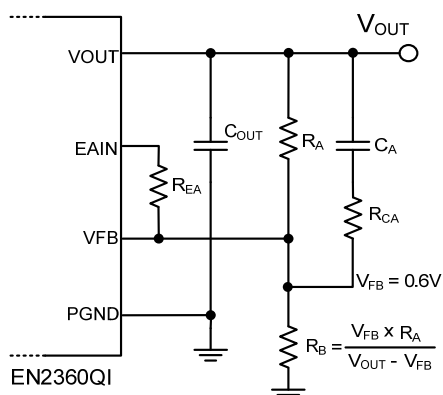
## Thermal Overload Protection

Thermal shutdown circuit will disable device operation when the junction temperature exceeds approximately 150°C. After a thermal shutdown event, when the junction temperature drops by approx 20°C, the converter will re-start with a normal soft-start.

## Application Information

### Output Voltage Programming and Loop Compensation

The EN2360QI uses a Type IV Voltage Mode compensation network. Type IV Voltage Mode control is a proprietary Enpirion control scheme that maximizes control loop bandwidth to deliver excellent load transient responses and maintain output regulation with pin point accuracy. For ease of use, most of this network has been customized and is integrated within the device package. The EN2360QI output voltage is programmed using a simple resistor divider network ( $R_A$  and  $R_B$ ). The feedback voltage at  $V_{FB}$  is nominally 0.6V.  $R_A$  is predetermined based on Table 5 and  $R_B$  can be calculated based on Figure 10. The values recommended for  $C_{OUT}$ ,  $C_A$ ,  $R_{CA}$  and  $R_{EA}$  make up the external compensation of the EN2360QI. It will vary with each  $P_{VIN}$  and  $V_{OUT}$  combination to optimize on performance. The EN2360QI solution can be optimized for either smallest size or highest performance. Please see Table 5 for a list of recommended  $R_A$ ,  $C_A$ ,  $R_{CA}$ ,  $R_{EA}$  and  $C_{OUT}$  values for each solution.



**Figure 8:**  $V_{OUT}$  Resistor Divider & Compensation Components. See Table 5 for details.

### Input Capacitor Selection

The EN2360QI requires a 22 $\mu$ F/1206 input capacitor. Low-cost, low-ESR ceramic capacitors should be used as input capacitors for this

### Input Under-Voltage Lock-Out (UVLO)

Internal circuits ensure that the converter will not start switching until the input voltage is above the specified minimum voltage. Hysteresis, input de-glitch and output leading edge blanking ensures high noise immunity and prevents false UVLO triggers.

converter. The dielectric must be X5R or X7R rated. **Y5V or equivalent dielectric formulations must not be used as these lose too much capacitance with frequency, temperature and bias voltage.** In some applications, lower value capacitors are needed in parallel with the larger, capacitors in order to provide high frequency decoupling. Table 3 contains a list of recommended input capacitors.

### Recommended Input Capacitors

Description	MFG	P/N
22 $\mu$ F, 16V, X5R, 10%, 1206	Murata	GRM31CR61C226ME15
22 $\mu$ F, 16V, X5R, 20%, 1206	Taiyo Yuden	EMK316ABJ226ML-T

**Table 3:** Recommended Input Capacitors

### Output Capacitor Selection

As seen from Table 5, the EN2360QI has been optimized for use with one 100 $\mu$ F/1206 plus two 47 $\mu$ F/1206 output capacitors for best performance. For the smallest solution size configuration see Table 5. Low ESR ceramic capacitors are required with X5R or X7R rated dielectric formulation. **Y5V or equivalent dielectric formulations must not be used as these lose too much capacitance with frequency, temperature and bias voltage.** Table 4 contains a list of recommended output capacitors

Output ripple voltage is determined by the aggregate output capacitor impedance. Capacitor impedance, denoted as  $Z$ , is comprised of capacitive reactance, effective series resistance, ESR, and effective series inductance, ESL reactance.

Placing output capacitors in parallel reduces the impedance and will hence result in lower ripple voltage.



$$\frac{1}{Z_{Total}} = \frac{1}{Z_1} + \frac{1}{Z_2} + \dots + \frac{1}{Z_n}$$

### Recommended Output Capacitors

Description	MFG	P/N
47µF, 6.3V, X5R, 20%, 1206	Murata	GRM31CR60J476ME19L
47µF, 10V, X5R, 20%, 1206	Taiyo Yuden	LMK316BJ476ML-T

22µF, 10V, X5R, 20%, 0805	Panasonic	ECJ-2FB1A226M
47µF, 6.3V, X5R, 20%, 0805	Taiyo Yuden	JMK212BBJ476MG-T
22µF, 10V, X5R, 20%, 0805	Taiyo Yuden	LMK212BJ226MG-T

**Table 4:** Recommended Output Capacitors

Best Performance							Smallest Solution Size							
$C_{IN} = 22\mu F/1206$							$C_{IN} = 22\mu F/1206$							
$C_{OUT} = 100\mu F/1206 + 2 \times 47\mu F/1206, R_A = 200k\Omega$							$V_{OUT} \leq 1.8V, C_{OUT} = 2 \times 47\mu F/0805$ $3.3V > V_{OUT} > 1.8V, C_{OUT} = 2 \times 47\mu F/1206$							
PVIN (V)	VOUT (V)	$C_A$ (pF)	$R_{CA}$ (k $\Omega$ )	$R_{EA}$ (k $\Omega$ )	Ripple (mV)	Deviation (mV)	PVIN (V)	VOUT (V)	$R_A$ (k $\Omega$ )	$C_A$ (pF)	$R_{CA}$ (k $\Omega$ )	$R_{EA}$ (k $\Omega$ )	Ripple (mV)	Deviation (mV)
14V	0.9V	15	8.2	0	5.29	26	14V	0.9V	200	10	0.2	Open	15	51
	1.2V	12	8.2	0	6.6	22		1.2V	200	10	0.2	Open	19	68
	1.5V	12	12	0	8.39	24		1.5V	200	10	0.2	Open	24	66
	1.8V	10	12	0	9.7	28		1.8V	200	8.2	0.2	Open	24	66
	2.5V	10	12	56	18.8	54		2.5V	120	8.2	15	Open	43	86
	3.3V	8.2	18	56	28.8	54		3.3V	120	6.8	15	Open	52	106
	5.0V	6.8	12	56	52.1	66		5.0V	120	5.6	0.2	Open	66	152
12V	0.9V	15	8.2	0	5.22	28	12V	0.9V	200	12	0.2	Open	17	57
	1.2V	15	8.2	0	6.51	22		1.2V	200	12	0.2	Open	18	70
	1.5V	12	12	0	7.5	28		1.5V	200	12	0.2	Open	24	70
	1.8V	10	12	0	9	34		1.8V	200	10	0.2	Open	26	80
	2.5V	12	12	56	16.8	50		2.5V	120	10	15	Open	39	94
	3.3V	10	18	56	27.3	54		3.3V	120	10	15	Open	45	114
	5.0V	8.2	12	56	48.5	74		5.0V	120	6.8	0.2	Open	56	164
10V	0.9V	18	8.2	0	5.01	28	10V	0.9V	200	18	0.2	Open	15	69
	1.2V	18	8.2	0	6.11	26		1.2V	200	18	0.2	Open	19	67
	1.5V	15	12	0	7.3	28		1.5V	200	15	0.2	Open	23	78
	1.8V	12	12	0	8.13	32		1.8V	200	12	0.2	Open	29	94
	2.5V	15	12	56	16.8	44		2.5V	120	15	15	Open	29	98
	3.3V	12	18	56	27.2	68		3.3V	120	12	15	Open	44	128
	5.0V	10	12	56	42	84		5.0V	120	10	0.2	Open	52	192
8V	0.9V	22	8.2	0	4.92	26	8V	0.9V	200	27	0.2	Open	16	68
	1.2V	18	8.2	0	5.41	32		1.2V	200	22	0.2	Open	19	75
	1.5V	15	12	0	6.48	32		1.5V	200	22	0.2	Open	23	82
	1.8V	15	12	0	7.32	36		1.8V	200	18	0.2	Open	27	104
	2.5V	18	12	56	16.1	64		2.5V	120	27	6.8	Open	36	124
	3.3V	15	18	56	24	72		3.3V	120	22	6.8	Open	36	152
	5.0V	12	12	56	31.4	102		5.0V	120	12	0.2	Open	40	236
6.6V	0.9V	22	8.2	0	4.6	30	6.6V	0.9V	200	33	0.2	Open	14	70
	1.2V	22	8.2	0	5.59	32		1.2V	200	33	0.2	Open	17	80
	1.5V	18	12	0	5.88	36		1.5V	200	27	0.2	Open	21	96
	1.8V	18	12	0	7.12	38		1.8V	200	27	0.2	Open	24	110
	2.5V	22	12	56	15.4	56		2.5V	120	39	4.3	Open	29	140
	3.3V	18	18	56	21.6	78		3.3V	120	27	4.3	Open	28	184
	5.0V	27	8.2	0	3.93	32		5.0V	200	68	0.2	Open	13	80
5V	1.2V	22	8.2	0	4.4	38	5V	1.2V	200	56	0.2	Open	15	92
	1.5V	22	12	0	5.91	38		1.5V	200	47	0.2	Open	17	106
	1.8V	22	12	0	6.91	42		1.8V	200	39	0.2	Open	19	124
	2.5V	27	12	56	13.6	76		2.5V	120	68	0.2	Open	21	172

**Table 5:**  $R_A$ ,  $C_A$ ,  $R_{CA}$  and  $R_{EA}$  Values for Various PVIN/VOUT Combinations: Smallest Solution Size vs. Best Performance. See Figure 8. Use the equation in Figure 8 to calculate  $R_B$ .

**Note 6:** Nominal Deviation is for a 6A load transient step.

**Note 7:** For compensation values of output voltage in between the specified output voltages, choose compensation values of the lower output voltage setting.

## Thermal Considerations

Thermal considerations are important power supply design facts that cannot be avoided in the real world. Whenever there are power losses in a system, the heat that is generated by the power dissipation needs to be accounted for. The Enpirion PowerSoC helps alleviate some of those concerns.

The Enpirion EN2360QI DC-DC converter is packaged in an 8x11x3mm 68-pin QFN package. The QFN package is constructed with copper lead frames that have exposed thermal pads. The exposed thermal pad on the package should be soldered directly on to a copper ground pad on the printed circuit board (PCB) to act as a heat sink. The recommended maximum junction temperature for continuous operation is 125°C. Continuous operation above 125°C may reduce long-term reliability. The device has a thermal overload protection circuit designed to turn off the device at an approximate junction temperature value of 150°C.

The following example and calculations illustrate the thermal performance of the EN2360QI.

Example:

$$V_{IN} = 12V$$

$$V_{OUT} = 3.3V$$

$$I_{OUT} = 6A$$

First calculate the output power.

$$P_{OUT} = 3.3V \times 6A = 19.8W$$

Next, determine the input power based on the efficiency ( $\eta$ ) shown in Figure 9.

$$\eta = P_{OUT} / P_{IN} = 87\% = 0.87$$

$$P_{IN} = P_{OUT} / \eta$$

$$P_{IN} \approx 19.8W / 0.87 \approx 22.76W$$

The power dissipation ( $P_D$ ) is the power loss in the system and can be calculated by subtracting the output power from the input power.

$$P_D = P_{IN} - P_{OUT}$$

$$\approx 22.76W - 19.8W \approx 2.96W$$

With the power dissipation known, the temperature rise in the device may be estimated based on the theta JA value ( $\theta_{JA}$ ). The  $\theta_{JA}$  parameter estimates how much the temperature will rise in the device for every watt of power dissipation. The EN2360QI has a  $\theta_{JA}$  value of 16 °C/W without airflow.

Determine the change in temperature ( $\Delta T$ ) based on  $P_D$  and  $\theta_{JA}$ .

$$\Delta T = P_D \times \theta_{JA}$$

$$\Delta T \approx 2.96W \times 16^\circ C/W = 47.36^\circ C \approx 47^\circ C$$

The junction temperature ( $T_J$ ) of the device is approximately the ambient temperature ( $T_A$ ) plus the change in temperature. We assume the initial ambient temperature to be 25°C.

$$T_J = T_A + \Delta T$$

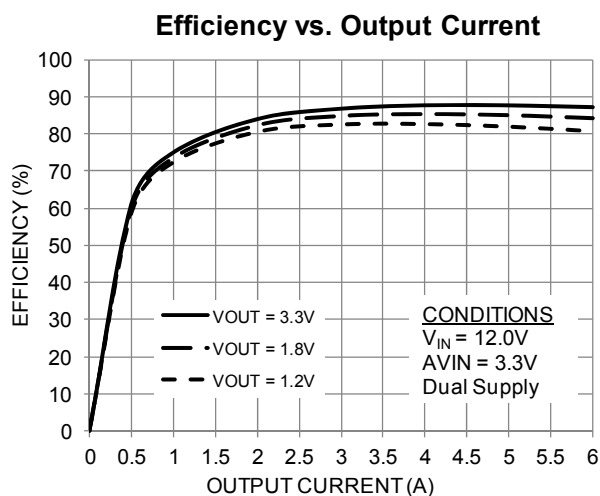
$$T_J \approx 25^\circ C + 47^\circ C \approx 72^\circ C$$

The maximum operating junction temperature ( $T_{JMAX}$ ) of the device is 125°C, so the device can operate at a higher ambient temperature. The maximum ambient temperature ( $T_{AMAX}$ ) allowed can be calculated.

$$T_{AMAX} = T_{JMAX} - P_D \times \theta_{JA}$$

$$\approx 125^\circ C - 47^\circ C \approx 78^\circ C$$

The maximum ambient temperature the device can reach is 78°C given the input and output conditions. Note that the efficiency will be slightly lower at higher temperatures and this calculation is an estimate.



**Figure 9:** Efficiency vs. Output Current

For  $V_{IN} = 12V$ ,  $V_{OUT} = 3.3V$  at 6A,  $\eta \approx 90\%$

Engineering Schematic

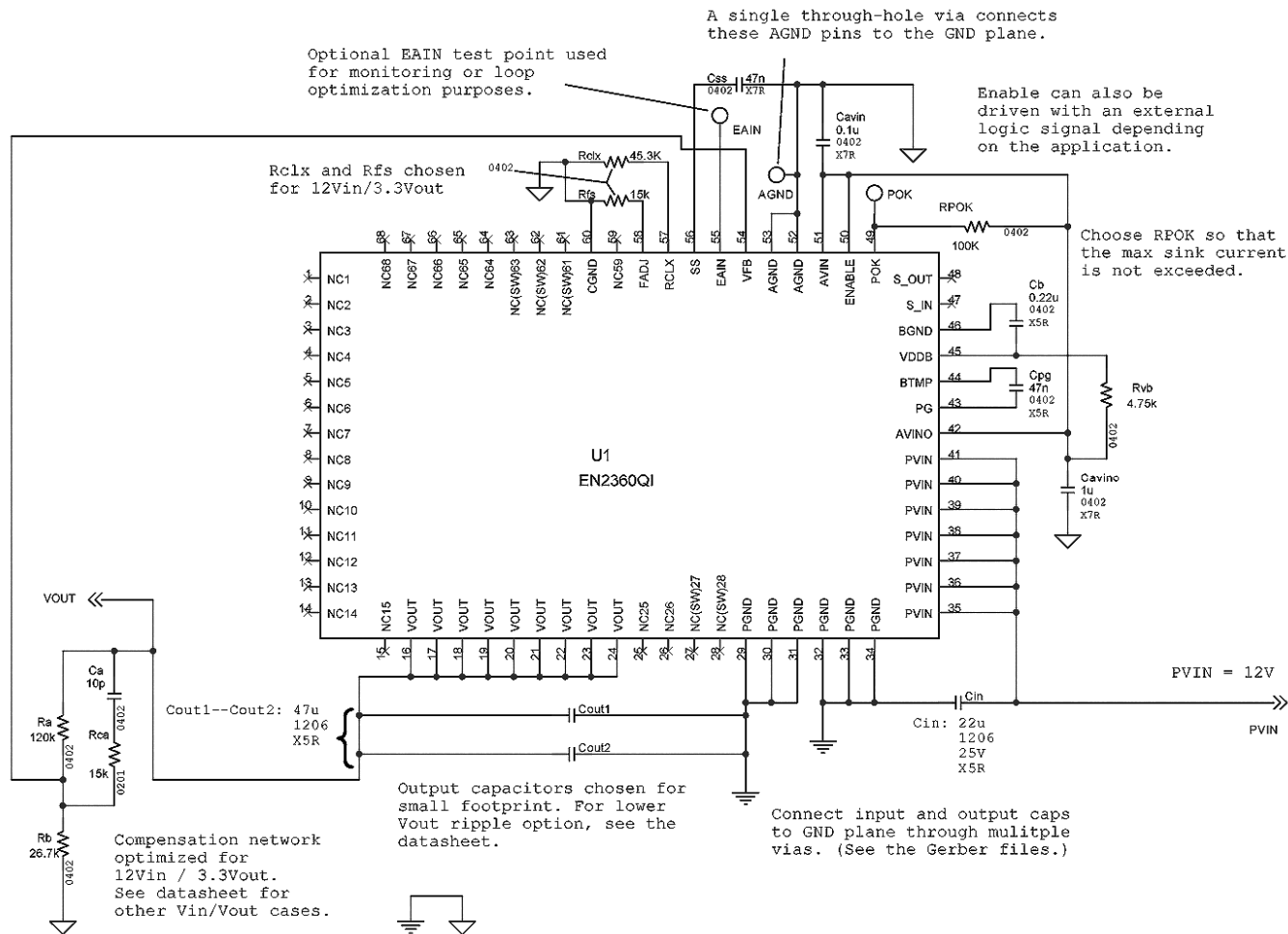
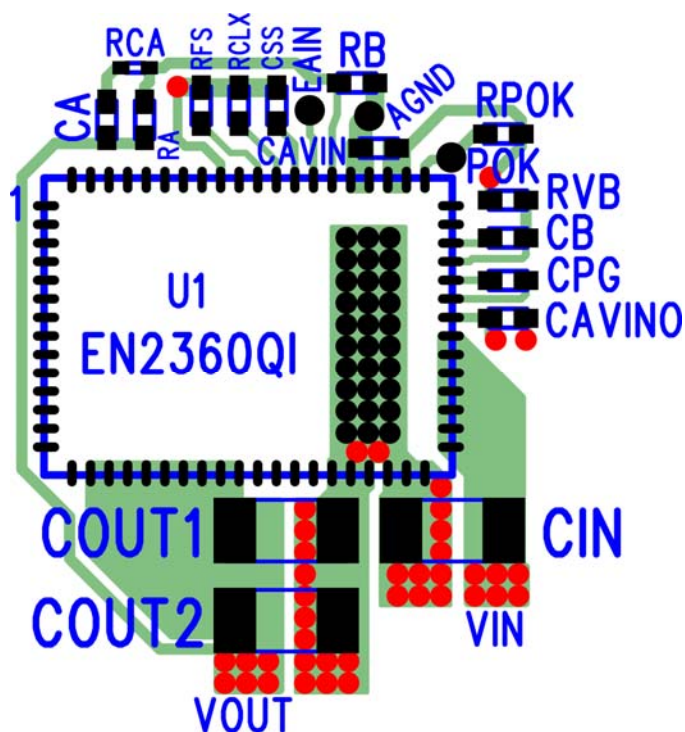


Figure 10: Engineering Schematic with Engineering Notes

## Layout Recommendation



**Figure 11:** Top Layer Layout with Critical Components (Top View). See Figure 10 for corresponding schematic.

*This layout only shows the critical components and top layer traces for minimum footprint in single-supply mode with ENABLE tied to AVIN. Alternate circuit configurations & other low-power pins need to be connected and routed according to customer application. Please see the Gerber files at [www.enpirion.com](http://www.enpirion.com) for details on all layers.*

**Recommendation 1:** Input and output filter capacitors should be placed on the same side of the PCB, and as close to the EN2360QI package as possible. They should be connected to the device with very short and wide traces. Do not use thermal reliefs or spokes when connecting the capacitor pads to the respective nodes. The +V and GND traces between the capacitors and the EN2360QI should be as close to each other as possible so that the gap between the two nodes is minimized, even under the capacitors.

**Recommendation 2:** The PGND connections for the input and output capacitors on layer 1 need to have a slit between them in order to provide some separation between input and output current loops.

**Recommendation 3:** The system ground plane should be the first layer immediately below the surface layer. This ground plane should be continuous and un-interrupted below the converter and the input/output capacitors.

**Recommendation 4:** The thermal pad underneath the component must be connected to the system ground plane through as many vias as possible. The drill diameter of the vias should be 0.33mm, and the vias must have at least 1 oz. copper plating on the inside wall, making the finished hole size around 0.20-0.26mm. Do not use thermal reliefs or spokes to connect the vias to the ground plane. This connection provides the path for heat dissipation from the converter.

**Recommendation 5:** Multiple small vias (the same size as the thermal via discussed in recommendation 4) should be used to connect ground terminal of the input capacitor and output capacitors to the system ground plane. It is preferred to put these vias along the edge of the GND copper closest to the +V copper. These vias connect the input/output filter capacitors to the GND plane, and help reduce parasitic inductances in the input and output current loops. If vias cannot be placed under the capacitors, then place them on both sides of the slit in the top layer PGND copper.

**Recommendation 6:** AVIN is the power supply for the small-signal control circuits. It should be connected to the input voltage at a quiet point. In Figure 11 this connection is made at the input capacitor.

**Recommendation 7:** The layer 1 metal under the device must not be more than shown in Figure 11. Refer to the section regarding Exposed Metal on Bottom of Package. As with any switch-mode DC/DC converter, try not to run sensitive signal or control lines underneath the converter package on other layers.

**Recommendation 8:** The  $V_{OUT}$  sense point should be just after the last output filter capacitor. Keep the sense trace short in order to avoid noise coupling into the node. Contact Enpirion Technical Support for any remote sensing applications.

**Recommendation 9:** Keep  $R_A$ ,  $C_A$ ,  $R_B$ , and  $R_{CA}$  close to the VFB pin (Refer to Figure 11). The VFB pin is a high-impedance, sensitive node. Keep the trace to this pin as short as possible. Whenever possible, connect  $R_B$  directly to the AGND (pin 52, 53) instead of going through the GND plane.

**Recommendation 10:** Follow all the layout recommendations as close as possible to optimize performance. Enpirion provides schematic and layout reviews for all customer designs. Contact Enpirion Applications Engineering for detailed support ([techsupport@enpirion.com](mailto:techsupport@enpirion.com)).

## Design Considerations for Lead-Frame Based Modules

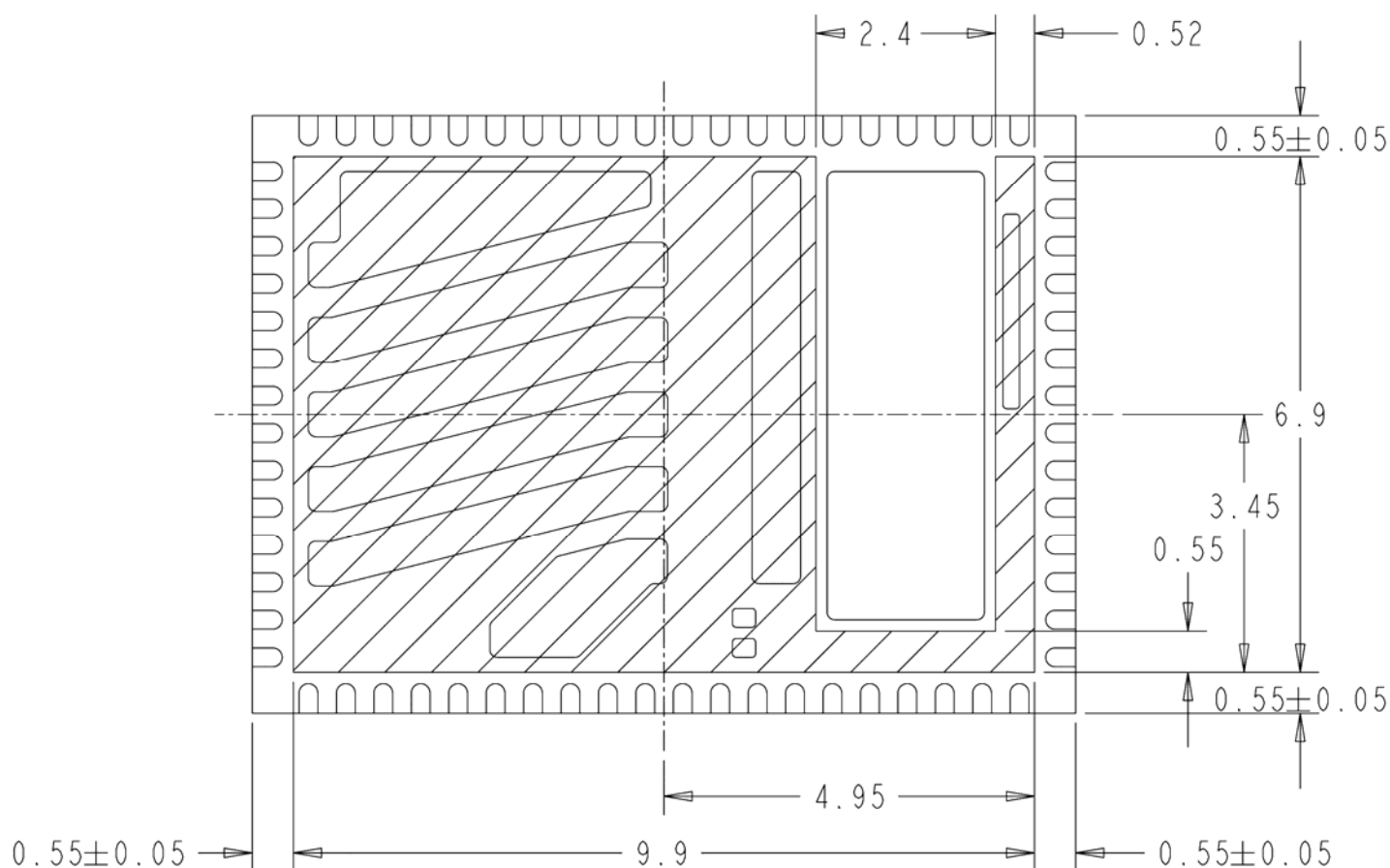
### Exposed Metal on Bottom of Package

Lead-frames offer many advantages in thermal performance, in reduced electrical lead resistance, and in overall foot print. However, they do require some special considerations.

In the assembly process lead frame construction requires that, for mechanical support, some of the lead-frame cantilevers be exposed at the point where wire-bond or internal passives are attached. This results in several small pads being exposed on the bottom of the package, as shown in Figure 10.

Only the thermal pad and the perimeter pads are to be mechanically or electrically connected to the PC board. The PCB top layer under the EN2360QI should be clear of any metal (copper pours, traces, or vias) except for the thermal pad. The “shaded-out” area in Figure 10 represents the area that should be clear of any metal on the top layer of the PCB. Any layer 1 metal under the shaded-out area runs the risk of undesirable shorted connections even if it is covered by soldermask.

The solder stencil aperture should be smaller than the PCB ground pad. This will prevent excess solder from causing bridging between adjacent pins or other exposed metal under the package. Please consult the Enpirion Manufacturing Application Note for more details and recommendations.



**Figure 12:** Lead-Frame exposed metal (Bottom View)

Shaded area highlights exposed metal that is not to be mechanically or electrically connected to the PCB.

Recommended PCB Footprint

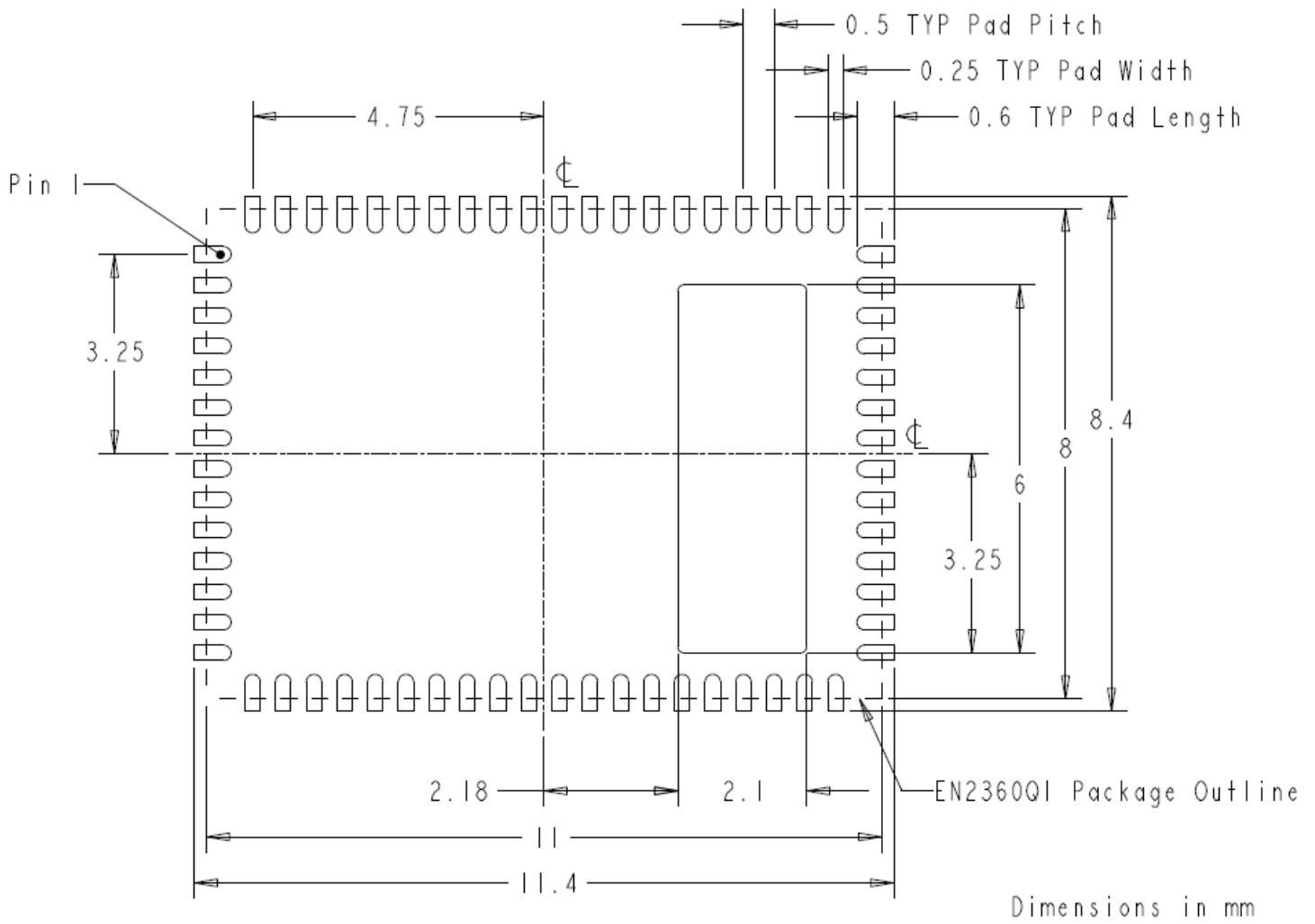
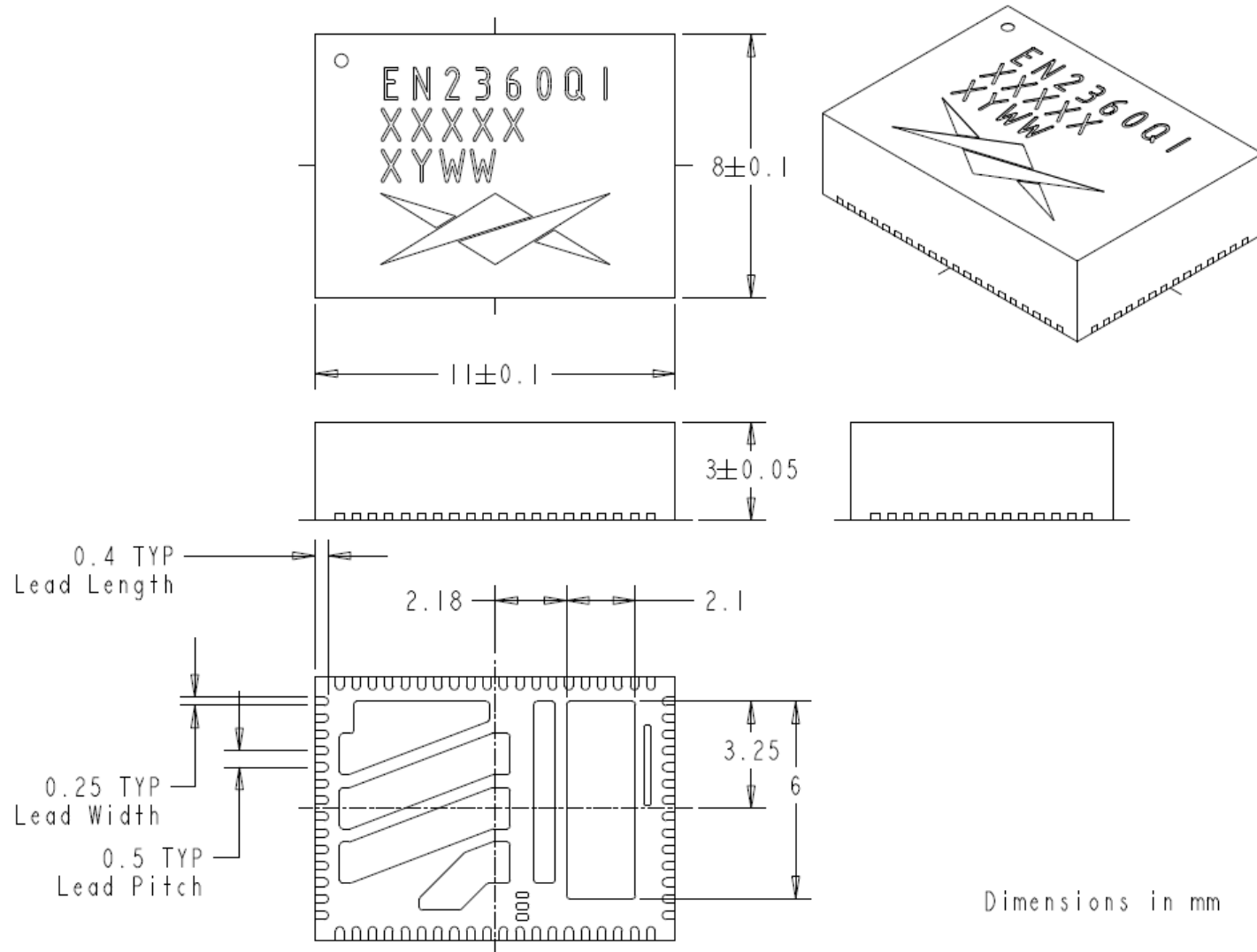


Figure 13: EN2360QI PCB Footprint (Top View)



## Package and Mechanical



**Figure 14:** EN2360QI Package Dimensions (Bottom View)

**Packing and Marking Information:** <http://www.enpirion.com/resource-center-packing-and-marking-information.htm>

## Contact Information

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