ISD8101

1.5W Audio Amplifier

with Chip Enable

1 GENERAL DESCRIPTION

The ISD8100 is a general purpose analog audio amplifier capable of driving an 8-ohm load with up to 1.5Wrms output power. This device includes current limiting and a chip enable pin with low standby current and excellent pop-and-click performance.

Also included is the ability for the inputs to be configured as either single-ended or differential. Internal resistors set the device gain at 20dB. With external resistors, any gain less than 20dB can be achieved. The device is unity gain stable, including when used with external feedback resistors and external capacitors as may be optionally used for implementing simple filtering functions.

2 FEATURES

- Wide power supply range and excellent standby current
  - o 2.4Vdc - 6.8Vdc operation
  - o <1uA standby current
- High output power (capless BTL configuration)
  - o Up to 1.5-W output into 8-ohm load (<10% distortion) with 6.8Vdc supply voltage
  - o < 0.1% distortion at 500mW into 8-ohms with 5Vdc supply voltage
- Excellent pop-and-click performance
  - o Low to inaudible pop/click using Chip Enable
- Single-Ended or Differential signal inputs
  - o > 40dB common mode rejection in differential mode
  - o > 40dB power supply noise rejection
- Very fast start-up time
  - o Less than 1msec when using Chip Enable
- Current limiting for over-current conditions
- Package options: Pb-free SOP-8, SOP-8 (Ex-Pad), PDIP-8
- Temperature Range: -40°C to +85°C

Applications:

- Toys
- Mobile Phones
- Greeting Cards
- Portable Speakers
- Boom Box
- White Goods

3 BLOCK DIAGRAM

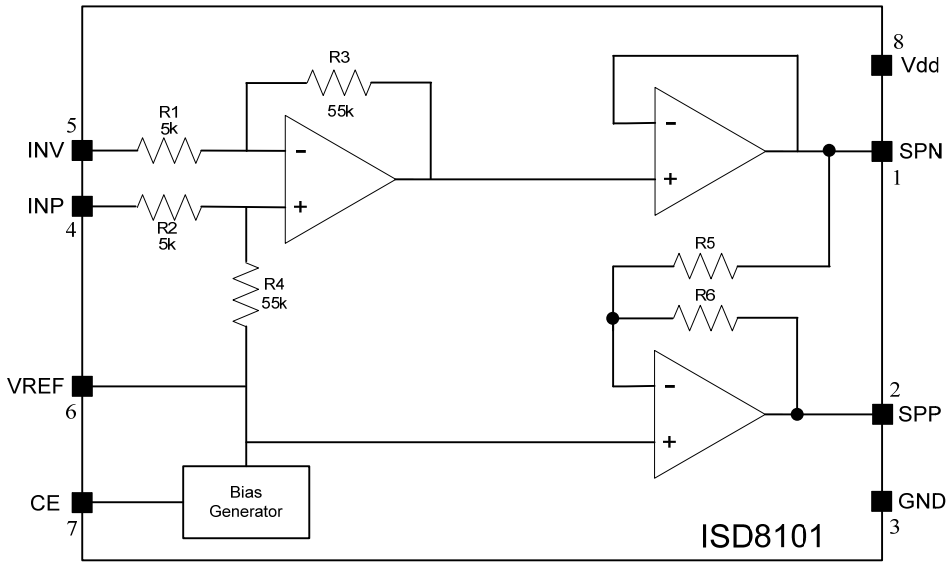


Figure 3-1 ISD8101 Block Diagram

4 PINOUT CONFIGURATION:

4.1 SOP- 8

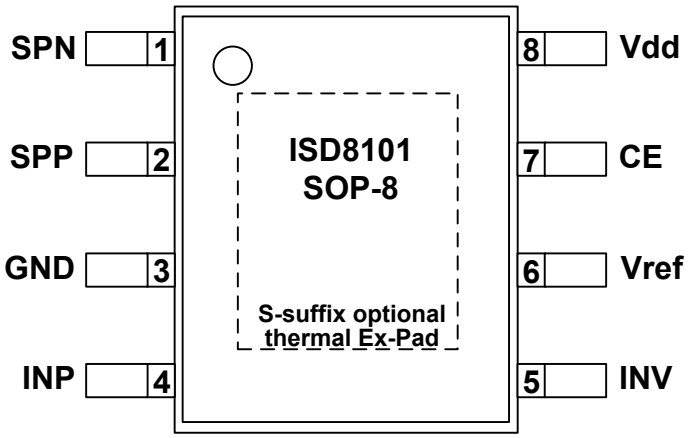


Figure 4-1 ISD8101 8-Lead SOP Pin Configuration.

4.2 PDIP-8

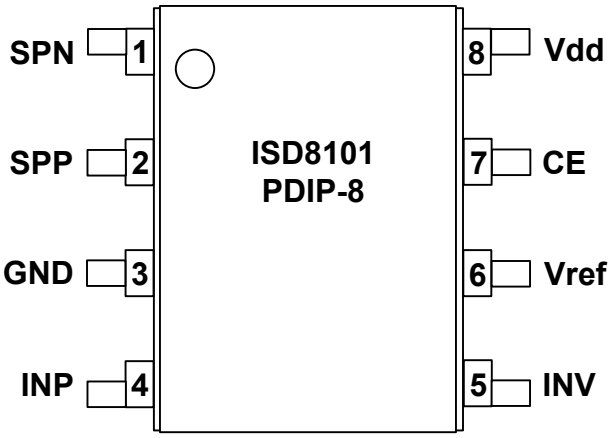


Figure 4-2 ISD8101 8-Lead PDIP Pin Configuration.

5 PIN DESCRIPTION

Pin Number	Pin Name	I/O	Function
1	SPN	O	Non-Inverting Speaker Output
2	SPP	O	Inverting Speaker Output
3	GND	I	Ground
4	INP	I	Non-Inverting Signal Input
5	INV	I	Inverting Signal Input
6	Vref	O	Internal Reference Voltage (1/2 Vdd)
7	CE	I	Chip Enable
8	Vdd	I	Supply Voltage
9	Ex-Pad	I	Thermal Tab (must be connected to Vss, SOP-8 package, only)

6 ELECTRICAL CHARACTERISTICS

6.1 OPERATING CONDITIONS

OPERATING CONDITIONS (DIE)

CONDITIONS	VALUES
Operating temperature range [1]	-40°C to +85°C
Supply voltage (V_{DD})	+2.4V to +6.8V
Ground voltage (V_{SS})	0V
Input voltage (V_{DD})	Vss to V_{DD}
Voltage applied to any pins	(V_{SS} –0.3V) to (V_{DD} +0.3V)

OPERATING CONDITIONS (INDUSTRIAL PACKAGED PARTS)

CONDITIONS	VALUES
Operating temperature range (Case temperature) [1]	-40°C to +85°C
Supply voltage (V_{DD})	+2.4V to +6.8V
Ground voltage (V_{SS})	0V
Input voltage (V_{DD})	Vss to V_{DD}
Voltage applied to any pins	(V_{SS} –0.3V) to (V_{DD} +0.3V)

Notes: [1] Conditions V_{DD}=3.3V, T_A=25°C unless otherwise stated. Die temperature must at all times be kept less than 125°C by appropriate thermal design of the system.

6.2 DC PARAMETERS

PARAMETER	SYMBOL	MIN	TYP [1]	MAX	UNITS	CONDITIONS
Supply Voltage	V_{DD}	2.4		6.8	V	
Operating Current	I_{DD}		2.4		mA	V_{DD} = 5V, no load
Standby Current	I_{SB}		0.1	1	µA	V_{DD} = 5V
CE input resistance			20k		Ω	Internal pull-down
CE input current			120		µA	CE = 2.3V, V_{DD}= 5V
CE threshold enabled	V_{ENL}		0.9		V	All supply voltages
CE threshold standby	V_{ENH}		1.5		V	All supply voltages
Vref Reference Voltage			V_{DD}/2		V	

Notes: [1] Conditions V_{DD} = 3.3V, T_A = 25°C unless otherwise stated. Die temperature must at all times be kept less than 125°C by appropriate thermal design of the system.

6.3AC PARAMETERS

6.3.1 Analog Characteristics; Cref=4.7uF

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	CONDITIONS
Audio Input Voltage Range			0.3 - 5.5		V	Vdd = 6.8Vdc
			0.3 - 2.3		V	Vdd = 3.3Vdc
			0.5 - 1.4		V	Vdd = 2.4Vdc
Inverting Input Impedance			5k		Ω	Gain=20dB
Non-Inverting Input Impedance			60k		Ω	Gain=20dB
Power Supply Rejection Ratio	PSRR		41		dB	Vdd = 5Vdc
Common Mode Rejection Ratio	CMRR		40		dB	Signal at INP = INV
Voltage Gain			20		dB	Rinput = zero-ohms
Enable Time from Standby			0.5		msec	Single-ended
Enable Time from Standby			0.5		msec	Differential
Pop-and-Click from Standby [1]			10		mV	Single Ended
Pop-and-Click from Standby [1]			10		mV	Differential
Thermal Resistance			90		°C/W	SOP-8 (with Ex-Pad)
Thermal Resistance			150		°C/W	SOP-8
Thermal Resistance			117		°C/W	PDIP-8

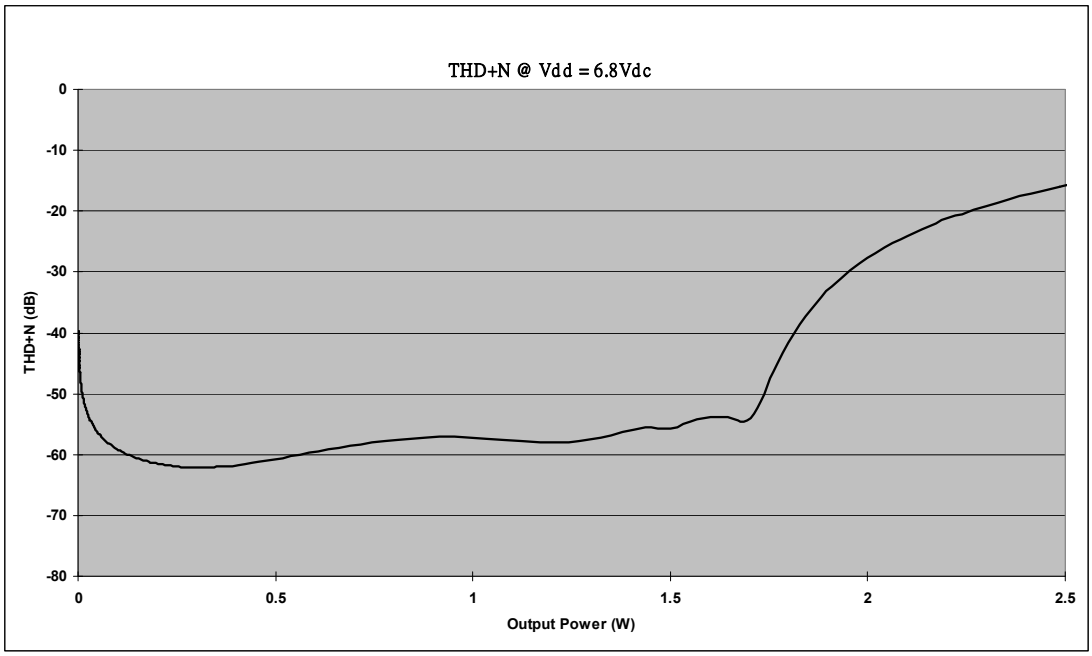
Notes: [1] Impulse voltage that is potentially audible. After impulse, there is a slow ramp from standby Vref to operating Vref, which is typically inaudible with Cref = 4.7uF

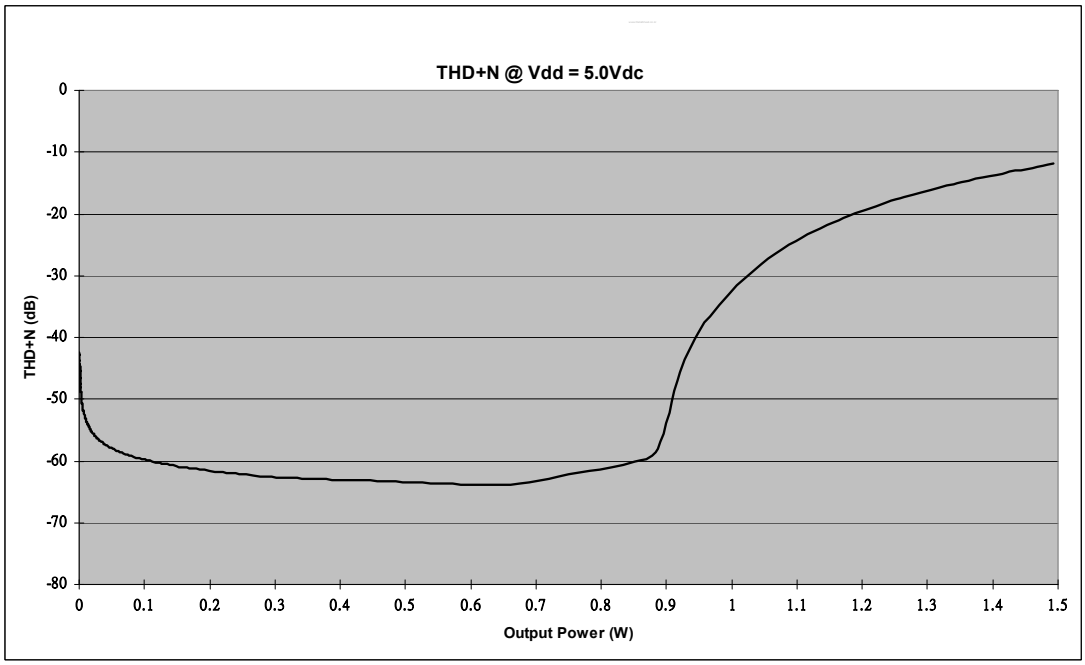
6.3.2 Speaker Outputs

PARAMETER	SYMBOL	MIN	TYP[1]	MAX	UNITS	CONDITIONS
Signal-to-Noise Ratio	SNR		100		dB	0dB gain, 5Vdc
Output Power (BTL mode) Load 8Ω Vdd=5Vdc 0dB gain Distortion = THD+N			500		mW	<0.1% distortion
			825		mW	<1% distortion
			1000		mW	5.6% distortion
			1.1		Watt	<10% distortion
			1.5		Watt	<10% distortion and Vdd = 6.8Vdc
Load Impedance	$R_{L(SPK)}$	7.5	8		Ω	
Output Offset Voltage			8		mV	

Notes: [1] Conditions V_{DD}=3.3V, T_A=25°C unless otherwise stated. Die temperature must at all times be kept less than 125°C by appropriate thermal design of the system.

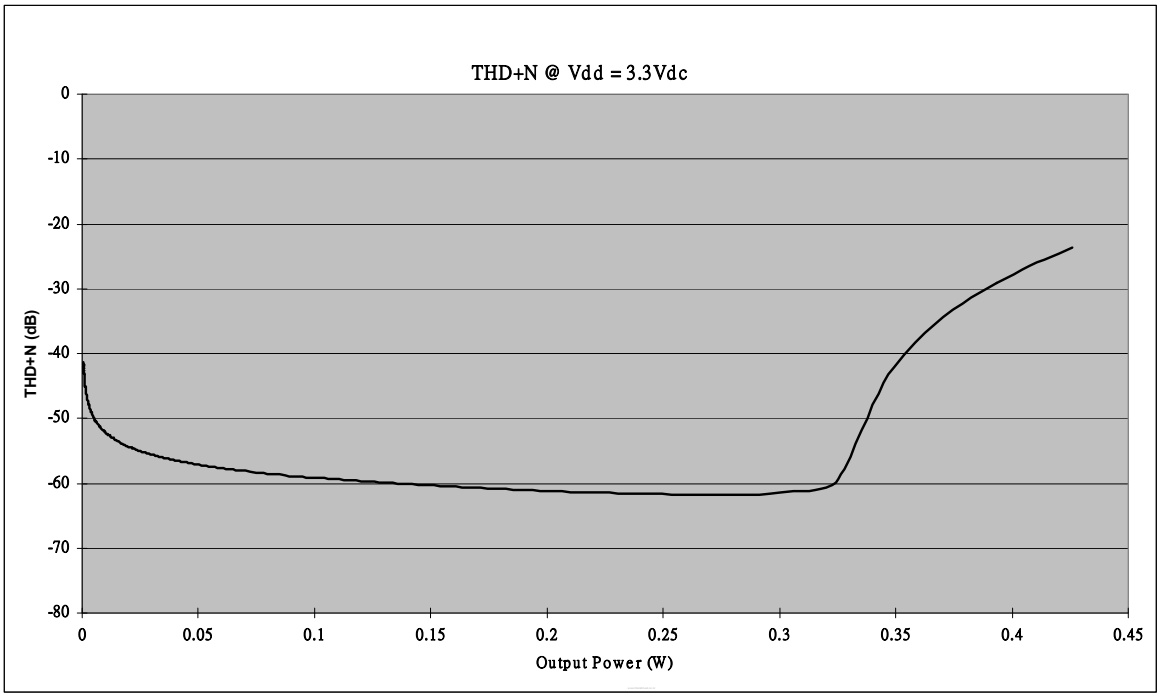
6.3.3 Total Harmonic Distortion Plus Noise VS. Output Power at 6.8Vdc and 5.0Vdc Supply Voltage with 8Ω Load

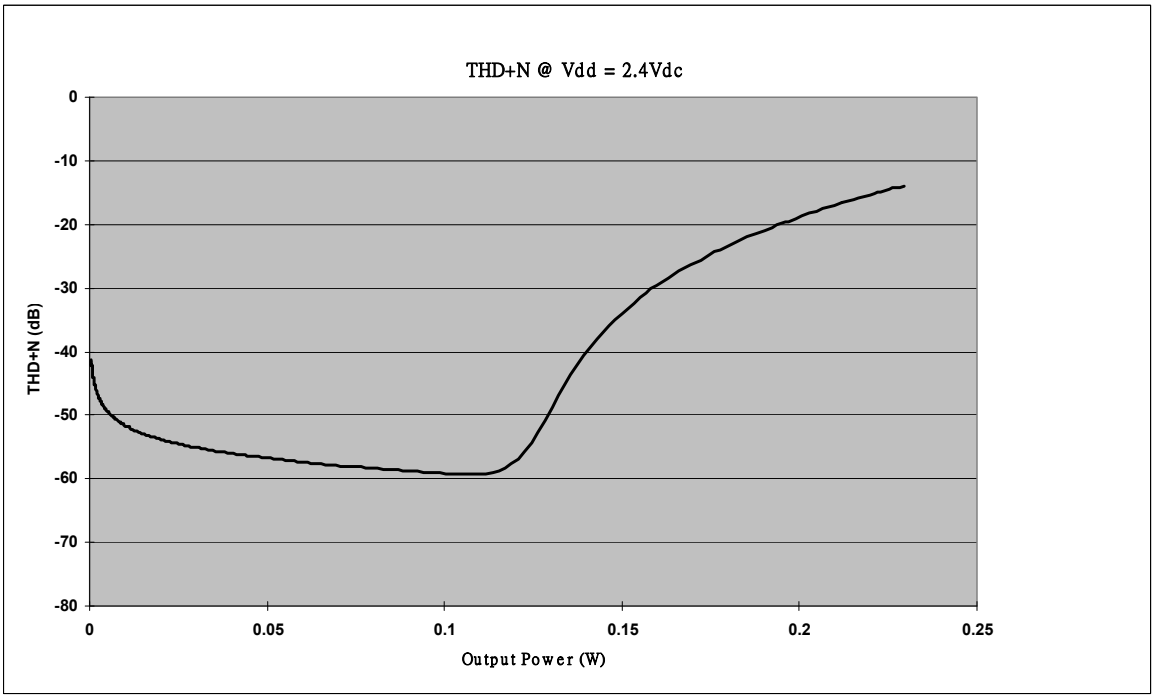




Conditions: THD+N measurement Bandwidth 22Hz to 22kHz at T_A=25°C

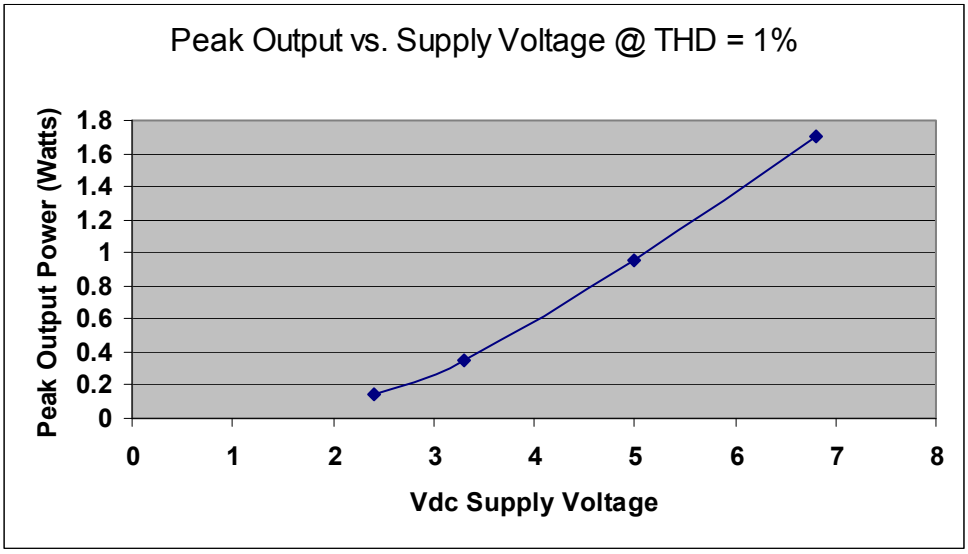
6.3.4 Total Harmonic Distortion Plus Noise VS. Output Power at 3.3Vdc and 2.4Vdc Supply Voltage with 8Ω Load





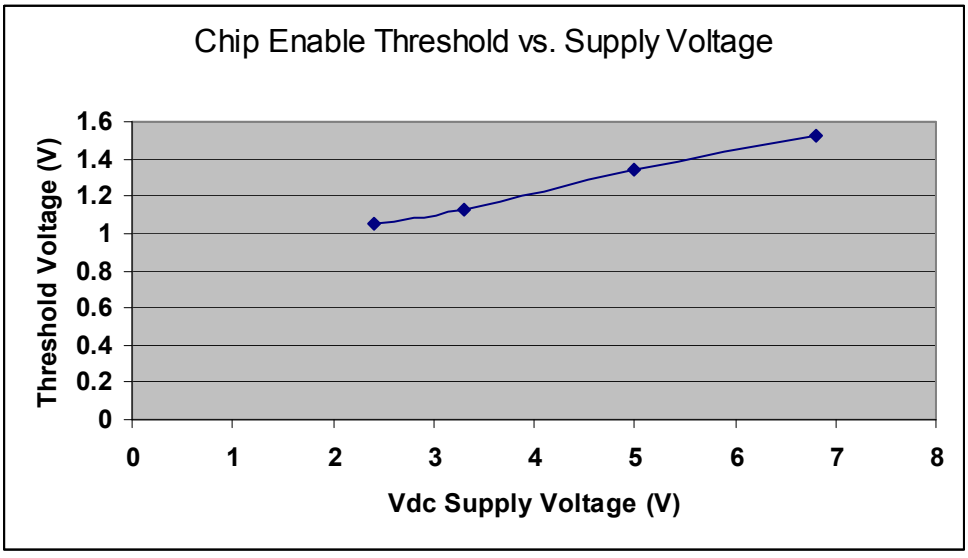
Conditions: THD+N measurement Bandwidth 22Hz to 22kHz at T_A=25°C

6.3.5 Typical Peak Output Power



Note: Peak output power becomes reduced as device becomes heated. Sustained medium duration heating typical for audio limits maximum useable output to approximately 1.5Wrms at less than 10% distortion.

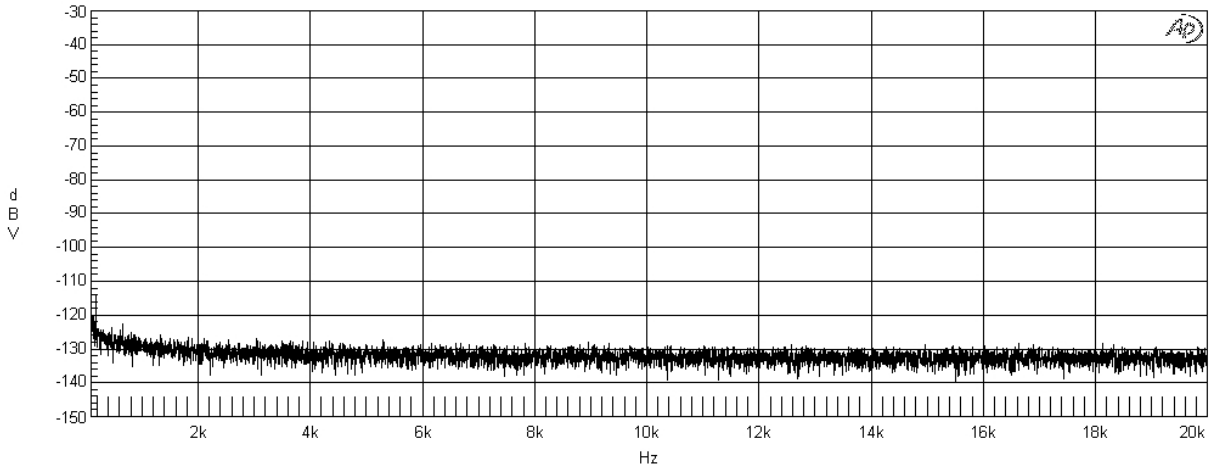
6.3.6 Chip Enable Threshold Voltage



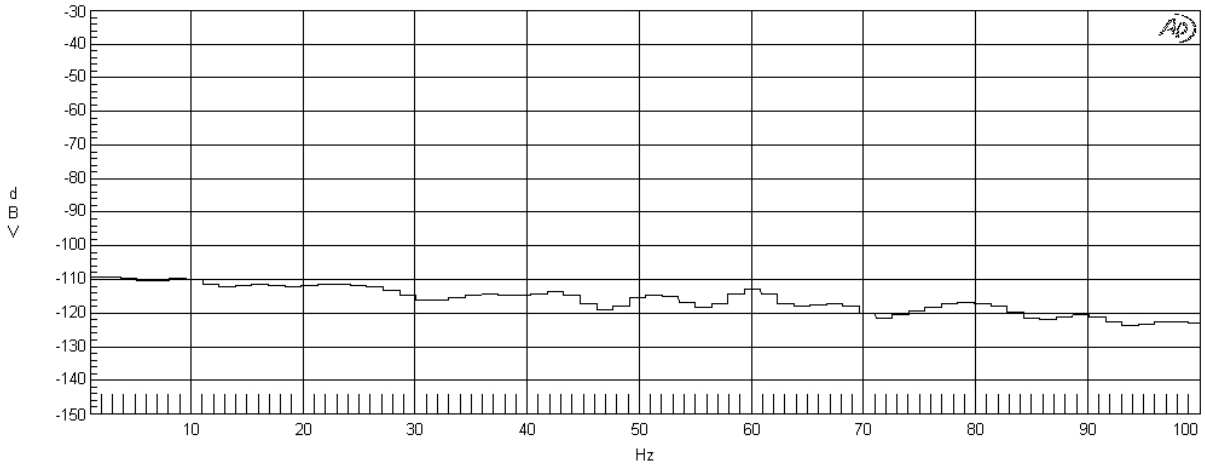
Conditions: T_A=25°C

6.3.7 Output Noise Spectrum

Noise spectrum at Vdd = 5.0Vdc, Gain = 0dB, BW<22kHz

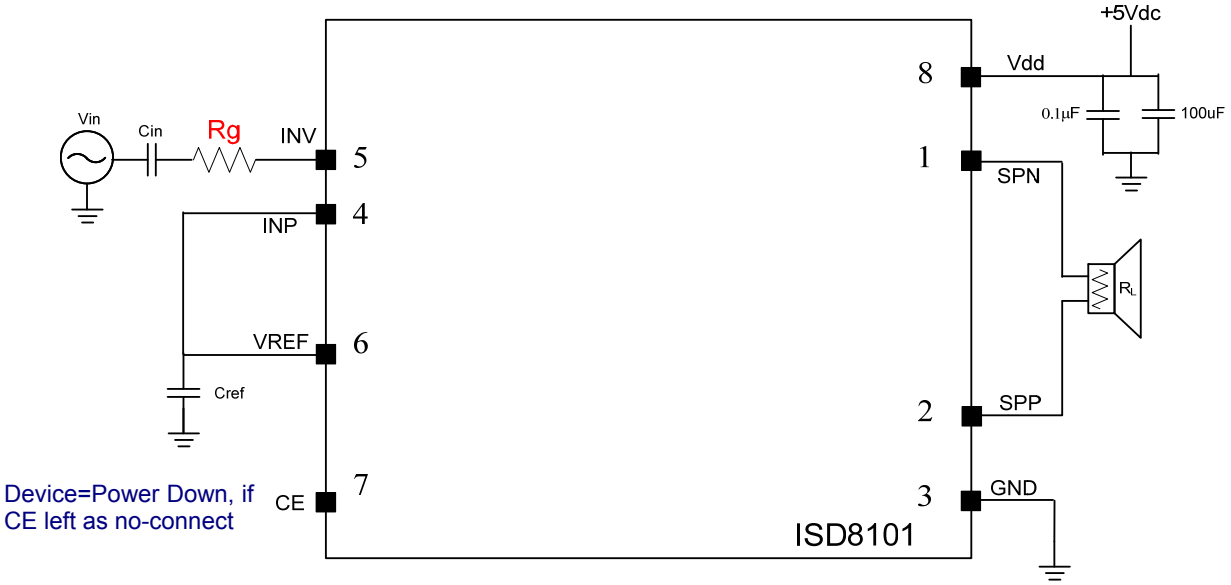


Noise Spectrum at Vdd = 5.0Vdc, Gain = 20dB, BW<22kHz



7 APPLICATION DIAGRAMS

7.1 SIMPLE GAIN SETTING



$$Differential\ Output\ Gain\ (SPP - SPN) = 2x\frac{50k}{5k + R_g}$$

By default: Rg = 0Ω,

ISD8101 Differential Output Gain = 20

ISD8101 Differential Output Gain (in dB) = 20 x log (20) = 26dB

Example: Rg = 45kΩ

ISD8101 Differential Output Gain = 2

ISD8101 Differential Output Gain (in dB) = 20 x log (2) = 6dB

7.2 SINGLE-ENDED ANALOG INPUT

The following application example is for reference. It is only to give a general idea of how to use the ISD8101. Each end-product design must be optimized in its own system for the best performance in terms of voice quality, power consumption, functionality, and other issues.

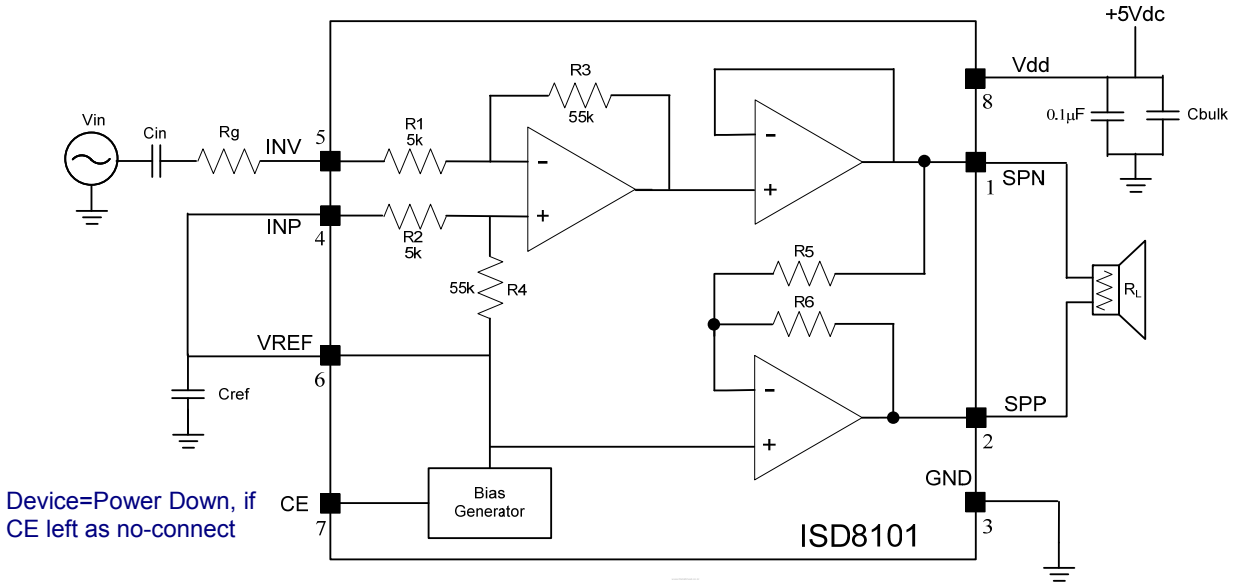


Figure 8-1 ISD8101 Application Diagram

DESIGN SUGGESTIONS

1.) Choose the desired Gain or amplification factor: G = R3/(R1+Rg) and then calculate the value for Rg = R3/G - R1 and use R1=5.5k-ohm and R3=55k-ohm.

2.) Choose the desired high pass frequency: Fc = 1/(6.28*Rin*Cin) and then calculate the value for Cin = 1/(6.28*Rin*Fc) and use Rin=Rg+R1 and Fc = high-pass frequency in Hz. Cin value is Farads. It is best to choose Cin as small as possible. This will minimize cost and any pop/click sound.

3.) Choose the value for Cref. Note that Cref does not generate any pop/click timing and that the main use for Cref is to filter any supply voltage noise. So, if the power supply noise is not a big concern, then Cref can be small. Typical values for Cref can be between 0.1uF and 10uF, and a recommended value for general applications is from 1uF to 4.7uF. In general, it is best if Cref is at least 3x larger in value than Cin. This can help minimize the first-time power-on pop noise. After the first-time power-on, the Cref value has no effect on pop/click performance.

4.) Choose the value for Cbulk. This value will depend on the both the physical layout (size and length of PCB traces/wires) and the power supply properties. The general suggestion for Cbulk is to choose it to be 100uF. If the power supply is far away or weak, then Cbulk may need to be a larger value. If the power supply is very close and has high current capacity, then it may be possible to use a smaller value for Cbulk. If Cbulk is too small, the system can be unstable and may oscillate.

7.3 DIFFERENTIAL INPUT FOR ANALOG OR PWM

The following application example is for reference, and is only to give a general idea how to use the ISD8101. Each end-product design must be optimized in its own system for the best performance on voice quality, power consumption, functionality, and all other issues.

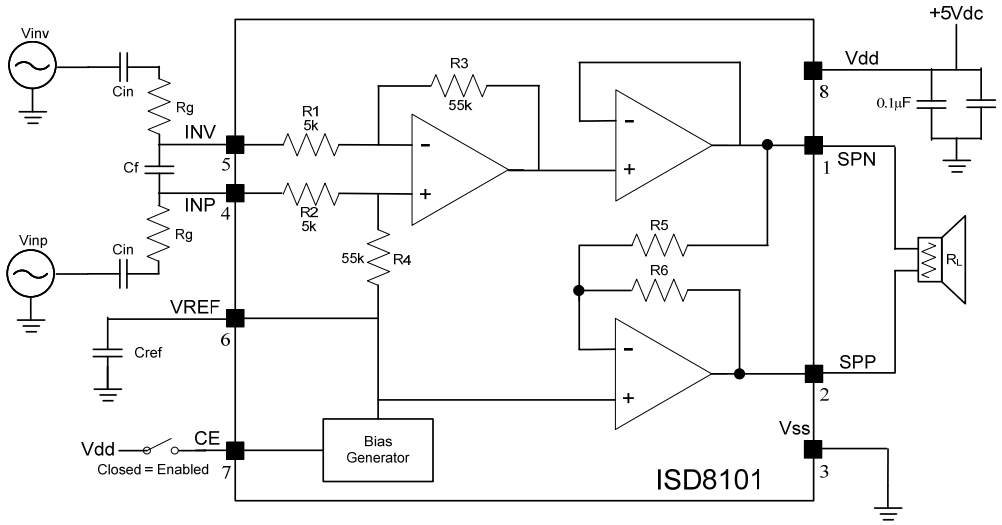


Figure 8-2 ISD8101 Application Diagram

DESIGN SUGGESTIONS

1.) Choose the desired Gain or amplification factor: G = R3/(R1+Rg) and then calculate the value for Rg = R3/G - R1 and use R1=5.5k-ohm and R3=55k-ohm. Both Rg parts should be the same value.

2.) Choose the desired low-pass frequency: Fc = 1/(6.28*Rin*Cf) and then calculate the resulting value for Cin = 1/(6.28*Rin*Fc), and use Rin=2Rg*R1/(Rg+R1), with Fc = low-pass frequency in Hz and the Cf value is Farads. For a PWM circuit, Fc should be about one-half the audio sample rate.

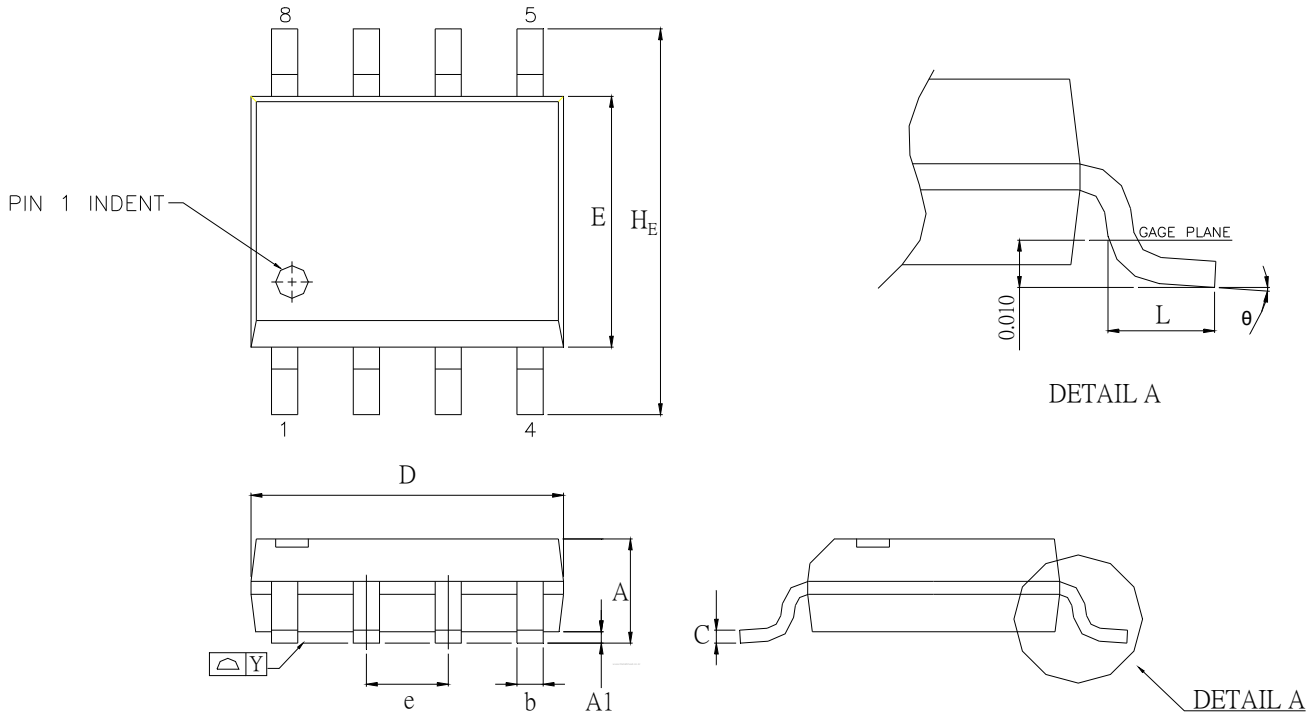
3.) Choose the desired high pass-frequency: Fc = 1/(6.28*Rin*Cin) and then calculate the value for Cin = 1/(6.28*Rin*Fc) and use Rin=Rg+R1 and Fc = high-pass frequency in Hz. Cin value is Farads. It is best to choose Cin as small as possible and both Cin parts should be the same value. This will minimize cost and any pop/click sound.

4.) Choose the value for Cref. Note that Cref does not generate any pop/click timing and that the main use for Cref is to filter any supply voltage noise. So, if the power supply noise is not a big concern, then Cref can be small. Typical values for Cref can be between 0.1uF and 10uF, and a recommended value for general applications is from 1uF to 4.7uF. In general, it is best if Cref is at least 3x larger in value than Cin. This can help minimize the first-time power-on pop noise. After the first-time power-on, the Cref value has no effect on pop/click performance.

5.) Choose the value for Cbulk. This value will depend on the both the physical layout (size and length of PCB traces/wires) and the power supply properties. The general suggestion for Cbulk is to choose it to be 100uF. If the power supply is far away or weak, then Cbulk may need to be a larger value. If the power supply is close and has high current capacity, then it may be possible to use a smaller value for Cbulk. If Cbulk is too small, the system can be unstable and may oscillate.

PACKAGE SPECIFICATION

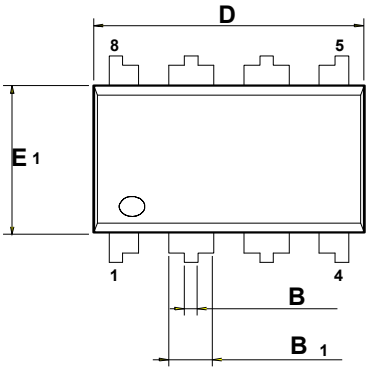
7.4 8 LEAD SOP- 8 (EX-PAD)

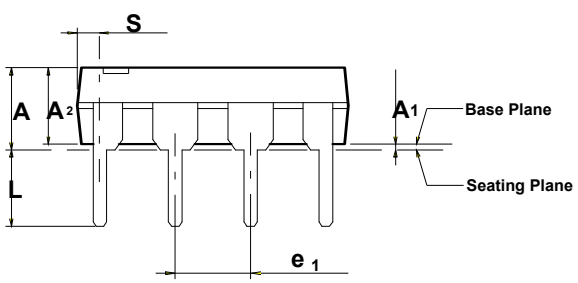


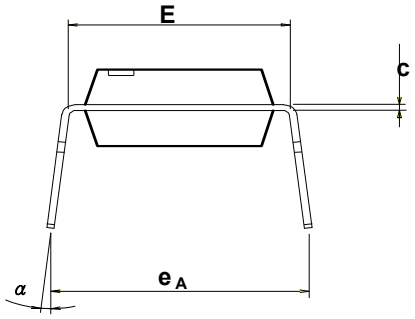
COTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.35	–	1.75	0.053	–	0.069
A1	0.05	–	0.15	0.002	–	0.006
b	0.33	–	0.51	0.013	–	0.020
C	0.19	–	0.25	0.008	–	0.010
D	4.8	–	5.00	0.188	–	0.196
E	3.8	–	4.0	0.150	–	0.157
e	1.27 BASIC			0.050 BASIC		
H_E	5.8	–	6.20	0.228	–	0.244
Y	–	–	0.10	–	–	0.004
L	0.40	–	1.27	0.016	–	0.050
θ	0°	–	10°	0°	–	10°

7.5 PDIP-8



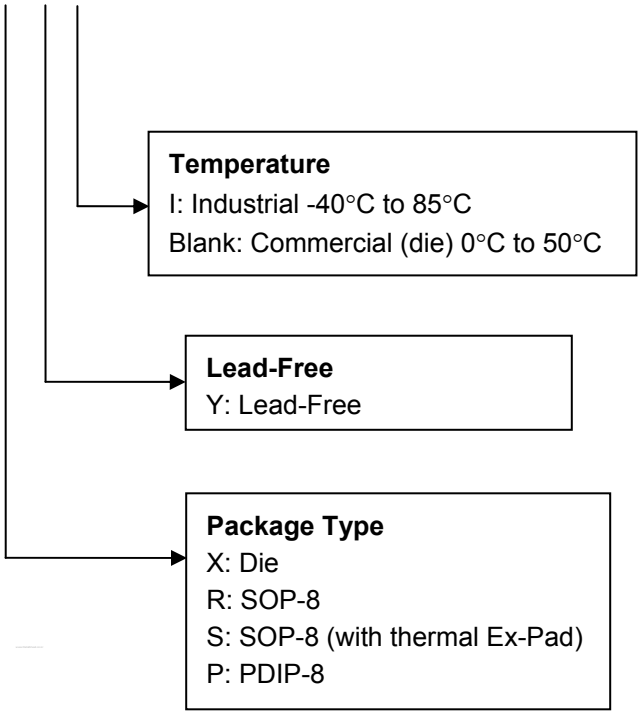




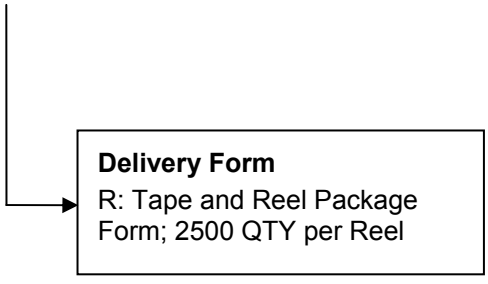
Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	0.175	—	—	4.45
A 1	0.010	—	—	0.25	—	—
A 2	0.125	0.130	0.135	3.18	3.30	3.43
B	0.016	0.018	0.022	0.41	0.46	0.56
B 1	0.058	0.060	0.064	1.47	1.52	1.63
c	0.008	0.010	0.014	0.20	0.25	0.36
D	—	0.360	0.380	—	9.14	9.65
E	0.290	0.300	0.310	7.37	7.62	7.87
E 1	0.245	0.250	0.255	6.22	6.35	6.48
e 1	0.090	0.100	0.110	2.29	2.54	2.79
L	0.120	0.130	0.140	3.05	3.30	3.56
α	0	—	15	0	—	15
e A	0.335	0.355	0.375	8.51	9.02	9.53
S	—	—	0.045	—	—	1.14

8 ORDERING INFORMATION

ISD8101 X Y I



ISD8101 S Y I R



9 REVISION HISTORY

Version	Date	Description
0.1	Dec, 2009	Initial draft
0.2	Dec. 20, 2009	Switched names on pin 1, 2
0.3	Jan. 15, 2010	Updated specs with values from initial testing
1.0	Mar. 10, 2010	Updated with full test results
1.1	Mar. 16, 2010	Modified to show preliminary status
1.2	Jun. 07, 2010	Added ordering option information
1.3	Jun. 28, 2010	Added instructions/equations for application schematics
1.4	Dec 30, 2010	Added the simple application schematic
1.5	Jan 31, 2011	Modified the application schematics
1.6	Jun 30, 2011	Update the format
1.7	Oct 20, 2011	Update the ordering information

Important Notice

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Insecure usage includes, but is not limited to: equipment for surgical implementation, atomic energy control instruments, airplane or spaceship instruments, the control or operation of dynamic, brake or safety systems designed for vehicular use, traffic signal instruments, all types of safety devices, and other applications intended to support or sustain life.

All Insecure Usage shall be made at customer's risk, and in the event that third parties lay claims to Nuvoton as a result of customer's Insecure Usage, customer shall indemnify the damages and liabilities thus incurred by Nuvoton.