

K61P256M120SF3

K61 Sub-Family Data Sheet

Supports the following:

MK61FX512VMJ12,
MK61FN1M0VMJ12

Features

- Operating Characteristics
 - Voltage range: 1.71 to 3.6 V
 - Flash write voltage range: 1.71 to 3.6 V
 - Temperature range (ambient): -40 to 105°C
- Performance
 - Up to 120 MHz ARM Cortex-M4 core with DSP instructions delivering 1.25 Dhrystone MIPS per MHz
- Memories and memory interfaces
 - Up to 1024 KB program flash memory on non-FlexMemory devices
 - Up to 512 KB program flash memory on FlexMemory devices
 - Up to 512 KB FlexNVM on FlexMemory devices
 - 16 KB FlexRAM on FlexMemory devices
 - Up to 128 KB RAM
 - Serial programming interface (EzPort)
 - FlexBus external bus interface
 - DDR controller interface
 - NAND flash controller interface
- Clocks
 - 3 to 32 MHz crystal oscillator
 - 32 kHz crystal oscillator
 - Multi-purpose clock generator
- System peripherals
 - 10 low-power modes to provide power optimization based on application requirements
 - Memory protection unit with multi-master protection
 - 32-channel DMA controller, supporting up to 128 request sources
 - External watchdog monitor
 - Software watchdog
 - Low-leakage wakeup unit
- Security and integrity modules
 - Hardware CRC module to support fast cyclic redundancy checks
 - Tamper detect and secure storage
 - Hardware random-number generator
 - Hardware encryption supporting DES, 3DES, AES, MD5, SHA-1, and SHA-256 algorithms
 - 128-bit unique identification (ID) number per chip
- Human-machine interface
 - Low-power hardware touch sensor interface (TSI)
 - General-purpose input/output
- Analog modules
 - Four 16-bit SAR ADCs
 - Programmable gain amplifier (PGA) (up to x64) integrated into each ADC
 - Two 12-bit DACs
 - Four analog comparators (CMP) containing a 6-bit DAC and programmable reference input
 - Voltage reference
- Timers
 - Programmable delay block
 - Two 8-channel motor control/general purpose/PWM timers
 - Two 2-channel quadrature decoder/general purpose timers
 - IEEE 1588 timers
 - Periodic interrupt timers
 - 16-bit low-power timer
 - Carrier modulator transmitter
 - Real-time clock

This document contains information on a new product. Specifications and information herein are subject to change without notice.

- Communication interfaces
 - Ethernet controller with MII and RMII interface to external PHY and hardware IEEE 1588 capability
 - USB high-/full-/low-speed On-the-Go controller with ULPI interface
 - USB full-/low-speed On-the-Go controller with on-chip transceiver
 - Two Controller Area Network (CAN) modules
 - Three SPI modules
 - Two I2C modules
 - Six UART modules
 - Secure Digital host controller (SDHC)
 - Two I2S modules

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1 Ordering parts

1.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to <http://www.freescale.com> and perform a part number search for the following device numbers: PK61 and MK61.

2 Part identification

2.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

2.2 Format

Part numbers for this device have the following format:

Q K## A M FFF T PP CC N

2.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Field	Description	Values
Q	Qualification status	<ul style="list-style-type: none"> M = Fully qualified, general market flow P = Prequalification
K##	Kinetis family	<ul style="list-style-type: none"> K61
A	Key attribute	<ul style="list-style-type: none"> D = Cortex-M4 w/ DSP F = Cortex-M4 w/ DSP and FPU
M	Flash memory type	<ul style="list-style-type: none"> N = Program flash only X = Program flash and FlexMemory

Table continues on the next page...

Terminology and guidelines

Field	Description	Values
FFF	Program flash memory size	<ul style="list-style-type: none">• 32 = 32 KB• 64 = 64 KB• 128 = 128 KB• 256 = 256 KB• 512 = 512 KB• 1M0 = 1 MB
T	Temperature range (°C)	<ul style="list-style-type: none">• V = -40 to 105• C = -40 to 85
PP	Package identifier	<ul style="list-style-type: none">• MJ = 256 MAPBGA (17 mm x 17 mm)
CC	Maximum CPU frequency (MHz)	<ul style="list-style-type: none">• 12 = 120 MHz
N	Packaging type	<ul style="list-style-type: none">• R = Tape and reel• (Blank) = Trays

2.4 Example

This is an example part number:

MK61FN1M0VMJ12

3 Terminology and guidelines

3.1 Definition: Operating requirement

An *operating requirement* is a specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip.

3.1.1 Example

This is an example of an operating requirement, which you must meet for the accompanying operating behaviors to be guaranteed:

Symbol	Description	Min.	Max.	Unit
V _{DD}	1.0 V core supply voltage	0.9	1.1	V

3.2 Definition: Operating behavior

An *operating behavior* is a specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions.

3.2.1 Example

This is an example of an operating behavior, which is guaranteed if you meet the accompanying operating requirements:

Symbol	Description	Min.	Max.	Unit
I _{WP}	Digital I/O weak pullup/ pulldown current	10	130	μA

3.3 Definition: Attribute

An *attribute* is a specified value or range of values for a technical characteristic that are guaranteed, regardless of whether you meet the operating requirements.

3.3.1 Example

This is an example of an attribute:

Symbol	Description	Min.	Max.	Unit
CIN_D	Input capacitance: digital pins	—	7	pF

3.4 Definition: Rating

A *rating* is a minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:

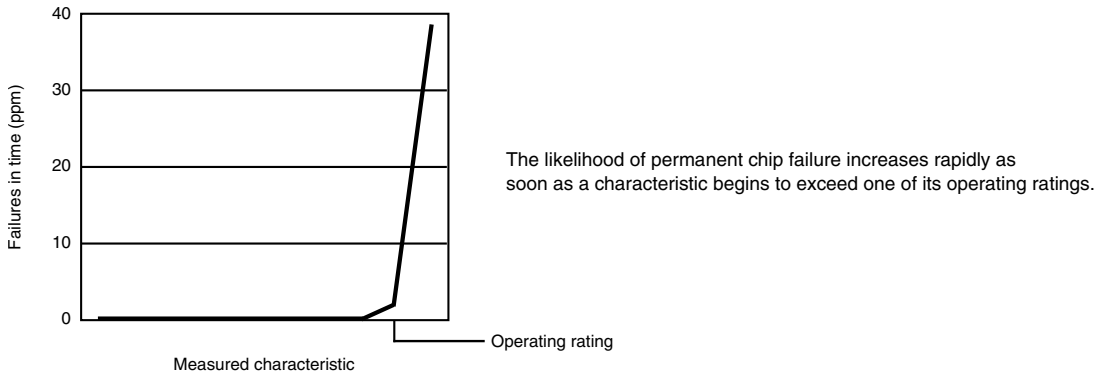
- *Operating ratings* apply during operation of the chip.
- *Handling ratings* apply when the chip is not powered.

3.4.1 Example

This is an example of an operating rating:

Symbol	Description	Min.	Max.	Unit
V _{DD}	1.0 V core supply voltage	-0.3	1.2	V

3.5 Result of exceeding a rating



3.6 Relationship between ratings and operating requirements

Fatal range - Probable permanent failure	Limited operating range - No permanent failure - Possible decreased life - Possible incorrect operation	Normal operating range - No permanent failure - Correct operation	Limited operating range - No permanent failure - Possible decreased life - Possible incorrect operation	Fatal range - Probable permanent failure
Handling range - No permanent failure				

Operating or handling rating (min.) *Operating requirement (min.)* *Operating requirement (max.)* *Operating or handling rating (max.)*

3.7 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip’s ratings.

- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

3.8 Definition: Typical value

A *typical value* is a specified value for a technical characteristic that:

- Lies within the range of values specified by the operating behavior
- Given the typical manufacturing process, is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions

Typical values are provided as design guidelines and are neither tested nor guaranteed.

3.8.1 Example 1

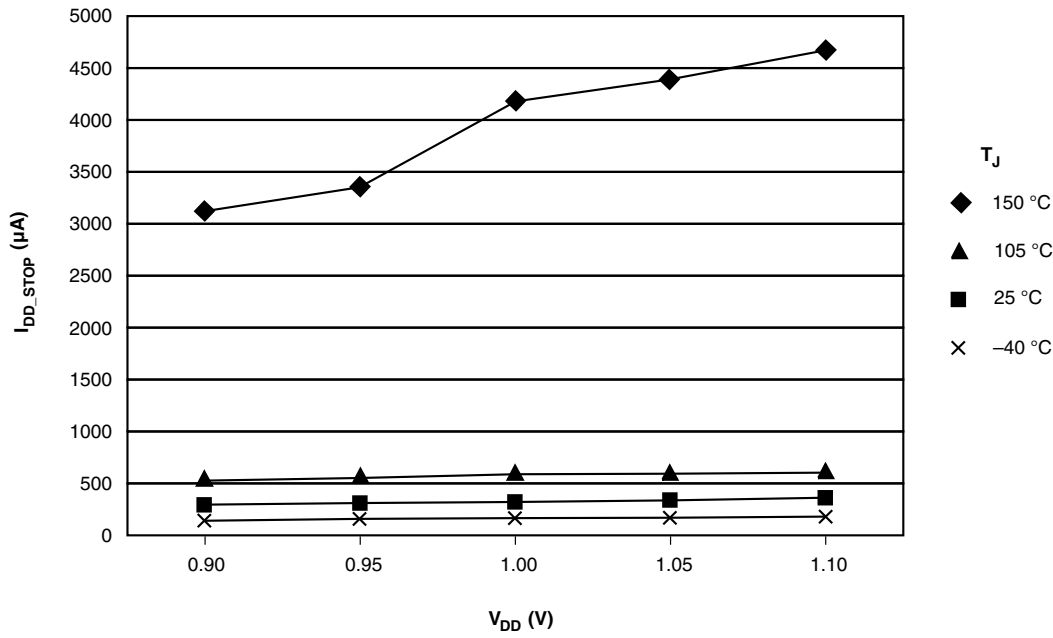
This is an example of an operating behavior that includes a typical value:

Symbol	Description	Min.	Typ.	Max.	Unit
I_{WP}	Digital I/O weak pullup/pulldown current	10	70	130	μA

3.8.2 Example 2

This is an example of a chart that shows typical values for various voltage and temperature conditions:

Ratings



3.9 Typical value conditions

Typical values assume you meet the following conditions (or other conditions as specified):

Symbol	Description	Value	Unit
T _A	Ambient temperature	25	°C
V _{DD}	3.3 V supply voltage	3.3	V

4 Ratings

4.1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T _{STG}	Storage temperature	-55	150	°C	1
T _{SDR}	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

4.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

4.3 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V _{HBM}	Electrostatic discharge voltage, human body model	-2000	+2000	V	1
V _{CDM}	Electrostatic discharge voltage, charged-device model	-500	+500	V	2
I _{LAT}	Latch-up current at ambient temperature of 105°C	-100	+100	mA	

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.

4.4 Voltage and current operating ratings

Symbol	Description	Min.	Max.	Unit
V _{DD}	Digital supply voltage ¹	-0.3	3.8	V
V _{DD_INT}	Core supply voltage	-0.3	3.8	V
V _{DD_DDR}	DDR I/O supply voltage	-0.3	3.8	V
I _{DD}	Digital supply current	—	300	mA
I _{DD_INT}	Core supply current	—	185	mA
I _{DD_DDR}	DDR supply current	—	220	mA
V _{DIO}	Digital input voltage (except RESET, EXTAL0/XTAL0, and EXTAL1/XTAL1) ²	-0.3	5.5	V
V _{DTamper}	Tamper input voltage	-0.3	V _{BAT} + 0.3	V
V _{DDDR}	DDR input voltage	-0.3	V _{DD_DDR} + 0.3	V
V _{AIO}	Analog ³ , RESET, EXTAL0/XTAL0, and EXTAL1/XTAL1 input voltage	-0.3	V _{DD} + 0.3	V

Table continues on the next page...

General

Symbol	Description	Min.	Max.	Unit
I_D	Instantaneous maximum current single pin limit (applies to all digital pins except Tamper and DDR pins)	-25	25	mA
I_{D_DDR}	Instantaneous maximum current single pin limit (applies to DDR pins)	TBD	TBD	mA
I_{D_Tamper}	Instantaneous maximum current single pin limit (applies to Tamper pins)	TBD	TBD	mA
V_{DDA}	Analog supply voltage	$V_{DD} - 0.3$	$V_{DD} + 0.3$	V
V_{USB_DP}	USB_DP input voltage	-0.3	3.63	V
V_{USB_DM}	USB_DM input voltage	-0.3	3.63	V
VREGIN	USB regulator input	-0.3	6.0	V
V_{BAT}	RTC battery supply voltage	-0.3	3.8	V

1. It applies for all port pins except Tamper pins.
2. It covers digital pins except Tamper pins and DDR pins.
3. Analog pins are defined as pins that do not have an associated general purpose I/O port function.

5 General

5.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.

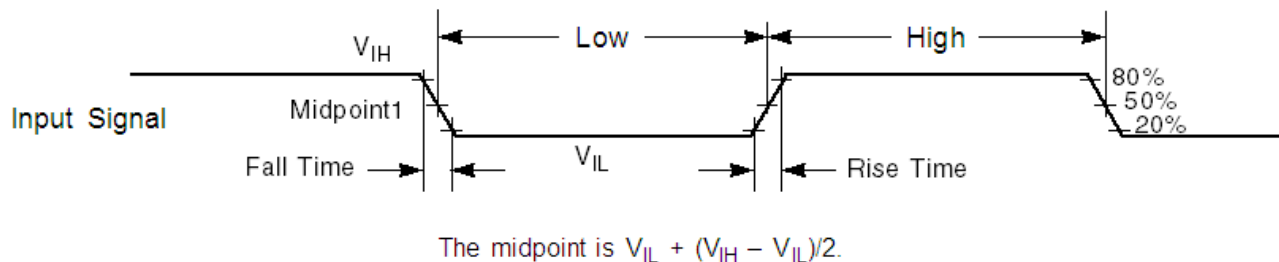


Figure 1. Input signal measurement reference

All digital I/O switching characteristics assume:

1. output pins
 - have $C_L=30\text{pF}$ loads,
 - are configured for fast slew rate ($\text{PORTx_PCRn[SRE]}=0$), and
 - are configured for high drive strength ($\text{PORTx_PCRn[DSE]}=1$)
2. input pins
 - have their passive filter disabled ($\text{PORTx_PCRn[PFE]}=0$)

5.2 Nonswitching electrical specifications

5.2.1 Voltage and current operating requirements

Table 1. Voltage and current operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DD}	Supply voltage	$\max(V_{DD_DD}, 1.71)$	3.6	V	
V_{DD_INT}	Core supply voltage	1.71	V_{DD}	V	
V_{DD_DDR}	DDR voltage — memory I/O buffers <ul style="list-style-type: none"> • DDR1 • DDR2/LPDDR 	2.3 1.7	2.7 1.9	V V	
V_{REF_DDR}	Input reference voltage (DDR1/DDR2)	$0.49 \times V_{DD_DDR}$	$0.51 \times V_{DD_DDR}$	V	
V_{DDA}	Analog supply voltage	1.71	3.6	V	
$V_{DD} - V_{DDA}$	V_{DD} -to- V_{DDA} differential voltage	-0.1	0.1	V	
$V_{SS} - V_{SSA}$	V_{SS} -to- V_{SSA} differential voltage	-0.1	0.1	V	
V_{BAT}	RTC battery supply voltage	1.71	3.6	V	
V_{IH}	Input high voltage (digital pins except Tamper pins and DDR pins) <ul style="list-style-type: none"> • $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ • $1.7\text{ V} \leq V_{DD} \leq 2.7\text{ V}$ 	$0.7 \times V_{DD}$ $0.75 \times V_{DD}$	— —	V V	
V_{IL}	Input low voltage (digital pins except Tamper pins and DDR pins) <ul style="list-style-type: none"> • $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ • $1.7\text{ V} \leq V_{DD} \leq 2.7\text{ V}$ 	— —	$0.35 \times V_{DD}$ $0.3 \times V_{DD}$	V V	
V_{IH_DDR}	Input high voltage (DDR pins) <ul style="list-style-type: none"> • DDR1 • DDR2 • LPDDR 	$V_{REF_DDR} + 0.15$ $V_{REF_DDR} + 0.125$ $0.7 \times V_{DD_DDR}$	— — —	V V V	

Table continues on the next page...

Table 1. Voltage and current operating requirements (continued)

Symbol	Description	Min.	Max.	Unit	Notes
V _{IL_DDR}	Input low voltage (DDR pins) <ul style="list-style-type: none"> • DDR1 • DDR2 • LPDDR 	—	V _{REF_DDR} - 0.15	V	
		—		V	
		—	V _{REF_DDR} - 0.125	V	
		—	0.3 × V _{DD_DDR}	V	
V _{IH_Tamper}	Tamper input high voltage <ul style="list-style-type: none"> • 2.7 V ≤ V_{BAT} ≤ 3.6 V • 1.7 V ≤ V_{BAT} ≤ 2.7 V 	0.7 × V _{BAT}	—	V	
		0.75 × V _{BAT}	—	V	
V _{IL_Tamper}	Tamper input low voltage <ul style="list-style-type: none"> • 2.7 V ≤ V_{BAT} ≤ 3.6 V • 1.7 V ≤ V_{BAT} ≤ 2.7 V 	—	0.35 × V _{BAT}	V	
		—	0.3 × V _{BAT}	V	
V _{HYS}	Input hysteresis (digital pins except Tamper pins and DDR pins)	0.06 × V _{DD}	—	V	
V _{HYS_Tamper}	Input hysteresis (Tamper pins)	0.06 × V _{BAT}	—	V	
I _{ICDIO}	Digital pin (except Tamper pins and DDR pins) negative DC injection current — single pin <ul style="list-style-type: none"> • V_{IN} < V_{SS}-0.3V 	-5	—	mA	1
I _{ICDIO_DDR}	DDR pin negative DC injection current -- single pin <ul style="list-style-type: none"> • TBD 	TBD	TBD	mA	
I _{ICDIO_Tamper}	Tamper pin negative DC injection current — single pin <ul style="list-style-type: none"> • V_{IN} < V_{SS}-0.3V • V_{IN} > V_{BAT} 	-0.2	—	mA	
		—	2.0	mA	
I _{ICAIO}	Analog ² , EXTAL0/XTAL0, and EXTAL1/XTAL1 pin DC injection current — single pin <ul style="list-style-type: none"> • V_{IN} < V_{SS}-0.3V (Negative current injection) • V_{IN} > V_{DD}+0.3V (Positive current injection) 	-5	—	mA	3
		—	+5		
I _{ICcont}	Contiguous pin DC injection current —regional limit, includes sum of negative injection currents or sum of positive injection currents of 16 contiguous pins <ul style="list-style-type: none"> • Negative current injection • Positive current injection 	-25	—	mA	
		—	+25		
V _{RAM}	V _{DD} (V _{DD_INT}) voltage required to retain RAM	1.2	—	V	
V _{REFVAT}	V _{BAT} voltage required to retain the VBAT register file	V _{POR_VBAT}	—	V	

1. All 5 V tolerant digital I/O pins are internally clamped to V_{SS} through a ESD protection diode. There is no diode connection to V_{DD}. If V_{IN} greater than V_{DIO_MIN} (=V_{SS}-0.3V) is observed, then there is no need to provide current limiting resistors at

the pads. If this limit cannot be observed then a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as $R=(V_{DIO_MIN}-V_{IN})/|I_{IC}|$.

- Analog pins are defined as pins that do not have an associated general purpose I/O port function.
- All analog pins are internally clamped to V_{SS} and V_{DD} through ESD protection diodes. If V_{IN} is greater than V_{AIO_MIN} ($=V_{SS}-0.3V$) and V_{IN} is less than V_{AIO_MAX} ($=V_{DD}+0.3V$) is observed, then there is no need to provide current limiting resistors at the pads. If these limits cannot be observed then a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as $R=(V_{AIO_MIN}-V_{IN})/|I_{IC}|$. The positive injection current limiting resistor is calculated as $R=(V_{IN}-V_{AIO_MAX})/|I_{IC}|$. Select the larger of these two calculated resistances.

5.2.2 LVD and POR operating requirements

Table 2. LVD and POR operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{POR}	Falling VDD POR detect voltage	0.8	1.1	1.5	V	
V_{LVDH}	Falling low-voltage detect threshold — high range (LVDV=01)	2.48	2.56	2.64	V	
V_{LVW1H}	Low-voltage warning thresholds — high range <ul style="list-style-type: none"> Level 1 falling (LVWV=00) Level 2 falling (LVWV=01) Level 3 falling (LVWV=10) Level 4 falling (LVWV=11) 	2.62	2.70	2.78	V	1
V_{LVW2H}		2.72	2.80	2.88	V	
V_{LVW3H}		2.82	2.90	2.98	V	
V_{LVW4H}		2.92	3.00	3.08	V	
V_{HYSH}	Low-voltage inhibit reset/recover hysteresis — high range	—	±80	—	mV	
V_{LVDL}	Falling low-voltage detect threshold — low range (LVDV=00)	1.54	1.60	1.66	V	
V_{LVW1L}	Low-voltage warning thresholds — low range <ul style="list-style-type: none"> Level 1 falling (LVWV=00) Level 2 falling (LVWV=01) Level 3 falling (LVWV=10) Level 4 falling (LVWV=11) 	1.74	1.80	1.86	V	1
V_{LVW2L}		1.84	1.90	1.96	V	
V_{LVW3L}		1.94	2.00	2.06	V	
V_{LVW4L}		2.04	2.10	2.16	V	
V_{HYSL}	Low-voltage inhibit reset/recover hysteresis — low range	—	±60	—	mV	
V_{BG}	Bandgap voltage reference	0.97	1.00	1.03	V	
t_{LPO}	Internal low power oscillator period factory trimmed	900	1000	1100	µs	

- Rising thresholds are falling threshold + hysteresis voltage

Table 3. VBAT power operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{POR_VBAT}	Falling VBAT supply POR detect voltage	0.8	1.1	1.5	V	

5.2.3 Voltage and current operating behaviors

Table 4. Voltage and current operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
V_{OH}	Output high voltage — high drive strength				
	• $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$, $I_{OH} = -9\text{mA}$	$V_{DD} - 0.5$	—	V	
	• $1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}$, $I_{OH} = -3\text{mA}$	$V_{DD} - 0.5$	—	V	
	Output high voltage — low drive strength				
V_{OH_DDR}	Output high voltage for DDR pins				
	• DDR1 ($I_{OH} = -16.2\text{ mA}$)	$V_{DD_DDR} - 0.36$	—	V	
	• DDR2 half strength ($I_{OH} = \text{TBD mA}$)	$V_{DD_DDR} - 0.28$	—	V	
	• DDR2 full strength ($I_{OH} = -13.4\text{ mA}$)	$V_{DD_DDR} - 0.28$	—	V	
I_{OHT}	Output high current total for all ports	—	100	mA	
	• LPDDR half strength ($I_{OH} = -0.1\text{ mA}$)	$0.9 \times V_{DD_DDR}$	—	V	
		$0.9 \times V_{DD_DDR}$	—	V	
	• LPDDR full strength ($I_{OH} = -0.1\text{ mA}$)	$0.9 \times V_{DD_DDR}$	—	V	
I_{OHT_io60}	Output high current total for fast digital ports	—	100	mA	
I_{OHT_DDR}	Output high current total for DDR pins	—	TBD	mA	
V_{OH_Tamper}	Output high voltage — high drive strength				
	• $2.7\text{ V} \leq V_{BAT} \leq 3.6\text{ V}$, $I_{OH} = -10\text{mA}$	$V_{BAT} - 0.5$	—	V	
	• $1.71\text{ V} \leq V_{BAT} \leq 2.7\text{ V}$, $I_{OH} = -3\text{mA}$	$V_{BAT} - 0.5$	—	V	
	Output high voltage — low drive strength				
I_{OH_Tamper}	Output high current total for Tamper pins	—	TBD	mA	
	• $2.7\text{ V} \leq V_{BAT} \leq 3.6\text{ V}$, $I_{OH} = -2\text{mA}$	$V_{BAT} - 0.5$	—	V	
	• $1.71\text{ V} \leq V_{BAT} \leq 2.7\text{ V}$, $I_{OH} = -0.6\text{mA}$	$V_{BAT} - 0.5$	—	V	

Table continues on the next page...

Table 4. Voltage and current operating behaviors (continued)

Symbol	Description	Min.	Max.	Unit	Notes
V _{OL}	Output low voltage — high drive strength				
	• 2.7 V ≤ V _{DD} ≤ 3.6 V, I _{OL} = 9mA	—	0.5	V	
	• 1.71 V ≤ V _{DD} ≤ 2.7 V, I _{OL} = 3mA	—	0.5	V	
	Output low voltage — low drive strength				
I _{OLT}	Output low current total for all ports	—	TBD	mA	
	Output low current total for fast digital ports	—	TBD	mA	
	Output low voltage for DDR pins				
	• DDR1 (I _{OL} = 16.2 mA)	—	0.37	V	
V _{OL_DDR}	• DDR2 half strength (I _{OL} = TBD mA)	—	0.28	V	
	• DDR2 full strength (I _{OL} = 13.4 mA)	—	0.28	V	
	• LPDDR half strength (I _{OL} = 0.1 mA)	—	0.1 x	V	
	• LPDDR full strength (I _{OL} = 0.1 mA)	—	V _{DD_DDR}	V	
		—	0.1 x	V	
	—	V _{DD_DDR}	V		
I _{OLT_DDR}	Output low current total for DDR pins	—	TBD	mA	
V _{OL_Tamper}	• DDR1				
	• DDR2				
	• LPDDR				
	Output low voltage — high drive strength				
I _{OL_Tamper}	• 2.7 V ≤ V _{BAT} ≤ 3.6 V, I _{OL} = 10mA	—	0.5	V	
	• 1.71 V ≤ V _{BAT} ≤ 2.7 V, I _{OL} = 3mA	—	0.5	V	
	Output low voltage — low drive strength				
	• 2.7 V ≤ V _{BAT} ≤ 3.6 V, I _{OL} = 2mA	—	0.5	V	
I _{IN}	• 1.71 V ≤ V _{BAT} ≤ 2.7 V, I _{OL} = 0.6mA	—	0.5	V	
	Output low current total for Tamper pins	—	TBD	mA	
I _{IN}	Input leakage current (per pin) for full temperature range	—	1	μA	1
I _{IN}	Input leakage current (per pin) at 25°C	—	0.025	μA	1
I _{IN_DDR}	Input leakage current (per DDR pin) for full temperature range	—	1	μA	
I _{IN_DDR}	Input leakage current (per DDR pin) at 25°C	—	0.025	μA	
I _{IN_Tamper}	Input leakage current (per Tamper pin) for full temperature range	—	TBD	μA	
I _{IN_Tamper}	Input leakage current (per Tamper pin) at 25°C	—	0.025	μA	

Table continues on the next page...

Table 4. Voltage and current operating behaviors (continued)

Symbol	Description	Min.	Max.	Unit	Notes
I_{OZ}	Hi-Z (off-state) leakage current (per pin)	—	1	μA	
I_{OZ_DDR}	Hi-Z (off-state) leakage current (per DDR pin)	—	1	μA	
I_{OZ_Tamper}	Hi-Z (off-state) leakage current (per Tamper pin)	—	1	μA	
R_{PU}	Internal pullup resistors	20	50	$\text{k}\Omega$	2
R_{PD}	Internal pulldown resistors	20	50	$\text{k}\Omega$	3
R_{PU_Tamper}	Internal pullup resistors (per Tamper pin)	20	50	$\text{k}\Omega$	
R_{PD_Tamper}	Internal pulldown resistors (per Tamper pin)	20	50	$\text{k}\Omega$	
R_{ODT}	On-die termination (ODT) resistance for DDR2 <ul style="list-style-type: none"> • $R_{tt1(\text{eff})} - 75 \Omega$ • $R_{tt2(\text{eff})} - 150 \Omega$ 	60 120	90 180	Ω Ω	

1. Measured at $V_{DD}=3.6\text{V}$
2. Measured at V_{DD} supply voltage = V_{DD} min and $V_{\text{input}} = V_{SS}$
3. Measured at V_{DD} supply voltage = V_{DD} min and $V_{\text{input}} = V_{DD}$

5.2.4 Power mode transition operating behaviors

All specifications except t_{POR} , and $V_{LLSx} \rightarrow \text{RUN}$ recovery times in the following table assume this clock configuration:

- CPU and system clocks = FEI 100 MHz
- Bus clock = 50 MHz
- FlexBus clock = 50 MHz
- Flash clock = 25 MHz

Table 5. Power mode transition operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
t_{POR}	After a POR event, amount of time from the point V_{DD} reaches 1.71 V to execution of the first instruction across the operating temperature range of the chip.	—	300	μs	1
	• $V_{LLS1} \rightarrow \text{RUN}$	—	126	μs	
	• $V_{LLS2} \rightarrow \text{RUN}$	—	82	μs	
	• $V_{LLS3} \rightarrow \text{RUN}$	—	82	μs	
	• $\text{LLS} \rightarrow \text{RUN}$	—	5.0	μs	

Table continues on the next page...

Table 5. Power mode transition operating behaviors (continued)

Symbol	Description	Min.	Max.	Unit	Notes
	• VLPS → RUN	—	TBD	μs	
	• STOP → RUN	—	TBD	μs	

1. Normal boot (FTFE_FOFT[LPBOOT]=1)

5.2.5 Power consumption operating behaviors

Table 6. Power consumption operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I _{DDA}	Analog supply current	—	—	See note	mA	1
I _{DD_RUN}	Run mode current — all peripheral clocks disabled, code executing from flash	—	65	TBD	mA	2
	• @ 1.8V	—	65	TBD	mA	
	• @ 3.0V					
I _{DD_RUN}	Run mode current — all peripheral clocks enabled, code executing from flash	—	95	TBD	mA	3
	• @ 1.8V	—	95	TBD	mA	
	• @ 3.0V					
I _{DD_WAIT}	Wait mode high frequency current at 3.0 V — all peripheral clocks disabled	—	37	TBD	mA	2
I _{DD_WAIT}	Wait mode reduced frequency current at 3.0 V — all peripheral clocks disabled	—	21	TBD	mA	4
I _{DD_STOP}	Stop mode current at 3.0 V	—	TBD	TBD	mA	
	• @ -40 to 25°C	—	TBD	TBD	mA	
	• @ 70°C	—	TBD	TBD	mA	
	• @ 105°C	—	TBD	TBD	mA	
I _{DD_VLPR}	Very-low-power run mode current at 3.0 V — all peripheral clocks disabled	—	2.3	TBD	mA	5
I _{DD_VLPR}	Very-low-power run mode current at 3.0 V — all peripheral clocks enabled	—	3.1	TBD	mA	6
I _{DD_VLPW}	Very-low-power wait mode current at 3.0 V	—	1.8	TBD	mA	7
I _{DD_VLPS}	Very-low-power stop mode current at 3.0 V	—	200	TBD	μA	
	• @ -40 to 25°C	—	TBD	TBD	μA	
	• @ 70°C	—	TBD	TBD	μA	
	• @ 105°C	—	TBD	TBD	μA	

Table continues on the next page...

Table 6. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I _{DD_ULLS}	Low leakage stop mode current at 3.0 V	—	200	TBD	μA	8
	• @ -40 to 25°C	—	TBD	TBD	μA	
	• @ 70°C	—	TBD	TBD	μA	
	• @ 105°C	—	TBD	TBD	μA	
I _{DD_VLLS3}	Very low-leakage stop mode 3 current at 3.0 V	—	6.5	TBD	μA	#new-reference/ llsramn
	• @ -40 to 25°C	—	37.4	TBD	μA	
	• @ 70°C	—	148.3	TBD	μA	
	• @ 105°C	—				
I _{DD_VLLS2}	Very low-leakage stop mode 2 current at 3.0 V	—	3.4	TBD	μA	
	• @ -40 to 25°C	—	13.4	TBD	μA	
	• @ 70°C	—	58.5	TBD	μA	
	• @ 105°C	—				
I _{DD_VLLS1}	Very low-leakage stop mode 1 current at 3.0 V	—	2.9	TBD	μA	
	• @ -40 to 25°C	—	9.8	TBD	μA	
	• @ 70°C	—	44.7	TBD	μA	
	• @ 105°C	—				
I _{DD_VBAT}	Average current when CPU is not accessing RTC registers at 3.0 V	—	0.91	1.1	μA	9
	• @ -40 to 25°C	—	1.5	1.85	μA	
	• @ 70°C	—	4.3	4.3	μA	
	• @ 105°C	—				

1. The analog supply current is the sum of the active or disabled current for each of the analog modules on the device. See each module's specification for its supply current.
2. 120 MHz core and system clock, 60 MHz bus, 30 MHz FlexBus clock, and 20 MHz flash clock. MCG configured for PEE mode. All peripheral clocks disabled.
3. 120 MHz core and system clock, 60 MHz bus, 50 MHz FlexBus clock, and 20 MHz flash clock. MCG configured for PEE mode. All peripheral clocks enabled, but peripherals are not in active operation.
4. 25 MHz core and system clock, 25 MHz bus clock, and 12.5 MHz FlexBus and flash clock. MCG configured for FEI mode.
5. 4 MHz core, system, 2 MHz FlexBus, and 2 MHz bus clock and 1 MHz flash clock. MCG configured for BLPE mode. All peripheral clocks disabled.
6. 4 MHz core, system, 2 MHz FlexBus, and 2 MHz bus clock and 1 MHz flash clock. MCG configured for BLPE mode. All peripheral clocks disabled.
7. 4 MHz core, system, 2 MHz FlexBus, and 2 MHz bus clock and 1 MHz flash clock. MCG configured for BLPE mode. All peripheral clocks disabled.
8. Data reflects devices with 128 KB of RAM. For devices with 64 KB of RAM, power consumption is reduced by 2 μA.
9. Includes 32kHz oscillator current and RTC operation.

5.2.5.1 Diagram: Typical IDD_RUN operating behavior

The following data was measured under these conditions:

- MCG in FBE mode for 50 MHz and lower frequencies. MCG in FEE mode at greater than 50 MHz frequencies. MCG in PEE mode is greater than 100 MHz frequencies.
- USB regulator disabled
- No GPIOs toggled
- Code execution from flash with cache enabled
- For the ALLOFF curve, all peripheral clocks are disabled except FTFL

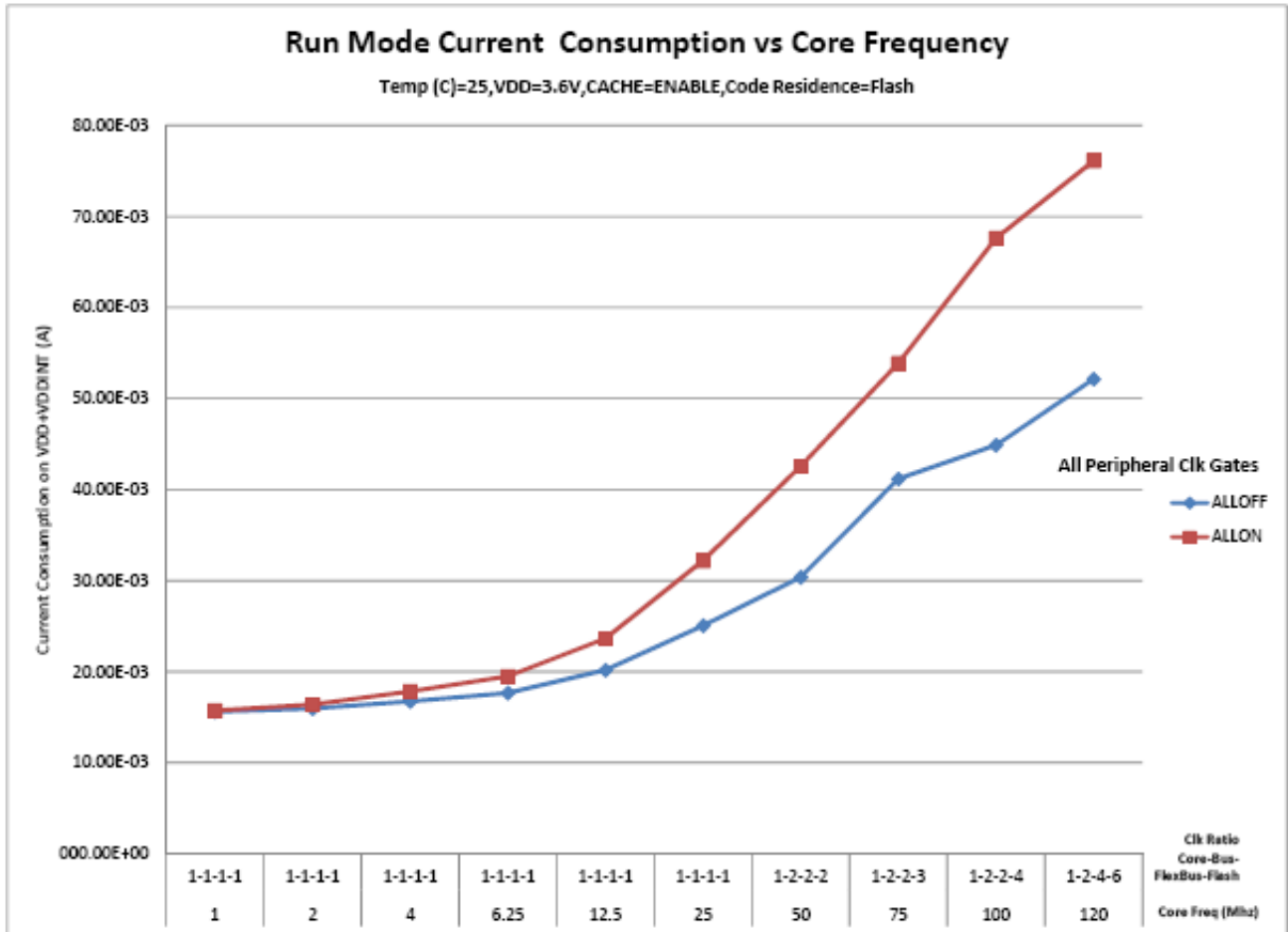


Figure 2. Run mode supply current vs. core frequency

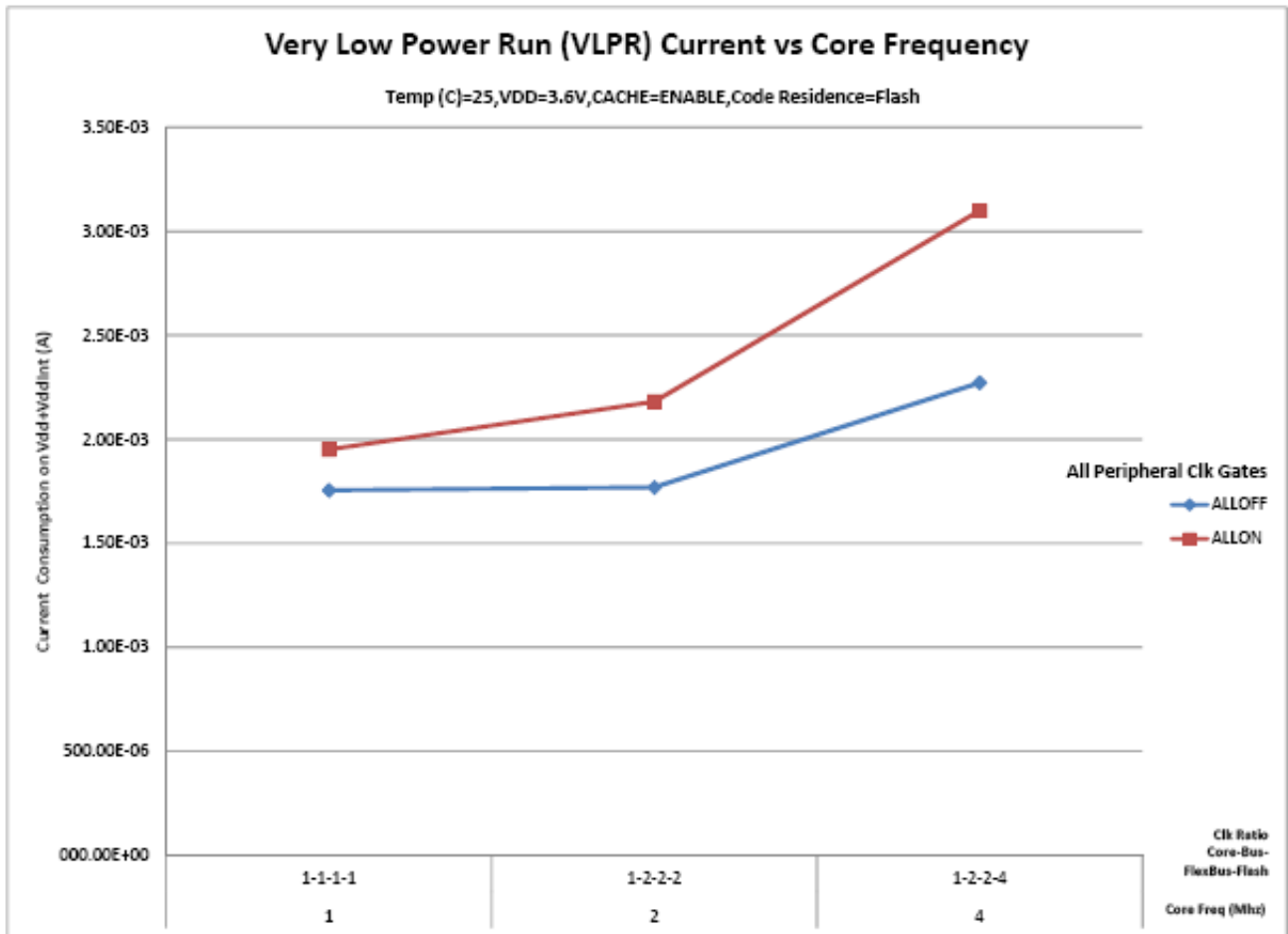


Figure 3. VLPR mode supply current vs. core frequency

5.2.6 EMC radiated emissions operating behaviors

Table 7. EMC radiated emissions operating behaviors for 256MAPBGA

Symbol	Description	Frequency band (MHz)	Typ.	Unit	Notes
V _{RE1}	Radiated emissions voltage, band 1	0.15–50	TBD	dBμV	1, 2
V _{RE2}	Radiated emissions voltage, band 2	50–150	TBD	dBμV	
V _{RE3}	Radiated emissions voltage, band 3	150–500	TBD	dBμV	
V _{RE4}	Radiated emissions voltage, band 4	500–1000	TBD	dBμV	
V _{RE_IEC}	IEC level	0.15–1000	K	—	2, 3

1. Determined according to IEC Standard 61967-1, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 1: General Conditions and Definitions* and IEC Standard 61967-2, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 2: Measurement of Radiated Emissions – TEM Cell and Wideband TEM Cell Method*. Measurements were made while the microcontroller was running basic application code. The reported emission level is the value of the maximum measured emission, rounded up to the next whole number, from among the measured orientations in each frequency range.
2. V_{DD} = 3.3 V, T_A = 25 °C, f_{OSC} = 12 MHz (crystal), f_{SYS} = 96 MHz, f_{BUS} = 48 MHz

3. Specified according to Annex D of IEC Standard 61967-2, *Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*

5.2.7 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to <http://www.freescale.com>.
2. Perform a keyword search for “EMC design.”

5.2.8 Capacitance attributes

Table 8. Capacitance attributes

Symbol	Description	Min.	Max.	Unit
C_{IN_A}	Input capacitance: analog pins	—	7	pF
C_{IN_D}	Input capacitance: digital pins	—	7	pF
$C_{IN_D_io60}$	Input capacitance: fast digital pins	—	9	pF

5.3 Switching specifications

5.3.1 Device clock specifications

Table 9. Device clock specifications

Symbol	Description	Min.	Max.	Unit	Notes
Normal run mode					
f_{SYS}	System and core clock	—	120	MHz	
f_{SYS_USBFS}	System and core clock when Full Speed USB in operation	20	—	MHz	
f_{SYS_USBHS}	System and core clock when High Speed USB in operation	60	—	MHz	
f_{ENET}	System and core clock when ethernet in operation <ul style="list-style-type: none"> • 10 Mbps • 100 Mbps 	5 50	— —	MHz	
f_{BUS}	Bus clock	—	60	MHz	
FB_CLK	FlexBus clock	—	50	MHz	
f_{FLASH}	Flash clock	—	25	MHz	

Table continues on the next page...

Table 9. Device clock specifications (continued)

Symbol	Description	Min.	Max.	Unit	Notes
f_{DDR}	DDR clock	—	150	MHz	
f_{LPTMR}	LPTMR clock	—	25	MHz	
VLPR mode ¹					
f_{SYS}	System and core clock	—	4	MHz	
f_{BUS}	Bus clock	—	4	MHz	
FB_CLK	FlexBus clock	—	4	MHz	
f_{FLASH}	Flash clock	—	1	MHz	
f_{LPTMR}	LPTMR clock	—	4	MHz	

1. The frequency limitations in VLPR mode here override any frequency specification listed in the timing specification for any other module.

5.3.2 General switching specifications

These general purpose specifications apply to all signals configured for GPIO, UART, CAN, CMT, IEEE 1588 timer, and I²C signals.

Table 10. General switching specifications

Symbol	Description	Min.	Max.	Unit	Notes
	GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path	1.5	—	Bus clock cycles	1
	GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter enabled) — Asynchronous path	100	—	ns	2
	GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter disabled) — Asynchronous path	16	—	ns	2
	External reset pulse width (digital glitch filter disabled)	100	—	ns	2
	Mode select (EZP_CS) hold time after reset deassertion	2	—	Bus clock cycles	
$t_{\text{i}050}$	Port rise and fall time (high drive strength) <ul style="list-style-type: none"> Slew disabled Slew enabled 	—	TBD	ns	3
		—	TBD	ns	4
$t_{\text{i}050}$	Port rise and fall time (low drive strength) <ul style="list-style-type: none"> Slew disabled Slew enabled 	—	TBD	ns	3
		—	TBD	ns	4
$t_{\text{i}060}$	Port rise and fall time (high drive strength) <ul style="list-style-type: none"> Slew disabled Slew enabled 	—	TBD	ns	3
		—	TBD	ns	4

Table continues on the next page...

Table 10. General switching specifications (continued)

Symbol	Description	Min.	Max.	Unit	Notes
t_{io60}	Port rise and fall time (low drive strength)	—	TBD	ns	3
	• Slew disabled	—	TBD	ns	4
	• Slew enabled				
t_{tamper}	Port rise and fall time (high drive strength)	—	TBD	ns	5
	• Slew disabled	—	TBD	ns	6
	• Slew enabled				
t_{tamper}	Port rise and fall time (low drive strength)	—	TBD	ns	7
	• Slew disabled	—	TBD	ns	8
	• Slew enabled				
t_{ddr}	Port rise time	—	TBD	ns	9
	• DDR1	—	TBD	ns	10
	• DDR2	—	TBD	ns	11
	• LPDDR				
t_{ddr}	Port fall time	—	TBD	ns	9
	• DDR1	—	TBD	ns	10
	• DDR2	—	TBD	ns	11
	• LPDDR				

1. The greater synchronous and asynchronous timing must be met.
2. This is the shortest pulse that is guaranteed to be recognized.
3. 25pF load
4. 15pF load
5. 75pF load
6. 15pF load
7. 75pF load
8. 15pF load
9. DDR —rise and fall times at 50 Ω transmission line impedance terminated to $0.5 \times V_{DD_DDR} + 5$ pF load.
10. Rising slew rate measured between $0.5 \times V_{DD_DDR}$ and $0.5 \times V_{DD_DDR} + 250$ mV for all modes.
11. Falling slew rate measured between $0.5 \times V_{DD_DDR}$ and $0.5 \times V_{DD_DDR} - 250$ mV for all modes.

5.4 Thermal specifications

5.4.1 Thermal operating requirements

Table 11. Thermal operating requirements

Symbol	Description	Min.	Max.	Unit
T_J	Die junction temperature	–40	125	$^{\circ}\text{C}$
T_A	Ambient temperature	–40	105	$^{\circ}\text{C}$

5.4.2 Thermal attributes

Board type	Symbol	Description	256 MAPBGA	Unit	Notes
Single-layer (1s)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	43	°C/W	1, 2
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	28	°C/W	1,2, 3
Single-layer (1s)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	36	°C/W	1,3
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	25	°C/W	1,3
—	$R_{\theta JB}$	Thermal resistance, junction to board	17	°C/W	4
—	$R_{\theta JC}$	Thermal resistance, junction to case	8	°C/W	5
—	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	2	°C/W	6

- Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
- Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)* with the single layer board horizontal. Board meets JESD51-9 specification.
- Determined according to JEDEC Standard JESD51-6, *Integrated Circuits Thermal Test Method Environmental Conditions—Forced Convection (Moving Air)* with the board horizontal.
- Determined according to JEDEC Standard JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions—Junction-to-Board*. Board temperature is measured on the top surface of the board near the package.
- Determined according to Method 1012.1 of MIL-STD 883, *Test Method Standard, Microcircuits*, with the cold plate temperature used for the case temperature. The value includes the thermal resistance of the interface material between the top of the package and the cold plate.
- Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*.

6 Peripheral operating requirements and behaviors

6.1 Core modules

6.1.1 Debug trace timing specifications

Table 12. Debug trace operating behaviors

Symbol	Description	Min.	Max.	Unit
T_{cyc}	Clock period	Frequency dependent		MHz
T_{wl}	Low pulse width	2	—	ns
T_{wh}	High pulse width	2	—	ns
T_r	Clock and data rise time	—	3	ns
T_f	Clock and data fall time	—	3	ns
T_s	Data setup	3	—	ns
T_h	Data hold	2	—	ns

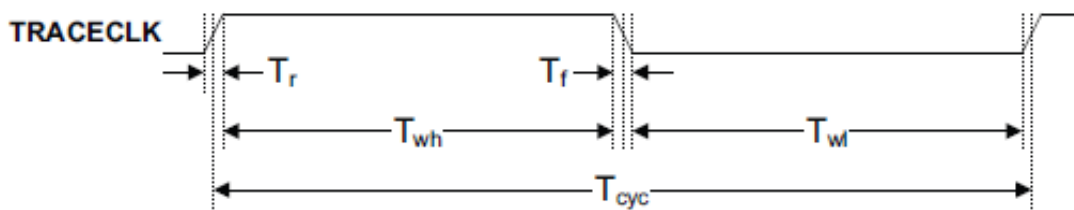


Figure 4. TRACE_CLKOUT specifications

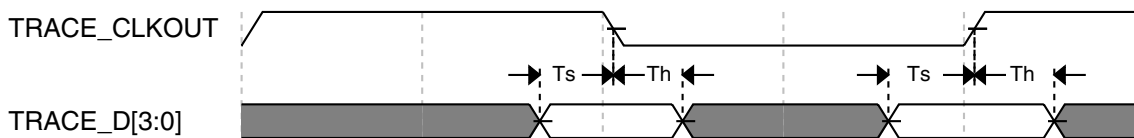


Figure 5. Trace data specifications

6.1.2 JTAG electricals

Table 13. JTAG voltage range electricals

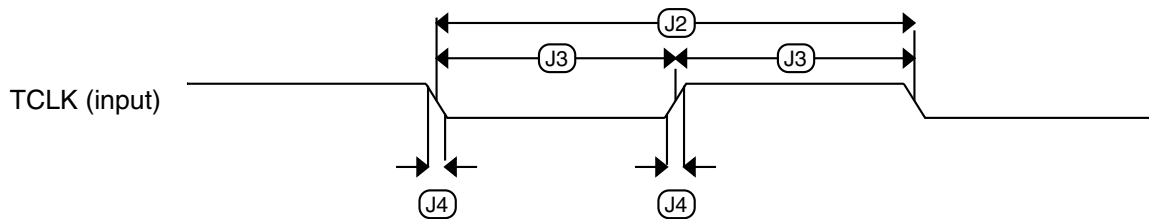
Symbol	Description	Min.	Max.	Unit
	Operating voltage	2.7	5.5	V
J1	TCLK frequency of operation			MHz
	• JTAG	—	10	
	• CJTAG	—	5	

Table continues on the next page...

Table 13. JTAG voltage range electricals (continued)

Symbol	Description	Min.	Max.	Unit
J2	TCLK cycle period	1/J1	—	ns
J3	TCLK clock pulse width <ul style="list-style-type: none"> • JTAG • CJTAG 	100	—	ns
		200	—	ns
		—	—	ns
J4	TCLK rise and fall times	—	1	ns
J5	TMS input data setup time to TCLK rise <ul style="list-style-type: none"> • JTAG • CJTAG 	53	—	ns
		112	—	ns
J6	TDI input data setup time to TCLK rise	8	—	ns
J7	TMS input data hold time after TCLK rise <ul style="list-style-type: none"> • JTAG • CJTAG 	3.4	—	ns
		3.4	—	ns
J8	TDI input data hold time after TCLK rise	3.4	—	ns
J9	TCLK low to TMS data valid <ul style="list-style-type: none"> • JTAG • CJTAG 	—	48	ns
		—	85	ns
J10	TCLK low to TDO data valid	—	48	ns
J11	Output data hold/invalid time after clock edge ¹	—	3	ns

1. They are common for JTAG and CJTAG.

**Figure 6. Test clock input timing**

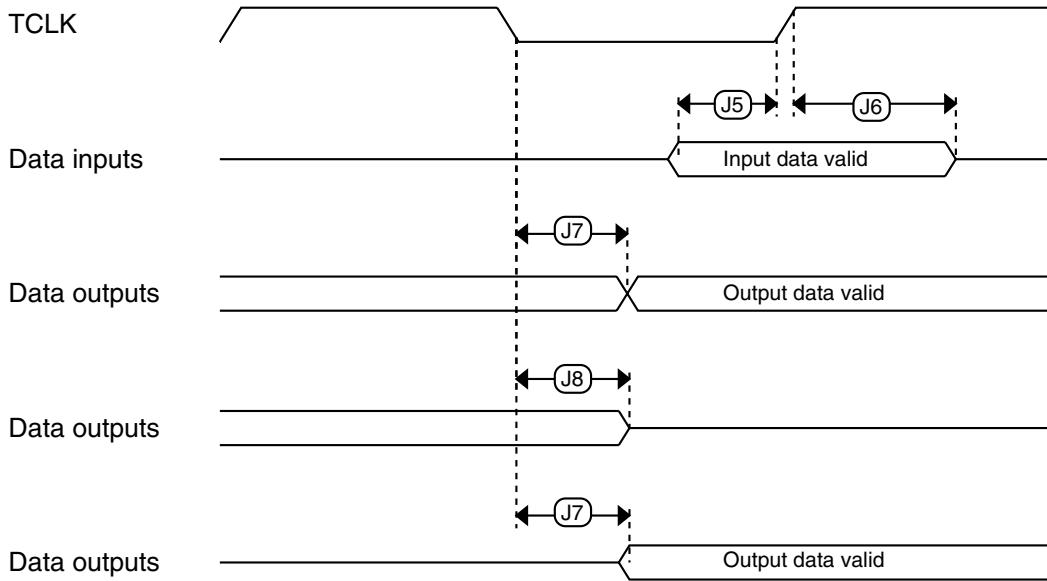


Figure 7. Boundary scan (JTAG) timing

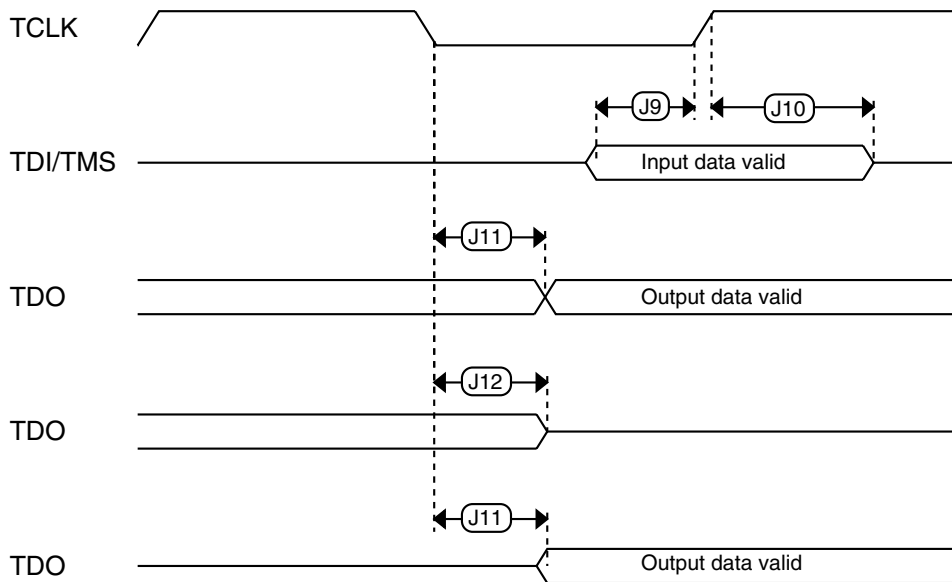


Figure 8. Test Access Port timing

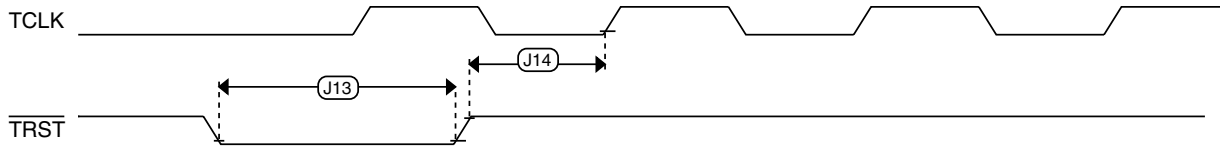


Figure 9. TRST timing

6.2 System modules

There are no specifications necessary for the device's system modules.

6.3 Clock modules

6.3.1 MCG specifications

Table 14. MCG specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$f_{\text{ints_ft}}$	Internal reference frequency (slow clock) — factory trimmed at nominal VDD and 25 °C	—	32.768	—	kHz	
$f_{\text{ints_t}}$	Internal reference frequency (slow clock) — user trimmed	31.25	—	39.0625	kHz	
I_{ints}	Internal reference (slow clock) current	—	TBD	—	μA	
$\Delta f_{\text{dco_res_t}}$	Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM and SCFTRIM	—	± 0.3	± 0.6	% f_{dco}	1
$\Delta f_{\text{dco_res_t}}$	Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM only	—	± 0.2	± 0.5	% f_{dco}	1
$\Delta f_{\text{dco_t}}$	Total deviation of trimmed average DCO output frequency over voltage and temperature	—	± 10	—	% f_{dco}	1
$\Delta f_{\text{dco_t}}$	Total deviation of trimmed average DCO output frequency over fixed voltage and temperature range of 0–70°C	—	± 4.5	—	% f_{dco}	1
$f_{\text{intf_ft}}$	Internal reference frequency (fast clock) — factory trimmed at nominal VDD and 25°C	—	—	4	MHz	
$f_{\text{intf_t}}$	Internal reference frequency (fast clock) — user trimmed at nominal VDD and 25 °C	3	—	5	MHz	
I_{intf}	Internal reference (fast clock) current	—	TBD	—	μA	

Table continues on the next page...

Table 14. MCG specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes	
f_{loc_low}	Loss of external clock minimum frequency — RANGE = 00	$(3/5) \times f_{ints_t}$	—	—	kHz		
f_{loc_high}	Loss of external clock minimum frequency — RANGE = 01, 10, or 11	$(16/5) \times f_{ints_t}$	—	—	kHz		
FLL							
f_{fll_ref}	FLL reference frequency range	31.25	—	39.0625	kHz		
f_{dco}	DCO output frequency range	Low range (DRS=00) $640 \times f_{fll_ref}$	20	20.97	25	MHz	2, 3
		Mid range (DRS=01) $1280 \times f_{fll_ref}$	40	41.94	50	MHz	
		Mid-high range (DRS=10) $1920 \times f_{fll_ref}$	60	62.91	75	MHz	
		High range (DRS=11) $2560 \times f_{fll_ref}$	80	83.89	100	MHz	
$f_{dco_t_DMX3_2}$	DCO output frequency	Low range (DRS=00) $732 \times f_{fll_ref}$	—	23.99	—	MHz	4, 5
		Mid range (DRS=01) $1464 \times f_{fll_ref}$	—	47.97	—	MHz	
		Mid-high range (DRS=10) $2197 \times f_{fll_ref}$	—	71.99	—	MHz	
		High range (DRS=11) $2929 \times f_{fll_ref}$	—	95.98	—	MHz	
J_{cyc_fll}	FLL period jitter <ul style="list-style-type: none"> $f_{VCO} = 48$ MHz $f_{VCO} = 98$ MHz 	—	180	—	ps		
J_{acc_fll}	FLL accumulated jitter of DCO output over a 1 μ s time window	—	TBD	—	ps		
$t_{fll_acquire}$	FLL target frequency acquisition time	—	—	1	ms	6	
PLL0,1							
f_{pll_ref}	PLL reference frequency range	8	—	16	MHz		
f_{vcoclk_2x}	VCO output frequency	180	—	360	MHz		
f_{vcoclk}	PLL output frequency	90	—	180	MHz		
f_{vcoclk_90}	PLL quadrature output frequency	90	—	180	MHz		
I_{pll}	PLL operating current (fast)	—	TBD	—	μ A	7	

Table continues on the next page...

Table 14. MCG specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{pll}	PLL operating current (fast)	—	TBD	—	μA	7
t_{pll_lock}	Lock detector detection time	—	—	$100 \times 10^{-6} + 1075(1/f_{pll_ref})$	s	8
J_{cyc_pll}	Jitter (cycle to cycle)	—	50	TBD	ps	
J_{acc_pll}	Jitter (accumulated)	—	500	TBD	ps	9

1. This parameter is measured with the internal reference (slow clock) being used as a reference to the FLL (FEI clock mode).
2. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=0.
3. The resulting system clock frequencies should not exceed their maximum specified values. The DCO frequency deviation (Δf_{dco_t}) over voltage and temperature should be considered.
4. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=1.
5. The resulting clock frequency must not exceed the maximum specified clock frequency of the device.
6. This specification applies to any time the FLL reference source or reference divider is changed, trim value is changed, DMX32 bit is changed, DRS bits are changed, or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.
7. Excludes any oscillator currents that are also consuming power while PLL is in operation.
8. This specification applies to any time the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, this specification assumes it is already running.
9. Accumulated jitter will depend on VCO frequency and VDIV.

6.3.2 Oscillator electrical specifications

This section provides the electrical characteristics of the module.

6.3.2.1 Oscillator DC electrical specifications

Table 15. Oscillator DC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	—	3.6	V	
I_{DDOSC}	Supply current — low-power mode (HGO=0) <ul style="list-style-type: none"> • 32 kHz • 4 MHz • 8 MHz (RANGE=01) • 16 MHz • 24 MHz • 32 MHz 	—	500	—	nA	1
		—	200	—	μA	
		—	300	—	μA	
		—	950	—	μA	
		—	1.2	—	mA	
		—	1.5	—	mA	

Table continues on the next page...

Table 15. Oscillator DC electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I _{DDOSC}	Supply current — high gain mode (HGO=1)					1
	• 32 kHz	—	25	—	μA	
	• 4 MHz	—	400	—	μA	
	• 8 MHz (RANGE=01)	—	500	—	μA	
	• 16 MHz	—	2.5	—	mA	
	• 24 MHz	—	3	—	mA	
• 32 MHz	—	4	—	mA		
C _x	EXTAL load capacitance	—	—	—		2, 3
C _y	XTAL load capacitance	—	—	—		2, 3
R _F	Feedback resistor — low-frequency, low-power mode (HGO=0)	—	—	—	MΩ	2, 4
	Feedback resistor — low-frequency, high-gain mode (HGO=1)	—	10	—	MΩ	
	Feedback resistor — high-frequency, low-power mode (HGO=0)	—	—	—	MΩ	
	Feedback resistor — high-frequency, high-gain mode (HGO=1)	—	1	—	MΩ	
R _S	Series resistor — low-frequency, low-power mode (HGO=0)	—	—	—	kΩ	
	Series resistor — low-frequency, high-gain mode (HGO=1)	—	200	—	kΩ	
	Series resistor — high-frequency, low-power mode (HGO=0)	—	—	—	kΩ	
	Series resistor — high-frequency, high-gain mode (HGO=1)	—	0	—	kΩ	
V _{pp} ⁵	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, high-gain mode (HGO=1)	—	V _{DD}	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, high-gain mode (HGO=1)	—	V _{DD}	—	V	

1. V_{DD}=3.3 V, Temperature =25 °C
2. See crystal or resonator manufacturer's recommendation
3. C_x,C_y can be provided by using either the integrated capacitors or by using external components.
4. When low power mode is selected, R_F is integrated and must not be attached externally.

Peripheral operating requirements and behaviors

- The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other devices.

6.3.2.2 Oscillator frequency specifications

Table 16. Oscillator frequency specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{osc_lo}	Oscillator crystal or resonator frequency — low frequency mode (MCG_C2[RANGE]=00)	32	—	40	kHz	
$f_{osc_hi_1}$	Oscillator crystal or resonator frequency — high frequency mode (low range) (MCG_C2[RANGE]=01)	3	—	8	MHz	1
$f_{osc_hi_2}$	Oscillator crystal or resonator frequency — high frequency mode (high range) (MCG_C2[RANGE]=1x)	8	—	32	MHz	
f_{ec_extal}	Input clock frequency (external clock mode)	—	—	60	MHz	2, 3
t_{dc_extal}	Input clock duty cycle (external clock mode)	40	50	60	%	
t_{cst}	Crystal startup time — 32 kHz low-frequency, low-power mode (HGO=0)	—	1000	—	ms	4, 5
	Crystal startup time — 32 kHz low-frequency, high-gain mode (HGO=1)	—	500	—	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), low-power mode (HGO=0)	—	0.6	—	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), high-gain mode (HGO=1)	—	1	—	ms	

- Frequencies less than 8 MHz are not in the PLL range.
- Other frequency limits may apply when external clock is being used as a reference for the FLL or PLL.
- When transitioning from FBE to FEI mode, restrict the frequency of the input clock so that, when it is divided by FRDIV, it remains within the limits of the DCO input clock frequency.
- Proper PC board layout procedures must be followed to achieve specifications.
- Crystal startup time is defined as the time between the oscillator being enabled and the OSCINIT bit in the MCG_S register being set.

6.3.3 32kHz Oscillator Electrical Characteristics

This section describes the module electrical characteristics.

6.3.3.1 32kHz oscillator DC electrical specifications

Table 17. 32kHz oscillator DC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{BAT}	Supply voltage	1.71	—	3.6	V
R_F	Internal feedback resistor	—	100	—	M Ω

Table continues on the next page...

Table 17. 32kHz oscillator DC electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit
C_{para}	Parasitical capacitance of EXTAL32 and XTAL32	—	5	7	pF
V_{pp} ¹	Peak-to-peak amplitude of oscillation	—	0.6	—	V

1. The EXTAL32 and XTAL32 pins should only be connected to required oscillator components and must not be connected to any other devices.

6.3.3.2 32kHz oscillator frequency specifications

Table 18. 32kHz oscillator frequency specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{osc_lo}	Oscillator crystal	—	32.768	—	kHz	
t_{start}	Crystal start-up time	—	1000	—	ms	1

1. Proper PC board layout procedures must be followed to achieve specifications.

6.4 Memories and memory interfaces

6.4.1 Flash (FTFE) electrical specifications

This section describes the electrical characteristics of the FTFE module.

6.4.1.1 Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

Table 19. NVM program/erase timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{hvp4}	Program Phrase high-voltage time	—	7.5	TBD	μ s	
$t_{hversscr}$	Erase Flash Sector high-voltage time	—	13	TBD	ms	1
$t_{hversblk}$	Erase Flash Block high-voltage time	—	425	TBD	ms	1

1. Maximum time based on expectations at cycling end-of-life.

6.4.1.2 Flash timing specifications — commands**Table 20. Flash command timing specifications**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{rd1blk}	Read 1s Block execution time	—	1.5	TBD	ms	
$t_{rd1sec4k}$	Read 1s Section execution time (4KB flash)	—	50	TBD	μ s	1
t_{pgmchk}	Program Check execution time	—	35	TBD	μ s	1
t_{rdsrc}	Read Resource execution time	—	35	TBD	μ s	1
t_{pgm8}	Program Phrase execution time	—	65	TBD	μ s	
t_{ersblk}	Erase Flash Block execution time	—	450	TBD	ms	2
t_{ersscr}	Erase Flash Sector execution time	—	15	TBD	ms	2
$t_{pgmsec4k}$	Program Section execution time (4KB flash)	—	20	TBD	ms	
t_{rd1all}	Read 1s All Blocks execution time	—	1.5	TBD	ms	
t_{rdonce}	Read Once execution time	—	17	TBD	μ s	1
$t_{pgmonce}$	Program Once execution time	—	65	TBD	μ s	
t_{ersall}	Erase All Blocks execution time	—	900	TBD	ms	2
t_{vfykey}	Verify Backdoor Access Key execution time	—	25	TBD	μ s	1
$t_{swapx01}$	Swap Control execution time • control code 0x01	—	185	TBD	μ s	
$t_{swapx02}$	• control code 0x02	—	65	TBD	μ s	
$t_{swapx04}$	• control code 0x04	—	65	TBD	μ s	
$t_{swapx08}$	• control code 0x08	—	25	TBD	μ s	
$t_{pgmpart}$	Program Partition for EEPROM execution time	—	TBD	TBD	ms	
$t_{setram64k}$	Set FlexRAM Function execution time: • 64 KB EEPROM backup	—	TBD	TBD	ms	
$t_{setram128k}$	• 128 KB EEPROM backup	—	TBD	TBD	ms	
$t_{setram256k}$	• 256 KB EEPROM backup	—	TBD	TBD	ms	
$t_{setram512k}$	• 512 KB EEPROM backup	—	TBD	TBD	ms	
$t_{eewr8bers}$	Byte-write to erased FlexRAM location execution time	—	100	TBD	μ s	3
$t_{eewr8b64k}$	Byte-write to FlexRAM execution time: • 64 KB EEPROM backup	—	TBD	TBD	ms	
$t_{eewr8b128k}$	• 128 KB EEPROM backup	—	TBD	TBD	ms	
$t_{eewr8b256k}$	• 256 KB EEPROM backup	—	TBD	TBD	ms	
$t_{eewr8b512k}$	• 512 KB EEPROM backup	—	TBD	TBD	ms	
$t_{eewr16bers}$	16-bit write to erased FlexRAM location execution time	—	100	TBD	μ s	

Table continues on the next page...

Table 20. Flash command timing specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{\text{eewr16b64k}}$	16-bit write to FlexRAM execution time: <ul style="list-style-type: none"> • 64 KB EEPROM backup • 128 KB EEPROM backup • 256 KB EEPROM backup • 512 KB EEPROM backup 	—	TBD	TBD	ms	
$t_{\text{eewr16b128k}}$		—	TBD	TBD	ms	
$t_{\text{eewr16b256k}}$		—	TBD	TBD	ms	
$t_{\text{eewr16b512k}}$		—	TBD	TBD	ms	
$t_{\text{eewr32bers}}$	32-bit write to erased FlexRAM location execution time	—	200	TBD	μs	
$t_{\text{eewr32b64k}}$	32-bit-write to FlexRAM execution time: <ul style="list-style-type: none"> • 64 KB EEPROM backup • 128 KB EEPROM backup • 256 KB EEPROM backup • 512 KB EEPROM backup 	—	TBD	TBD	ms	
$t_{\text{eewr32b128k}}$		—	TBD	TBD	ms	
$t_{\text{eewr32b256k}}$		—	TBD	TBD	ms	
$t_{\text{eewr32b512k}}$		—	TBD	TBD	ms	

1. Assumes 25MHz flash clock frequency.
2. Maximum times for erase parameters based on expectations at cycling end-of-life.
3. For byte-writes to an erased FlexRAM location, the aligned word containing the byte must be erased.

6.4.1.3 Flash (FTFE) current and power specifications

Table 21. Flash (FTFE) current and power specifications

Symbol	Description	Typ.	Unit
$I_{\text{DD_PGM}}$	Worst case programming current in program flash	10	mA

6.4.1.4 Reliability specifications

Table 22. NVM reliability specifications

Symbol	Description	Min.	Typ. ¹	Max.	Unit	Notes
Program Flash						
$t_{\text{nv mretp10k}}$	Data retention after up to 10 K cycles	5	50	—	years	2
$t_{\text{nv mretp1k}}$	Data retention after up to 1 K cycles	10	100	—	years	2
$t_{\text{nv mretp100}}$	Data retention after up to 100 cycles	15	100	—	years	2
$\eta_{\text{nv mcycp}}$	Cycling endurance	10 K	35 K	—	cycles	3
Data Flash						
$t_{\text{nv mretd10k}}$	Data retention after up to 10 K cycles	5	50	—	years	2
$t_{\text{nv mretd1k}}$	Data retention after up to 1 K cycles	10	100	—	years	2
$t_{\text{nv mretd100}}$	Data retention after up to 100 cycles	15	100	—	years	2
$\eta_{\text{nv mcycd}}$	Cycling endurance	10 K	35 K	—	cycles	3

Table continues on the next page...

Table 22. NVM reliability specifications (continued)

Symbol	Description	Min.	Typ. ¹	Max.	Unit	Notes
FlexRAM as EEPROM						
$t_{nmwreee100}$	Data retention up to 100% of write endurance	5	50	—	years	2
$t_{nmwreee10}$	Data retention up to 10% of write endurance	10	100	—	years	2
$t_{nmwreee1}$	Data retention up to 1% of write endurance	15	100	—	years	2
	Write endurance					4
$n_{nmwreee16}$	• EEPROM backup to FlexRAM ratio = 16	TBD	TBD	—	writes	
$n_{nmwreee128}$	• EEPROM backup to FlexRAM ratio = 128	TBD	TBD	—	writes	
$n_{nmwreee512}$	• EEPROM backup to FlexRAM ratio = 512	TBD	TBD	—	writes	
$n_{nmwreee4k}$	• EEPROM backup to FlexRAM ratio = 4096	TBD	TBD	—	writes	
$n_{nmwreee32k}$	• EEPROM backup to FlexRAM ratio = 32,768	TBD	TBD	—	writes	

1. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25°C profile. Engineering Bulletin EB618 does not apply to this technology.
2. Data retention is based on $T_{javg} = 55^{\circ}\text{C}$ (temperature profile over the lifetime of the application).
3. Cycling endurance represents number of program/erase cycles at $-40^{\circ}\text{C} \leq T_j \leq 125^{\circ}\text{C}$.
4. Write endurance represents the number of writes to each FlexRAM location at $-40^{\circ}\text{C} \leq T_j \leq 125^{\circ}\text{C}$ influenced by the cycling endurance of the FlexNVM (same value as data flash) and the allocated EEPROM backup per subsystem. Minimum and typical values assume all byte-writes to FlexRAM.

6.4.1.5 Write endurance to FlexRAM for EEPROM

TBD

6.4.2 EzPort Switching Specifications

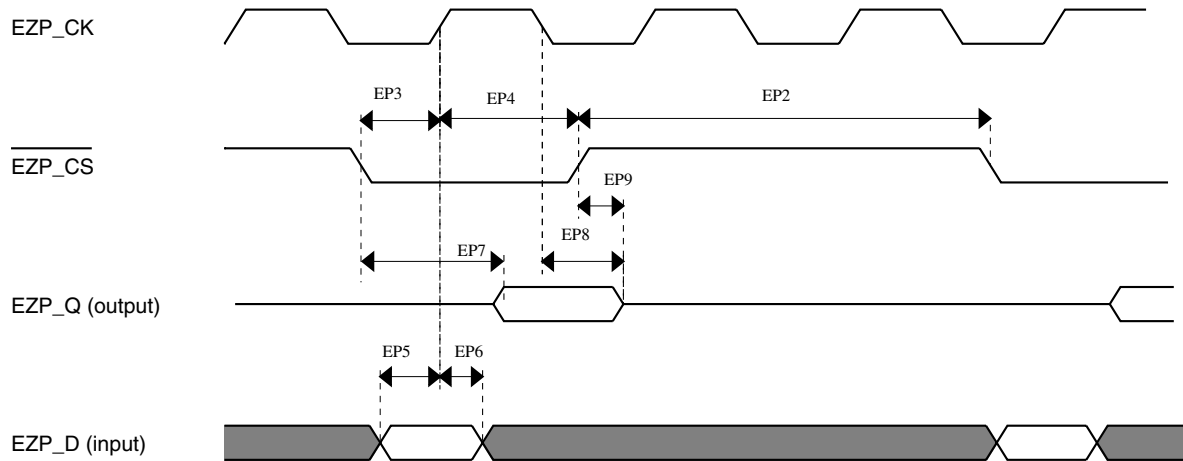
Table 23. EzPort switching specifications

Num	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
EP1	EZP_CK frequency of operation (all commands except READ)	—	$f_{\text{SYS}}/2$	MHz
EP1a	EZP_CK frequency of operation (READ command)	—	$f_{\text{SYS}}/8$	MHz
EP2	$\overline{\text{EZP_CS}}$ negation to next $\overline{\text{EZP_CS}}$ assertion	$2 \times t_{\text{EZP_CK}}$	—	ns
EP3	$\overline{\text{EZP_CS}}$ input valid to EZP_CK high (setup)	5	—	ns
EP4	EZP_CK high to $\overline{\text{EZP_CS}}$ input invalid (hold)	5	—	ns
EP5	EZP_D input valid to EZP_CK high (setup)	2	—	ns
EP6	EZP_CK high to EZP_D input invalid (hold)	5	—	ns
EP7	EZP_CK low to EZP_Q output valid	—	16	ns

Table continues on the next page...

Table 23. EzPort switching specifications (continued)

Num	Description	Min.	Max.	Unit
EP8	EZP_CK low to EZP_Q output invalid (hold)	0	—	ns
EP9	$\overline{\text{EZP_CS}}$ negation to EZP_Q tri-state	—	12	ns

**Figure 10. EzPort Timing Diagram**

6.4.3 NFC specifications

The NAND flash controller (NFC) implements the interface to standard NAND flash memory devices. This section describes the timing parameters of the NFC.

In the following table:

- T_H is the flash clock high time and
- T_L is flash clock low time,

which are defined as:

$$T_{\text{NFC}} = T_L + T_H = \frac{T_{\text{input clock}}}{\text{SCALER}}$$

The SCALER value is derived from the fractional divider specified in the SIM's CLKDIV4 register:

$$\text{SCALER} = \frac{\text{SIM_CLKDIV4}[\text{NFCFRAC}] + 1}{\text{SIM_CLKDIV4}[\text{NFCDIV}] + 1}$$

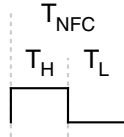
Peripheral operating requirements and behaviors

In case the reciprocal of SCALER is an integer, the duty cycle of NFC clock is 50%, means $T_H = T_L$. In case the reciprocal of SCALER is not an integer:

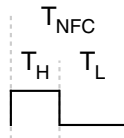
$$T_L = (1 + \text{SCALER} / 2) \times \frac{T_{\text{NFC}}}{2}$$

$$T_H = (1 - \text{SCALER} / 2) \times \frac{T_{\text{NFC}}}{2}$$

For example, if SCALER is 0.2, then $T_H = T_L = T_{\text{NFC}}/2$.



However, if SCALER is 0.667, then $T_L = 2/3 \times T_{\text{NFC}}$ and $T_H = 1/3 \times T_{\text{NFC}}$.



NOTE

The reciprocal of SCALER must be a multiple of 0.5. For example, 1, 1.5, 2, 2.5, etc.

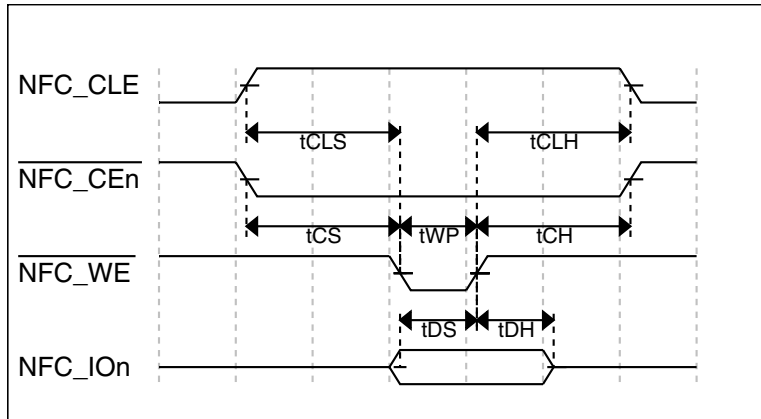
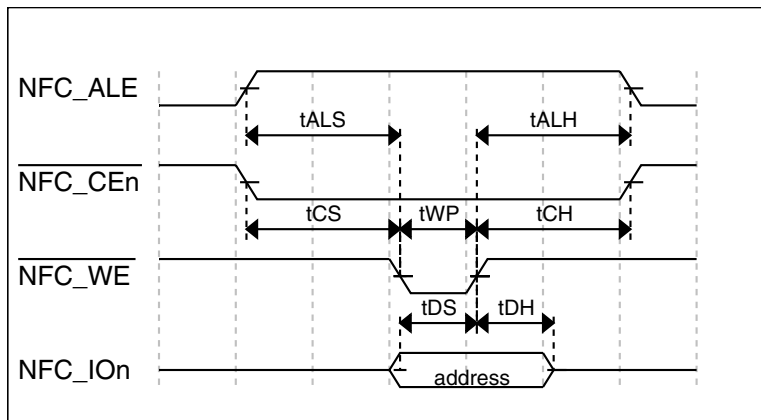
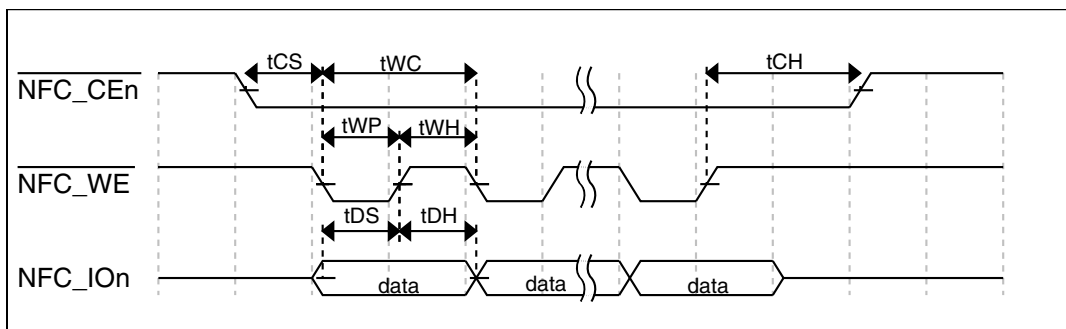
Table 24. NFC specifications

Num	Description	Min.	Max.	Unit
t _{CLS}	NFC_CLE setup time	2T _H + T _L - 1	—	ns
t _{CLH}	NFC_CLE hold time	T _H + T _L - 1	—	ns
t _{CS}	NFC_CEn setup time	2T _H + T _L - 1	—	ns
t _{CH}	NFC_CEn hold time	T _H + T _L	—	ns
t _{WP}	NFC_WP pulse width	T _L - 1	—	ns
t _{ALS}	NFC_ALE setup time	2T _H + T _L	—	ns
t _{ALH}	NFC_ALE hold time	T _H + T _L	—	ns
t _{DS}	Data setup time	T _L - 1	—	ns
t _{DH}	Data hold time	T _H - 1	—	ns
t _{WC}	Write cycle time	T _H + T _L - 1	—	ns
t _{WH}	NFC_WE hold time	T _H - 1	—	ns
t _{RR}	Ready to NFC_RE low	4T _H + 3T _L + 90	—	ns
t _{RP}	NFC_RE pulse width	T _L + 1	—	ns

Table continues on the next page...

Table 24. NFC specifications (continued)

Num	Description	Min.	Max.	Unit
t_{RC}	Read cycle time	$T_L + T_H - 1$	—	ns
t_{REH}	$\overline{\text{NFC_RE}}$ high hold time	$T_H - 1$	—	ns
t_{IS}	Data input setup time	11	—	ns

**Figure 11. Command latch cycle timing****Figure 12. Address latch cycle timing****Figure 13. Write data latch cycle timing**

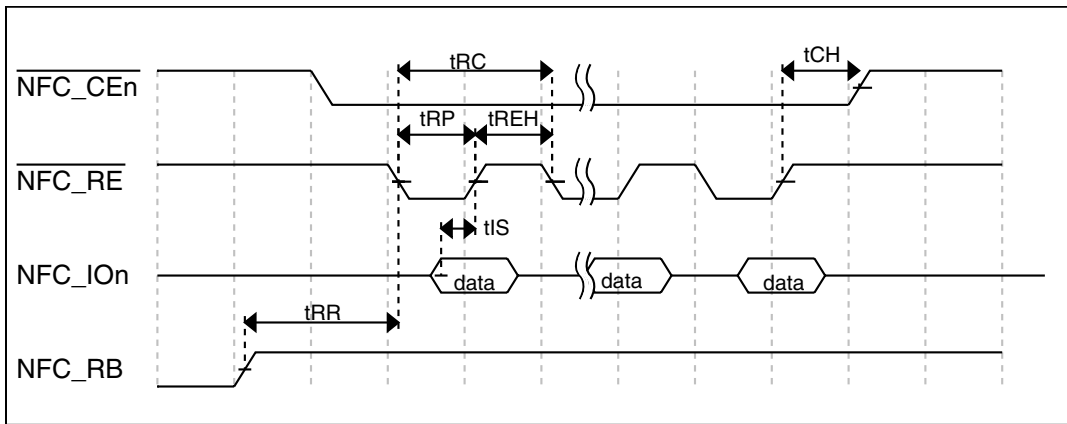


Figure 14. Read data latch cycle timing in non-fast mode

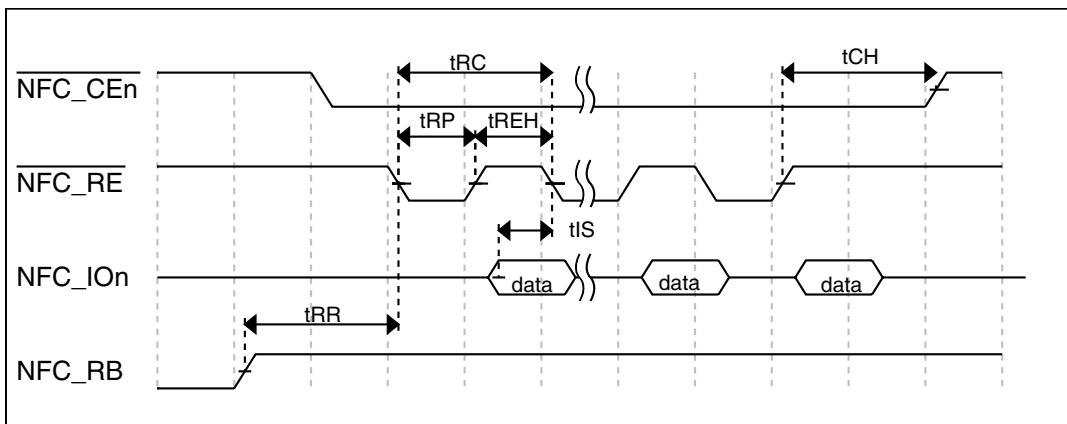


Figure 15. Read data latch cycle timing in fast mode

6.4.4 DDR controller specifications

The following timing numbers must be followed to properly latch or drive data onto the DDR memory bus. All timing numbers are relative to the DQS byte lanes.

Table 25. DDR controller — AC timing specifications

Symbol	Description	Min.	Max.	Unit	Notes
	Frequency of operation				2
	• DDR1	83.3	150	MHz	
	• DDR2	125 ¹	150	MHz	
	• LPDDR	50	150	MHz	

Table continues on the next page...

Table 25. DDR controller — AC timing specifications (continued)

Symbol	Description	Min.	Max.	Unit	Notes
t_{DDRCK}	Clock period				
	• DDR1	6.6	12	ns	
	• DDR2	6.6	8	ns	
	• LPDDR	6.6	20	ns	
V_{OX-AC}	DDRCK AC differential cross point voltage			V	
	• DDR1	$0.5 \times V_{DD_DDR} - 0.2 \text{ V}$	$0.5 \times V_{DD_DDR} + 0.2 \text{ V}$	V	
	• DDR2	$0.5 \times V_{DD_DDR} - 0.125 \text{ V}$	$0.5 \times V_{DD_DDR} + 0.125 \text{ V}$	V	
	• LPDDR	$0.4 \times V_{DD_DDR}$	$0.4 \times V_{DD_DDR}$		
t_{DDRCKH}	Pulse width high	0.45	0.55	t_{DDRCK}	3
t_{DDRCKL}	Pulse width low	0.45	0.55	t_{DDRCK}	3
t_{CMV}	Address, DDR_CKE, DDR_CAS, DDR_RAS, DDR_WE, DDR_CS _n — output valid	$0.5 \times t_{DDRCK} - 1$	—	ns	4
t_{CMH}	Address, DDR_CKE, DDR_CAS, DDR_RAS, DDR_WE, DDR_CS _n — output hold	$0.5 \times t_{DDRCK} - 1$	—	ns	
t_{DQSS}	Write command to first DQS latching transition	$WL - 0.2 \times t_{DDRCK}$	$WL + 0.2 \times t_{DDRCK}$	ns	
t_{QS}	Data and data mask output setup (DQ→DQS) relative to DQS (DDR write mode)	$0.25 \times t_{DDRCK} - 1$	—	ns	5, 6
t_{QH}	Data and data mask output hold (DQS→DQ) relative to DQS (DDR write mode)	$0.25 \times t_{DDRCK} - 1$	—	ns	7
t_{DQSQ}	DQS-DQ skew for DQS and associated DQ signals	$-(0.25 \times t_{DDRCK} - 1)$	$0.25 \times t_{DDRCK} - 1$	ns	8

1. This is minimum frequency of operation according to JEDEC DDR2 specification.
2. DDR data rate = 2 x DDR clock frequency
3. Pulse width high plus pulse width low cannot exceed min and max clock period.
4. Command output valid should be 1/2 the memory bus clock (t_{DDRCK}) plus some minor adjustments for process, temperature, and voltage variations.
5. This specification relates to the required input setup time of DDR memories. The microprocessor's output setup should be larger than the input setup of the DDR memories. If it is not larger, then the input setup on the memory is in violation. DDR_DQ[15:8] is relative to DDR_DQS[1]; DDR_DQ[7:0] is relative to DDR_DQS[0].
6. The first data beat is valid before the first rising edge of DQS and after the DQS write preamble. The remaining data beats are valid for each subsequent DQS edge.
7. This specification relates to the required hold time of DDR memories. DDR_DQ[15:8] is relative to DDR_DQS[1]; DDR_DQ[7:0] is relative to DDR_DQS[0].
8. Data input skew is derived from each DQS clock edge. It begins with a DQS transition and ends when the last data line becomes valid. This input skew must include DDR memory output skew and system level board skew (due to routing or other factors).

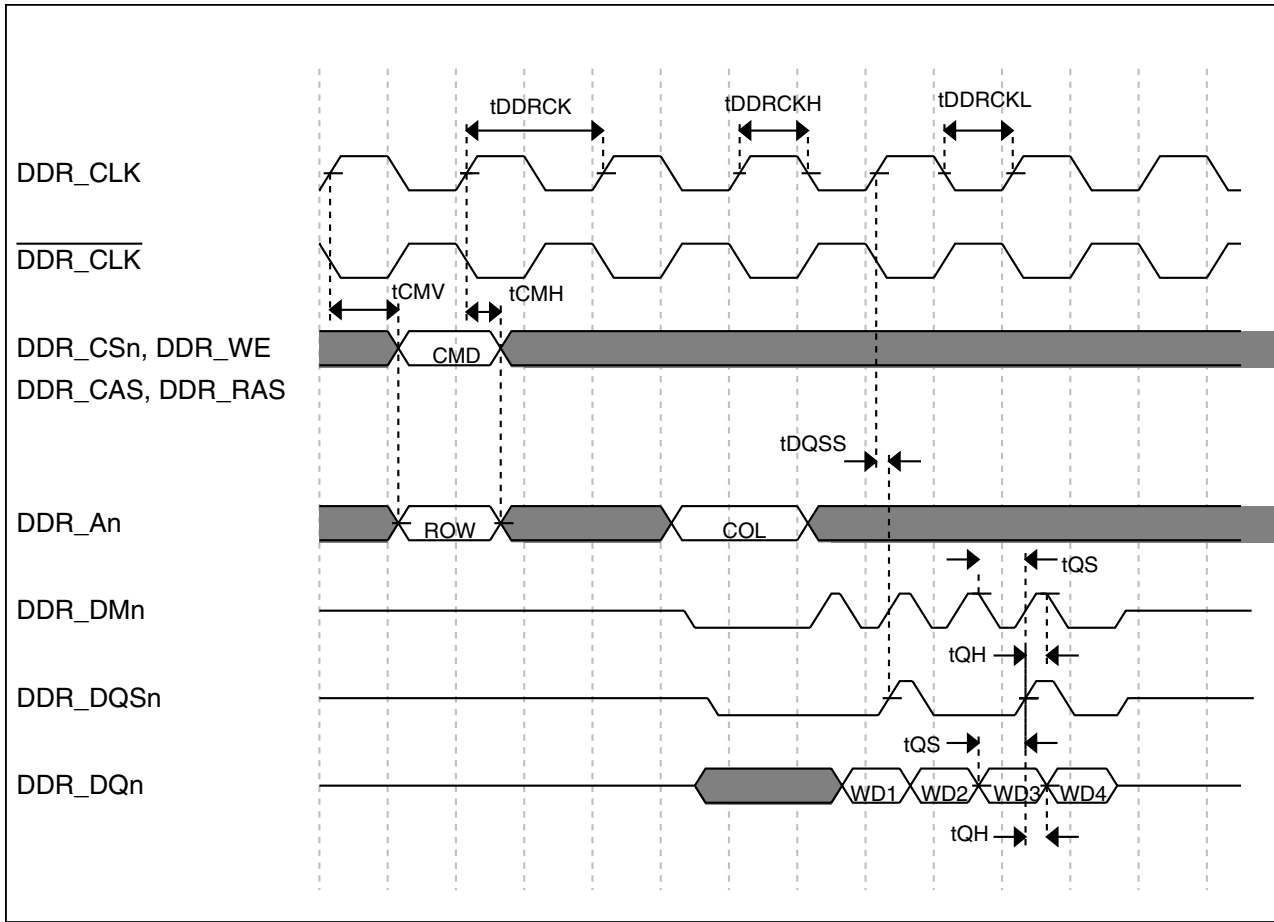


Figure 16. DDR write timing

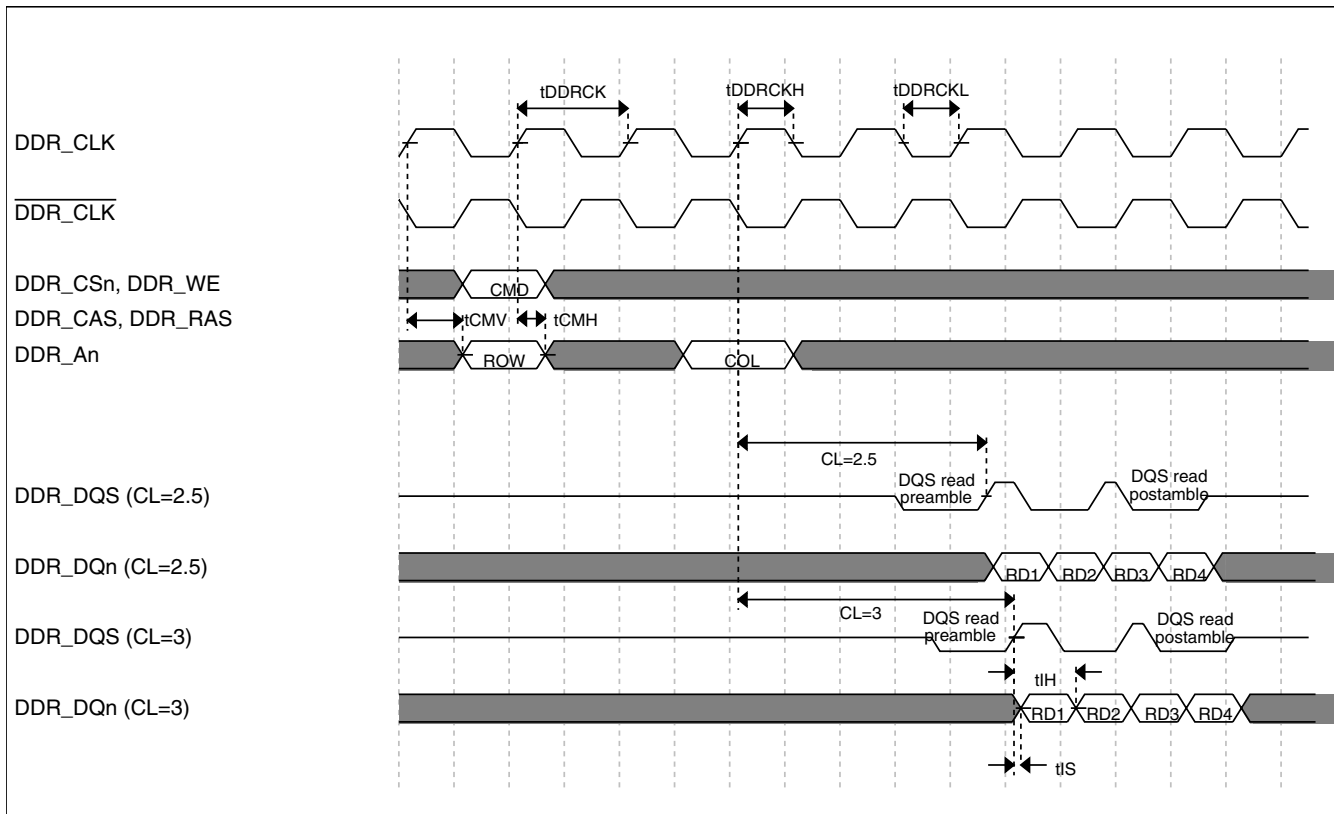


Figure 17. DDR read timing

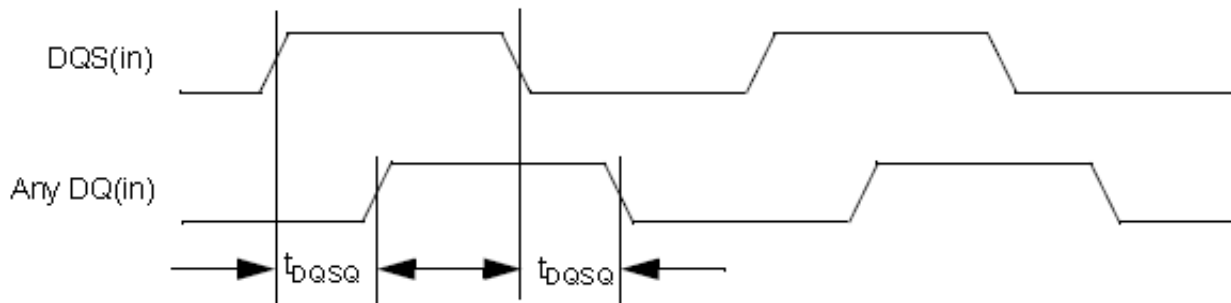


Figure 18. DDR read timing, DQ vs. DQS

6.4.5 Flexbus Switching Specifications

All processor bus timings are synchronous; input setup/hold and output delay are given in respect to the rising edge of a reference clock, FB_CLK. The FB_CLK frequency may be the same as the internal system bus frequency or an integer divider of that frequency.

The following timing numbers indicate when data is latched or driven onto the external bus, relative to the Flexbus output clock (FB_CLK). All other timing relationships can be derived from these values.

Table 26. Flexbus limited voltage range switching specifications

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	2.7	3.6	V	
	Frequency of operation	—	FB_CLK	MHz	
FB1	Clock period	20	—	ns	
FB2	Address, data, and control output valid	—	11.5	ns	1
FB3	Address, data, and control output hold	0.5	—	ns	1
FB4	Data and $\overline{\text{FB_TA}}$ input setup	8.5	—	ns	2
FB5	Data and $\overline{\text{FB_TA}}$ input hold	0.5	—	ns	2

1. Specification is valid for all FB_AD[31:0], $\overline{\text{FB_BE/BWE}n}$, $\overline{\text{FB_CS}n}$, $\overline{\text{FB_OE}}$, FB_R/W, $\overline{\text{FB_TBST}}$, FB_TSIZE[1:0], FB_ALE, and $\overline{\text{FB_TS}}$.
2. Specification is valid for all FB_AD[31:0] and $\overline{\text{FB_TA}}$.

Table 27. Flexbus full voltage range switching specifications

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	1.71	3.6	V	
	Frequency of operation	—	FB_CLK	MHz	
FB1	Clock period	1/FB_CLK	—	ns	
FB2	Address, data, and control output valid	—	13.5	ns	1
FB3	Address, data, and control output hold	0	—	ns	1
FB4	Data and $\overline{\text{FB_TA}}$ input setup	13.7	—	ns	2
FB5	Data and $\overline{\text{FB_TA}}$ input hold	0.5	—	ns	2

1. Specification is valid for all FB_AD[31:0], $\overline{\text{FB_BE/BWE}n}$, $\overline{\text{FB_CS}n}$, $\overline{\text{FB_OE}}$, FB_R/W, $\overline{\text{FB_TBST}}$, FB_TSIZE[1:0], FB_ALE, and $\overline{\text{FB_TS}}$.
2. Specification is valid for all FB_AD[31:0] and $\overline{\text{FB_TA}}$.

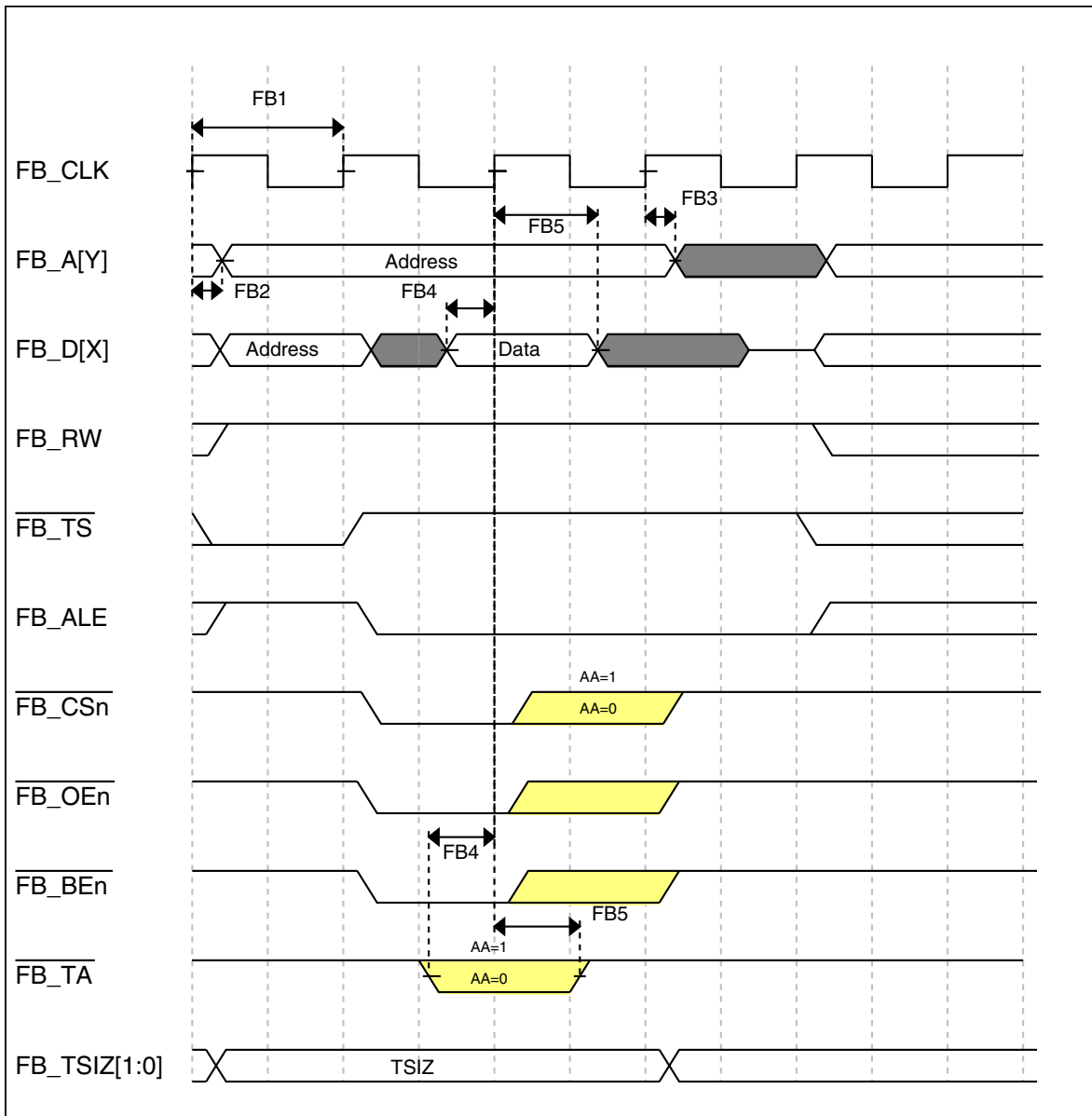


Figure 19. FlexBus read timing diagram

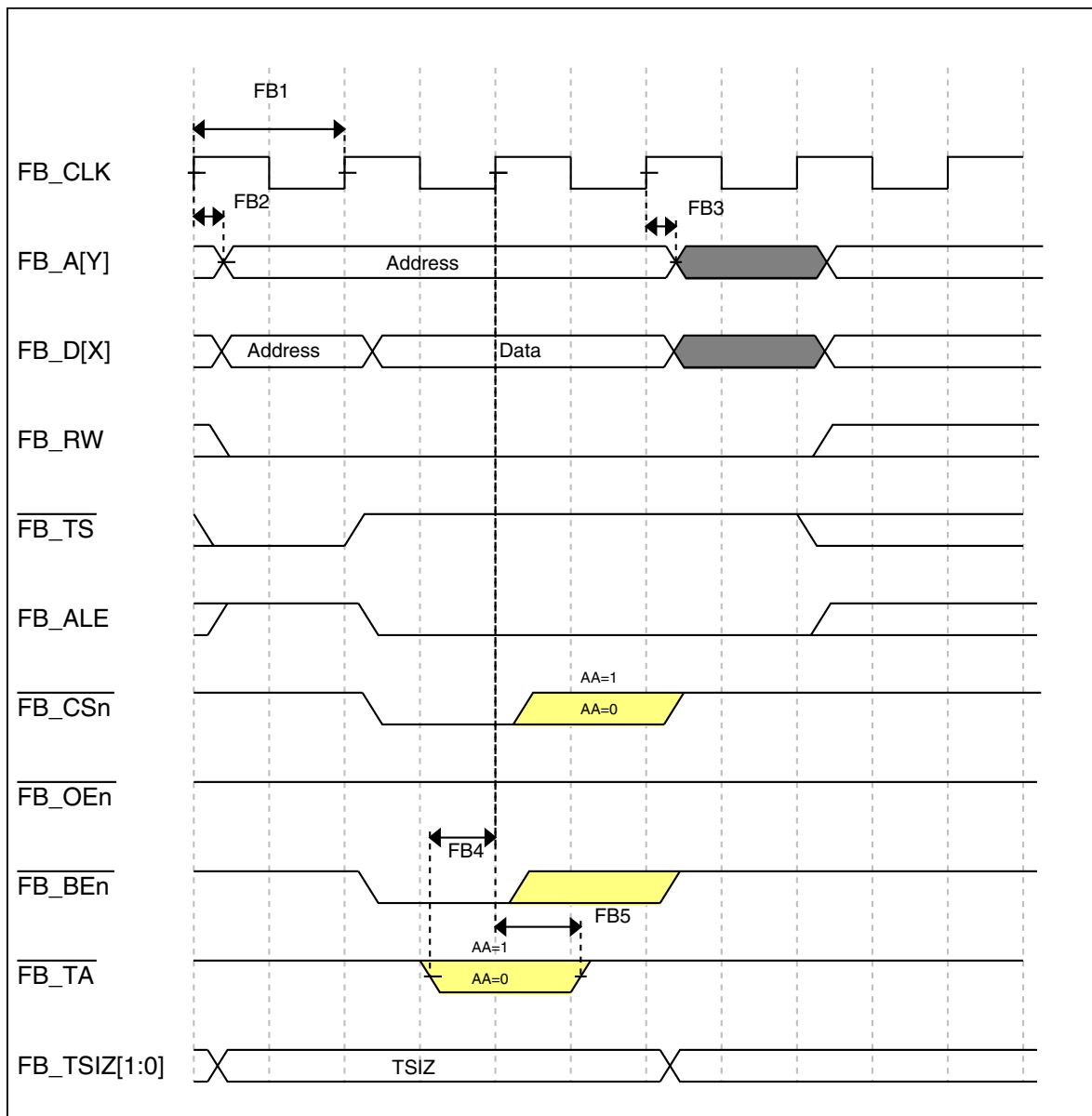


Figure 20. FlexBus write timing diagram

6.5 Security and integrity modules

6.5.1 DryIce Tamper Electrical Specifications

Table 28. DryIce Tamper Electrical Specifications

Symbol	Description	Min	Typ	Max	Unit	Notes
V _{BAT}	3.3V supply voltage	1.71		3.6	V	

Table continues on the next page...

Table 28. Drylce Tamper Electrical Specifications (continued)

Symbol	Description	Min	Typ	Max	Unit	Notes
I _{TAM}	Supply current					
	• clock tamper enabled		0.9	TBD	μA	
	• clock and voltage tamper enabled		1.01	TBD	μA	
	• clock, voltage and temperature tamper enabled		1.35	TBD	μA	
	EXTAL32 input clock		32.768		kHz	1
	Low Voltage Detect					
	• assertion	1.55	1.60	1.65	V	
	• negation	1.7	1.75	1.8	V	
	High Voltage Detect assertion	3.65	3.7	3.75	V	
	Voltage Tamper Detect operational temperature					
	• no false alarms	-50		150	°C	
	• with possible false alarms	-60		160	°C	
	Temperature Tamper Detect assertion					2
	• low temperature detect	-55		-45	°C	
	• high temperature detect	110		130	°C	
	Temperature Tamper Detect operational voltage					
	• no false alarms	1.6		3.7	V	
	• with possible false alarms	< 1.5		> 3.8	V	
	Clock Tamper Detect assertion					3
	• low frequency			20	kHz	
	• high frequency	40			kHz	
	• delay after loss of clock		2		ms	
	Clock Tamper Detect operational temperature					
	• no false alarms	-50		150	°C	
	• with possible false alarms	-60		160		
	Clock Tamper Detect operational voltage					
	• no false alarms	1.6		3.7	V	
	• with possible false alarms	< 1.5		> 3.8	V	

- EXTAL32 oscillator must be enabled before enabling Drylce tamper detect.
- Temperature tamper detector assertion/negation is refreshed each 28 EXTAL32 clock cycles.
- Clock tamper detector assertion/negation is refreshed each 28 EXTAL32 clock cycles.

6.6 Analog

6.6.1 ADC electrical specifications

The 16-bit accuracy specifications listed in [Table 29](#) and [Table 30](#) are achievable on the differential pins ADCx_DP0, ADCx_DM0.

The ADCx_DP2 and ADCx_DM2 ADC inputs are connected to the PGA outputs and are not direct device pins. Accuracy specifications for these pins are defined in [Table 31](#) and [Table 32](#).

All other ADC channels meet the 13-bit differential/12-bit single-ended accuracy specifications.

6.6.1.1 16-bit ADC operating conditions

Table 29. 16-bit ADC operating conditions

Symbol	Description	Conditions	Min.	Typ. ¹	Max.	Unit	Notes
V _{DDA}	Supply voltage	Absolute	1.71	—	3.6	V	
ΔV _{DDA}	Supply voltage	Delta to V _{DD} (V _{DD} -V _{DDA})	-100	0	+100	mV	2
ΔV _{SSA}	Ground voltage	Delta to V _{SS} (V _{SS} -V _{SSA})	-100	0	+100	mV	2
V _{REFH}	ADC reference voltage high		1.13	V _{DDA}	V _{DDA}	V	
V _{REFL}	Reference voltage low		V _{SSA}	V _{SSA}	V _{SSA}	V	
V _{ADIN}	Input voltage		V _{REFL}	—	V _{REFH}	V	
C _{ADIN}	Input capacitance	<ul style="list-style-type: none"> 16 bit modes 8/10/12 bit modes 	—	8	10	pF	
R _{ADIN}	Input resistance		—	2	5	kΩ	
R _{AS}	Analog source resistance	13/12 bit modes f _{ADCK} < 4MHz	—	—	5	kΩ	3
f _{ADCK}	ADC conversion clock frequency	≤ 13 bit modes	1.0	—	18.0	MHz	4
f _{ADCK}	ADC conversion clock frequency	16 bit modes	2.0	—	12.0	MHz	4

Table continues on the next page...

6.6.1.2 16-bit ADC electrical characteristics

Table 30. 16-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$)

Symbol	Description	Conditions ¹	Min.	Typ. ²	Max.	Unit	Notes
I_{DDA_ADC}	Supply current		0.215	—	1.7	mA	3
f_{ADACK}	ADC asynchronous clock source	• ADLPC=1, ADHSC=0	1.2	2.4	3.9	MHz	$t_{ADACK} = 1/f_{ADACK}$
		• ADLPC=1, ADHSC=1	3.0	4.0	7.3	MHz	
		• ADLPC=0, ADHSC=0	2.4	5.2	6.1	MHz	
		• ADLPC=0, ADHSC=1	4.4	6.2	9.5	MHz	
	Sample Time	See Reference Manual chapter for sample times					
TUE	Total unadjusted error	• 12 bit modes • <12 bit modes	— —	±4 ±1.4	±6.8 ±2.1	LSB ⁴	5
DNL	Differential non-linearity	• 12 bit modes • <12 bit modes	— —	±0.7 ±0.2	-1.1 to +1.9 -0.3 to 0.5	LSB ⁴	5
INL	Integral non-linearity	• 12 bit modes • <12 bit modes	— —	±1.0 ±0.5	-2.7 to +1.9 -0.7 to +0.5	LSB ⁴	5
E_{FS}	Full-scale error	• 12 bit modes • <12 bit modes	— —	-4 -1.4	-5.4 -1.8	LSB ⁴	$V_{ADIN} = V_{DDA}$ 5
E_Q	Quantization error	• 16 bit modes • ≤13 bit modes	— —	-1 to 0 —	— ±0.5	LSB ⁴	
ENOB	Effective number of bits	16 bit differential mode • Avg=32 • Avg=4 16 bit single-ended mode • Avg=32 • Avg=4	12.8 11.9 12.2 11.4	14.5 13.8 13.9 13.1	— — — —	bits bits bits bits	6
SINAD	Signal-to-noise plus distortion	See ENOB	6.02 × ENOB + 1.76			dB	
THD	Total harmonic distortion	16 bit differential mode • Avg=32 16 bit single-ended mode • Avg=32	— —	-94 -85	— —	dB dB	7

Table continues on the next page...

Table 30. 16-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

Symbol	Description	Conditions ¹	Min.	Typ. ²	Max.	Unit	Notes
SFDR	Spurious free dynamic range	16 bit differential mode • Avg=32	82	95	—	dB	7
		16 bit single-ended mode • Avg=32	78	90	—	dB	
E _{IL}	Input leakage error		$I_{in} \times R_{AS}$			mV	I _{in} = leakage current (refer to the MCU's voltage and current operating ratings)
	Temp sensor slope	−40°C to 105°C	—	1.715	—	mV/°C	
V _{TEMP25}	Temp sensor voltage	25°C	—	719	—	mV	

- All accuracy numbers assume the ADC is calibrated with $V_{REFH} = V_{DDA}$
- Typical values assume $V_{DDA} = 3.0$ V, Temp = 25°C, $f_{ADCK} = 2.0$ MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
- The ADC supply current depends on the ADC conversion clock speed, conversion rate and the ADLPC bit (low power). For lowest power operation the ADLPC bit should be set, the HSC bit should be clear with 1MHz ADC conversion clock speed.
- 1 LSB = $(V_{REFH} - V_{REFL})/2^N$
- ADC conversion clock <16MHz, Max hardware averaging (AVGE = %1, AVGS = %11)
- Input data is 100 Hz sine wave. ADC conversion clock <12MHz.
- Input data is 1 kHz sine wave. ADC conversion clock <12MHz.

Typical ADC 16-bit Differential ENOB vs ADC Clock
 100Hz, 90% FS Sine Input

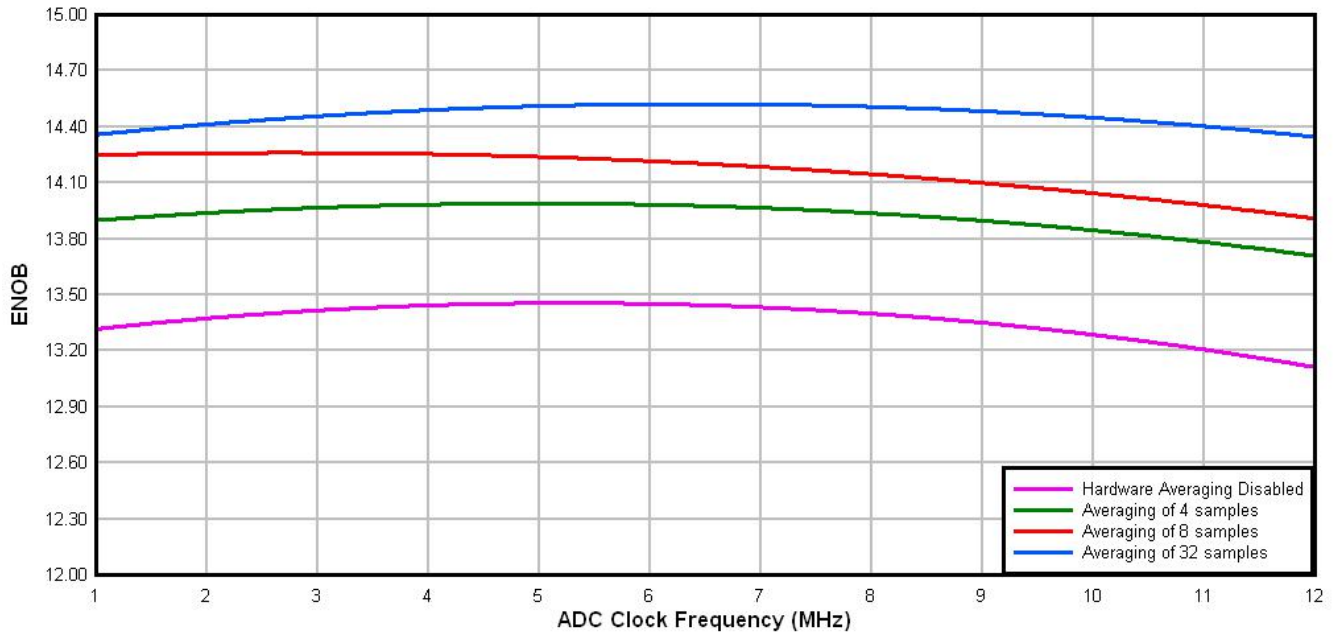


Figure 22. Typical ENOB vs. ADC_CLK for 16-bit differential mode

Typical ADC 16-bit Single-Ended ENOB vs ADC Clock
 100Hz, 90% FS Sine Input

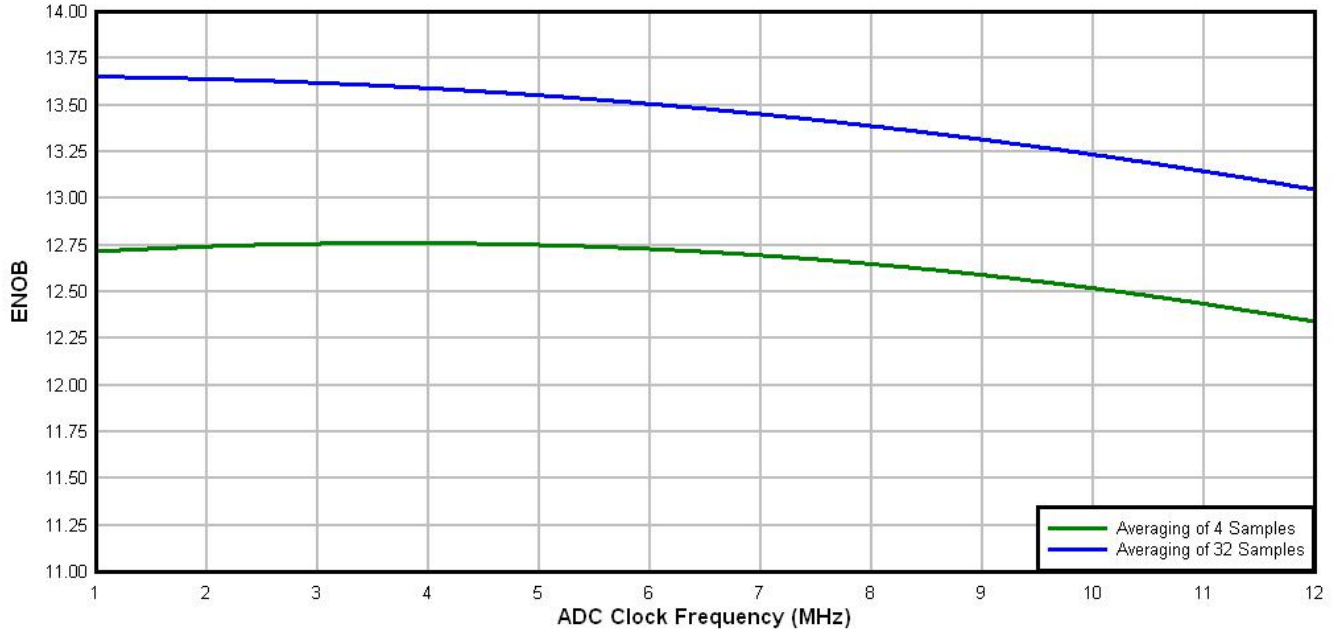


Figure 23. Typical ENOB vs. ADC_CLK for 16-bit single-ended mode

6.6.1.3 16-bit ADC with PGA operating conditions

Table 31. 16-bit ADC with PGA operating conditions

Symbol	Description	Conditions	Min.	Typ. ¹	Max.	Unit	Notes
V _{DDA}	Supply voltage	Absolute	1.71	—	3.6	V	
V _{REFPGA}	PGA ref voltage		VREF_OUT T	VREF_OUT T	VREF_OUT T	V	2, 3
V _{ADIN}	Input voltage		V _{SSA}	—	V _{DDA}	V	
V _{CM}	Input Common Mode range		V _{SSA}	—	V _{DDA}	V	
R _{PGAD}	Differential input impedance	Gain = 1, 2, 4, 8 Gain = 16, 32 Gain = 64	— — —	128 64 32	— — —	kΩ	IN+ to IN- ⁴
R _{AS}	Analog source resistance		—	100	—	Ω	5
T _S	ADC sampling time		1.25	—	—	μs	6
C _{rate}	ADC conversion rate	≤ 13 bit modes No ADC hardware averaging Continuous conversions enabled Peripheral clock = 50 MHz	18.484	—	450	Ksps	7
		16 bit modes No ADC hardware averaging Continuous conversions enabled Peripheral clock = 50 MHz	37.037	—	250	Ksps	8

1. Typical values assume V_{DDA} = 3.0 V, Temp = 25°C, f_{ADCK} = 6 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
2. ADC must be configured to use the internal voltage reference (VREF_OUT)
3. PGA reference is internally connected to the VREF_OUT pin. If the user wishes to drive VREF_OUT with a voltage other than the output of the VREF module, the VREF module must be disabled.
4. For single ended configurations the input impedance of the driven input is R_{PGAD}/2
5. The analog source resistance (R_{AS}), external to MCU, should be kept as minimum as possible. Increased R_{AS} causes drop in PGA gain without affecting other performances. This is not dependent on ADC clock frequency.
6. The minimum sampling time is dependent on input signal frequency and ADC mode of operation. A minimum of 1.25μs time should be allowed for F_{in}=4 kHz at 16-bit differential mode. Recommended ADC setting is: ADLSMP=1, ADLSTS=2 at 8 MHz ADC clock.
7. ADC clock = 18 MHz, ADLSMP = 1, ADLST = 00, ADHSC = 1
8. ADC clock = 12 MHz, ADLSMP = 1, ADLST = 01, ADHSC = 1

6.6.1.4 16-bit ADC with PGA characteristics

Table 32. 16-bit ADC with PGA characteristics

Symbol	Description	Conditions	Min.	Typ. ¹	Max.	Unit	Notes
I _{DDA_PGA}	Supply current	Low power (ADC_PGA[PGALPb]=0)	—	420	644	μA	2
I _{DC_PGA}	Input DC current		$\frac{2}{R_{PGAD}} \left(\frac{V_{REFPGA} \times 0.583 - V_{CM}}{\text{Gain} + 1} \right)$			A	3
		Gain =1, V _{REFPGA} =1.2V, V _{CM} =0.5V	—	1.54	—	μA	
		Gain =64, V _{REFPGA} =1.2V, V _{CM} =0.1V	—	0.57	—	μA	
G	Gain ⁴	• PGAG=0	0.95	1	1.05		R _{AS} < 100Ω
		• PGAG=1	1.9	2	2.1		
		• PGAG=2	3.8	4	4.2		
		• PGAG=3	7.6	8	8.4		
		• PGAG=4	15.2	16	16.6		
		• PGAG=5	30.0	31.6	33.2		
		• PGAG=6	58.8	63.3	67.8		
BW	Input signal bandwidth	• 16-bit modes	—	—	4	kHz	
		• < 16-bit modes	—	—	40	kHz	
PSRR	Power supply rejection ratio	Gain=1	—	-84	—	dB	V _{DDA} = 3V ±100mV, f _{VDDA} = 50Hz, 60Hz
CMRR	Common mode rejection ratio	• Gain=1	—	-84	—	dB	V _{CM} = 500mVpp, f _{VCM} = 50Hz, 100Hz
		• Gain=64	—	-85	—	dB	
V _{OFS}	Input offset voltage	• Chopping disabled (ADC_PGA[PGACHPb]=1)	—	2.4	TBD	mV	Output offset = V _{OFS} *(Gain+1)
		• Chopping enabled (ADC_PGA[PGACHPb]=0)	—	0.2	—	mV	
T _{GSW}	Gain switching settling time		—	—	10	μs	5
dG/dT	Gain drift over temperature	• Gain=1	—	TBD	TBD	ppm/°C	0 to 50°C
		• Gain=64	—	TBD	TBD	ppm/°C	
dV _{OFS} /dT	Offset drift over temperature	Gain=1	—	TBD	TBD	ppm/°C	0 to 50°C, ADC Averaging=32
dG/dV _{DDA}	Gain drift over supply voltage	• Gain=1	—	TBD	TBD	%/V	V _{DDA} from 1.71 to 3.6V
		• Gain=64	—	TBD	TBD	%/V	

Table continues on the next page...

Table 32. 16-bit ADC with PGA characteristics (continued)

Symbol	Description	Conditions	Min.	Typ. ¹	Max.	Unit	Notes
E_{IL}	Input leakage error	All modes	$I_{in} \times R_{AS}$			mV	I_{in} = leakage current (refer to the MCU's voltage and current operating ratings)
$V_{PP,DIFF}$	Maximum differential input signal swing		$\left(\frac{(\min(V_X, V_{DDA} - V_X) - 0.2) \times 4}{Gain}\right)$ where $V_X = V_{REFPGA} \times 0.583$			V	6
SNR	Signal-to-noise ratio	• Gain=1	80	90	—	dB	16-bit differential mode, Average=32
		• Gain=64	52	66	—	dB	
THD	Total harmonic distortion	• Gain=1	85	100	—	dB	16-bit differential mode, Average=32, $f_{in}=100\text{Hz}$
		• Gain=64	49	95	—	dB	
SFDR	Spurious free dynamic range	• Gain=1	85	105	—	dB	16-bit differential mode, Average=32, $f_{in}=100\text{Hz}$
		• Gain=64	53	88	—	dB	
ENOB	Effective number of bits	• Gain=1, Average=4	11.6	13.4	—	bits	16-bit differential mode, $f_{in}=100\text{Hz}$ z
		• Gain=1, Average=8	TBD	12.7	—	bits	
		• Gain=64, Average=4	7.2	9.6	—	bits	
		• Gain=64, Average=8	TBD	8.7	—	bits	
		• Gain=1, Average=32	12.8	14.5	—	bits	
		• Gain=2, Average=32	11.0	14.3	—	bits	
		• Gain=4, Average=32	7.9	13.8	—	bits	
		• Gain=8, Average=32	7.3	13.1	—	bits	
		• Gain=16, Average=32	6.8	12.5	—	bits	
		• Gain=32, Average=32	6.8	11.5	—	bits	
• Gain=64, Average=32	7.5	10.6	—	bits			
SINAD	Signal-to-noise plus distortion ratio	See ENOB	$6.02 \times \text{ENOB} + 1.76$			dB	

1. Typical values assume $V_{DDA} = 3.0\text{V}$, $\text{Temp} = 25^\circ\text{C}$, $f_{ADCK} = 6\text{MHz}$ unless otherwise stated.
2. This current is a PGA module adder, in addition to and ADC conversion currents.
3. Between $IN+$ and $IN-$. The PGA draws a DC current from the input terminals. The magnitude of the DC current is a strong function of input common mode voltage (V_{CM}) and the PGA gain.
4. $\text{Gain} = 2^{\text{PGAG}}$
5. After changing the PGA gain setting, a minimum of 2 ADC+PGA conversions should be ignored.

Peripheral operating requirements and behaviors

- Limit the input signal swing so that the PGA does not saturate during operation. Input signal swing is dependent on the PGA reference voltage and gain setting.

6.6.2 CMP and 6-bit DAC electrical specifications

Table 33. Comparator and 6-bit DAC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage	1.71	—	3.6	V
I_{DDHS}	Supply current, High-speed mode (EN=1, PMODE=1)	—	—	200	μ A
$I_{DDL S}$	Supply current, low-speed mode (EN=1, PMODE=0)	—	—	20	μ A
V_{AIN}	Analog input voltage	$V_{SS} - 0.3$	—	V_{DD}	V
V_{AIO}	Analog input offset voltage	—	—	20	mV
V_H	Analog comparator hysteresis ¹ <ul style="list-style-type: none"> • CR0[HYSTCTR] = 00 • CR0[HYSTCTR] = 01 • CR0[HYSTCTR] = 10 • CR0[HYSTCTR] = 11 	—	5	—	mV
		—	10	—	mV
		—	20	—	mV
		—	30	—	mV
V_{CMPOH}	Output high	$V_{DD} - 0.5$	—	—	V
V_{CMPOI}	Output low	—	—	0.5	V
t_{DHS}	Propagation delay, high-speed mode (EN=1, PMODE=1)	20	50	200	ns
t_{DLS}	Propagation delay, low-speed mode (EN=1, PMODE=0)	80	250	600	ns
	Analog comparator initialization delay ²	—	—	40	μ s
I_{DAC6b}	6-bit DAC current adder (enabled)	—	7	—	μ A
INL	6-bit DAC integral non-linearity	-0.5	—	0.5	LSB ³
DNL	6-bit DAC differential non-linearity	-0.3	—	0.3	LSB

- Typical hysteresis is measured with input voltage range limited to 0.6 to $V_{DD}-0.6V$.
- Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to DACEN, VRSEL, PSEL, MSEL, VOSEL) and the comparator output settling to a stable level.
- 1 LSB = $V_{reference}/64$

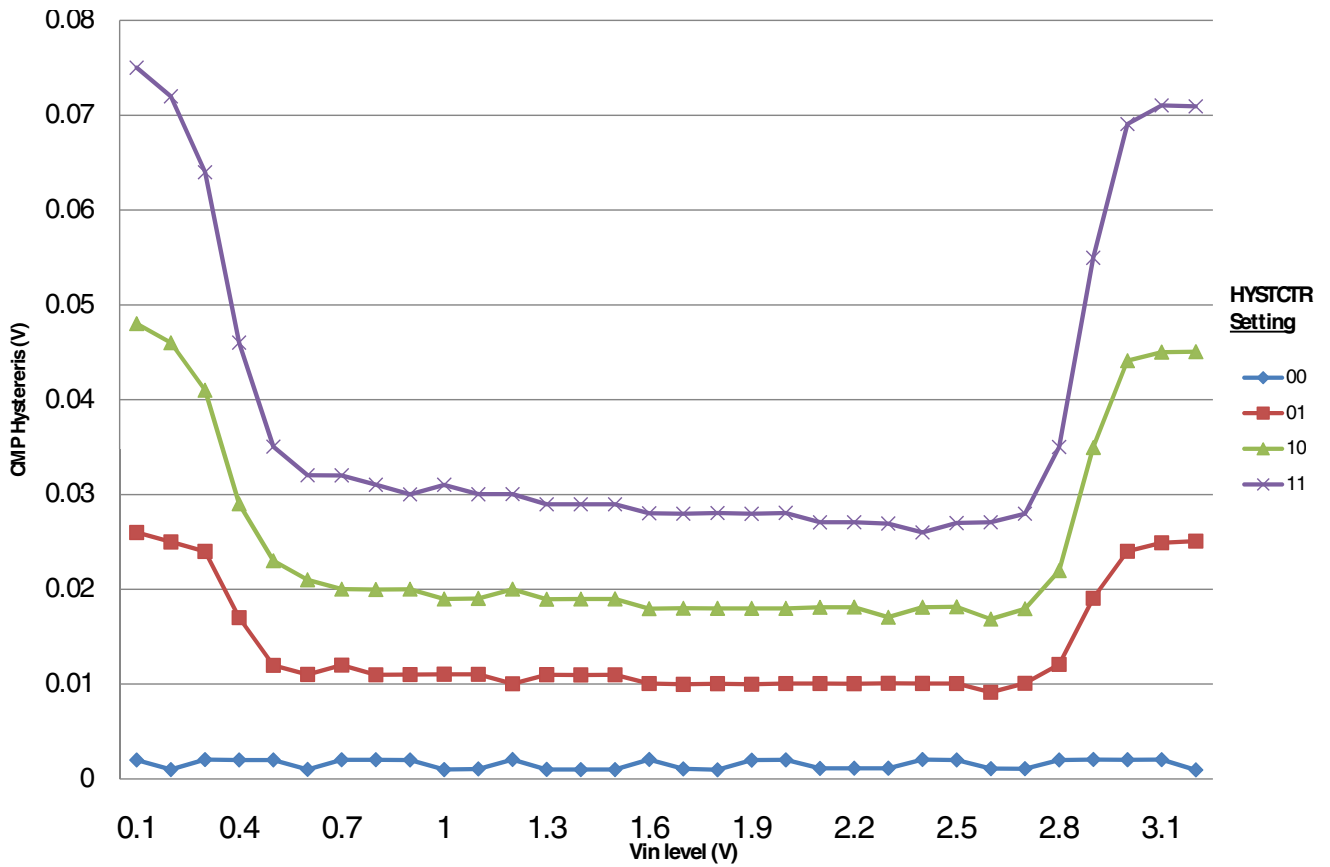


Figure 24. Typical hysteresis vs. Vin level (VDD=3.3V, PMODE=0)

Peripheral operating requirements and behaviors

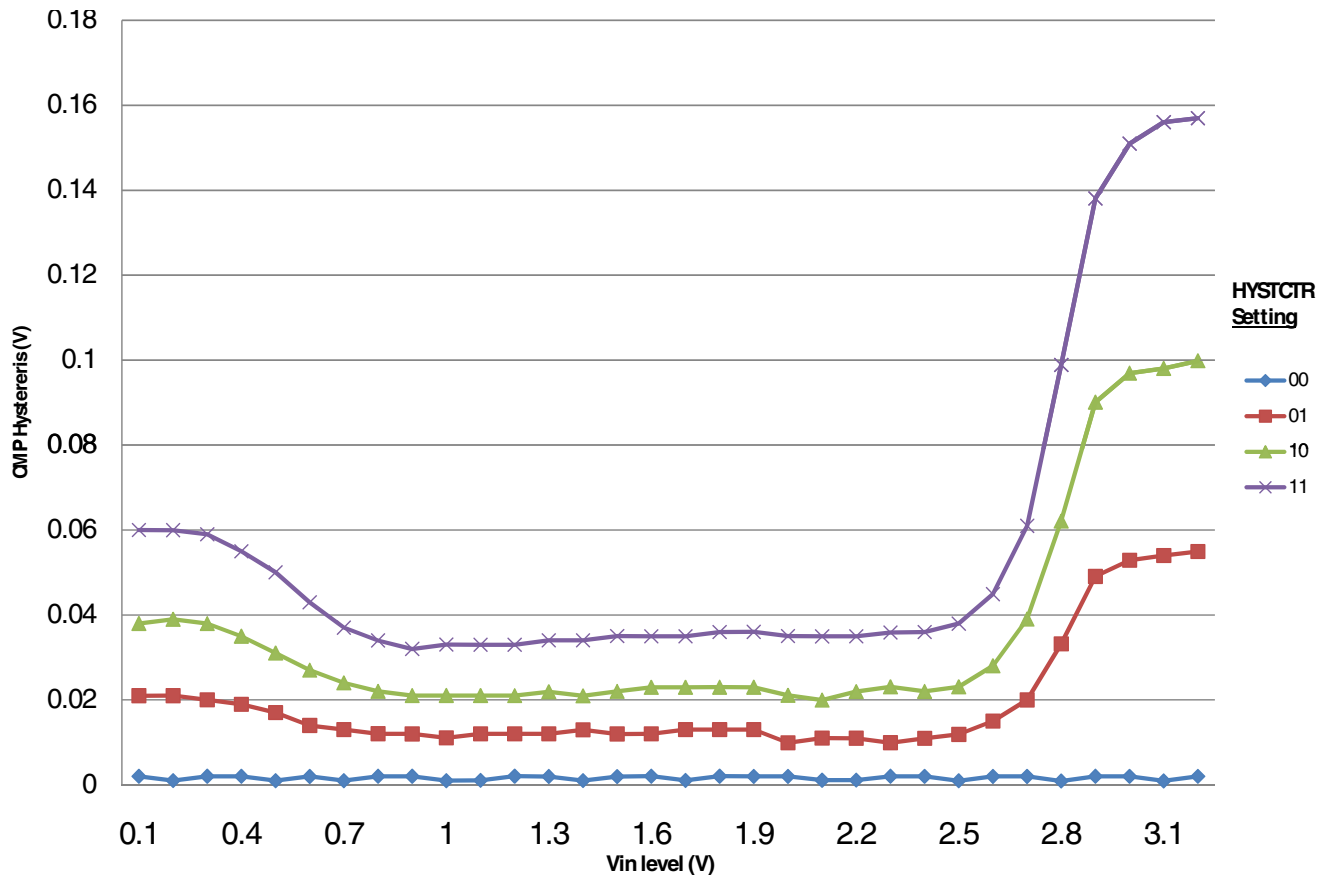


Figure 25. Typical hysteresis vs. Vin level (VDD=3.3V, PMODE=1)

6.6.3 12-bit DAC electrical characteristics

6.6.3.1 12-bit DAC operating requirements

Table 34. 12-bit DAC operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DDA}	Supply voltage	1.71	3.6	V	
V_{DACR}	Reference voltage	1.13	3.6	V	1
T_A	Temperature	-40	105	°C	
C_L	Output load capacitance	—	100	pF	2
I_L	Output load current	—	1	mA	

1. The DAC reference can be selected to be VDDA or the voltage output of the VREF module (VREF_OUT)
2. A small load capacitance (47 pF) can improve the bandwidth performance of the DAC

6.6.3.2 12-bit DAC operating behaviors

Table 35. 12-bit DAC operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$I_{DDA_DACL_P}$	Supply current — low-power mode	—	—	150	μA	
$I_{DDA_DAC_HP}$	Supply current — high-speed mode	—	—	700	μA	
t_{DACLP}	Full-scale settling time (0x080 to 0xF7F) — low-power mode	—	100	200	μs	1
t_{DACHP}	Full-scale settling time (0x080 to 0xF7F) — high-power mode	—	15	30	μs	1
$t_{CCDACLP}$	Code-to-code settling time (0xBF8 to 0xC08) — low-power mode and high-speed mode	—	0.7	1	μs	1
$V_{dacoutl}$	DAC output voltage range low — high-speed mode, no load, DAC set to 0x000	—	—	100	mV	
$V_{dacouth}$	DAC output voltage range high — high-speed mode, no load, DAC set to 0xFFF	$V_{DACR} - 100$	—	V_{DACR}	mV	
INL	Integral non-linearity error — high speed mode	—	—	± 8	LSB	2
DNL	Differential non-linearity error — $V_{DACR} > 2\text{ V}$	—	—	± 1	LSB	3
DNL	Differential non-linearity error — $V_{DACR} = V_{REF_OUT}$	—	—	± 1	LSB	4
V_{OFFSET}	Offset error	—	± 0.4	± 0.8	%FSR	5
E_G	Gain error	—	± 0.1	± 0.6	%FSR	5
PSRR	Power supply rejection ratio, $V_{DDA} > 2.4\text{ V}$	60	—	90	dB	
T_{CO}	Temperature coefficient offset voltage	—	3.7	—	$\mu\text{V}/\text{C}$	6
T_{GE}	Temperature coefficient gain error	—	0.000421	—	%FSR/C	
Rop	Output resistance load = 3 k Ω	—	—	250	Ω	
SR	Slew rate -80h → F7Fh → 80h <ul style="list-style-type: none"> High power (SP_{HP}) Low power (SP_{LP}) 	1.2 0.05	1.7 0.12	— —	V/ μs	
CT	Channel to channel cross talk	—	—	-80	dB	
BW	3dB bandwidth <ul style="list-style-type: none"> High power (SP_{HP}) Low power (SP_{LP}) 	550 40	— —	— —	kHz	

1. Settling within ± 1 LSB
2. The INL is measured for 0+100mV to $V_{DACR} - 100\text{ mV}$
3. The DNL is measured for 0+100 mV to $V_{DACR} - 100\text{ mV}$
4. The DNL is measured for 0+100mV to $V_{DACR} - 100\text{ mV}$ with $V_{DDA} > 2.4\text{V}$
5. Calculated by a best fit curve from $V_{SS} + 100\text{ mV}$ to $V_{DACR} - 100\text{ mV}$

Peripheral operating requirements and behaviors

- 6. VDDA = 3.0V, reference select set for VDDA (DACx_CO:DACRFS = 1), high power mode(DACx_C0:LPEN = 0), DAC set to 0x800, Temp range from -40C to 105C

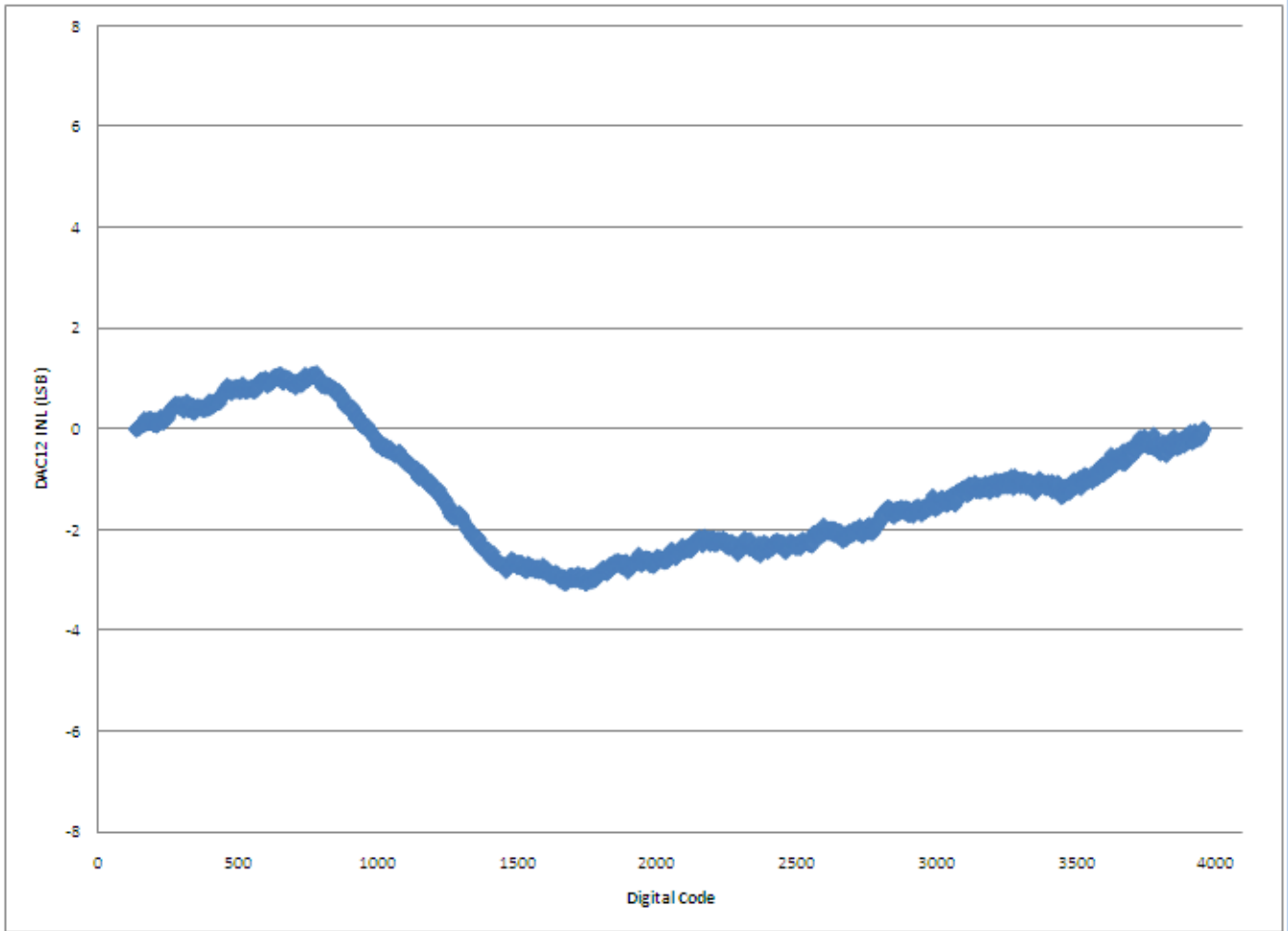


Figure 26. Typical INL error vs. digital code



Figure 27. Offset at half scale vs. temperature

6.6.4 Voltage reference electrical specifications

Table 36. VREF full-range operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DDA}	Supply voltage	1.71	3.6	V	
T_A	Temperature	-40	105	°C	
C_L	Output load capacitance	100		nF	1, 2

1. C_L must be connected to VREF_OUT if the VREF_OUT functionality is being used for either an internal or external reference.
2. The load capacitance should not exceed +/-25% of the nominal specified C_L value over the operating temperature range of the device.

Table 37. VREF full-range operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{out}	Voltage reference output with factory trim at nominal V_{DDA} and temperature=25C	1.1965	1.2	1.2027	V	
V_{out}	Voltage reference output with— factory trim	1.1584	—	1.2376	V	
V_{out}	Voltage reference output — user trim	1.198	—	1.202	V	
V_{step}	Voltage reference trim step	—	0.5	—	mV	
V_{tdrift}	Temperature drift ($V_{max} - V_{min}$ across the full temperature range)	—	—	80	mV	
I_{bg}	Bandgap only current	—	—	80	μ A	1
I_{tr}	High-power buffer current	—	—	TBD	mA	1
ΔV_{LOAD}	Load regulation <ul style="list-style-type: none"> current = + 1.0 mA current = - 1.0 mA 	— —	2 5	— —	mV	1, 2
T_{stup}	Buffer startup time	—	—	100	μ s	
V_{vdrift}	Voltage drift ($V_{max} - V_{min}$ across the full voltage range)	—	2	—	mV	1

1. See the chip's Reference Manual for the appropriate settings of the VREF Status and Control register.
2. Load regulation voltage is the difference between the VREF_OUT voltage with no load vs. voltage with defined load

Table 38. VREF limited-range operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
T_A	Temperature	0	50	$^{\circ}$ C	

Table 39. VREF limited-range operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
V_{out}	Voltage reference output with factory trim	1.173	1.225	V	

6.7 Timers

See [General switching specifications](#).

6.8 Communication interfaces

6.8.1 Ethernet switching specifications

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface.

6.8.1.1 MII signal switching specifications

The following timing specs meet the requirements for MII style interfaces for a range of transceiver devices.

Table 40. MII signal switching specifications

Symbol	Description	Min.	Max.	Unit
—	RXCLK frequency	—	25	MHz
MII1	RXCLK pulse width high	35%	65%	RXCLK period
MII2	RXCLK pulse width low	35%	65%	RXCLK period
MII3	RXD[3:0], RXDV, RXER to RXCLK setup	5	—	ns
MII4	RXCLK to RXD[3:0], RXDV, RXER hold	5	—	ns
—	TXCLK frequency	—	25	MHz
MII5	TXCLK pulse width high	35%	65%	TXCLK period
MII6	TXCLK pulse width low	35%	65%	TXCLK period
MII7	TXCLK to TXD[3:0], TXEN, TXER invalid	2	—	ns
MII8	TXCLK to TXD[3:0], TXEN, TXER valid	—	25	ns

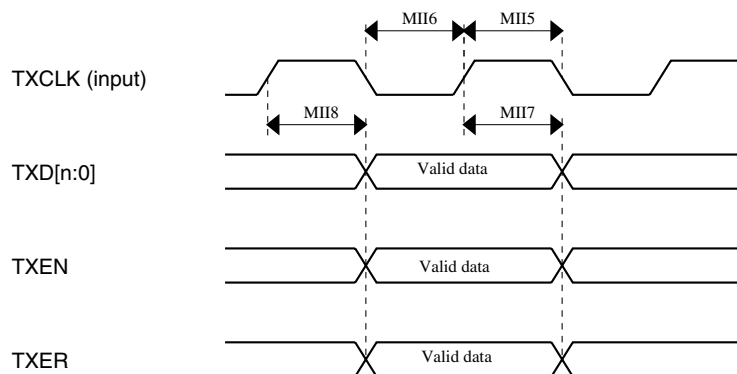


Figure 28. MII transmit signal timing diagram

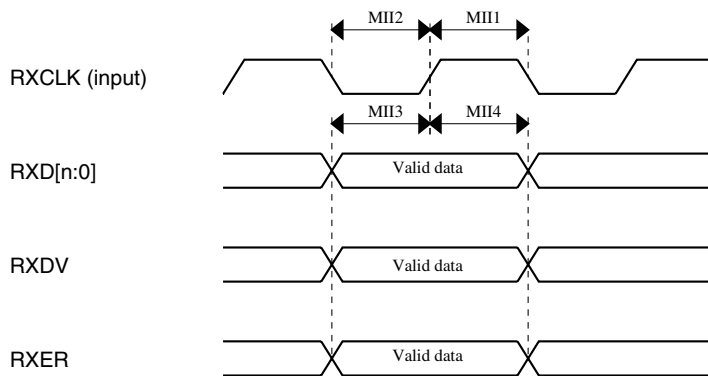


Figure 29. MII receive signal timing diagram

6.8.1.2 RMII signal switching specifications

The following timing specs meet the requirements for RMII style interfaces for a range of transceiver devices.

Table 41. RMII signal switching specifications

Num	Description	Min.	Max.	Unit
—	EXTAL frequency (RMII input clock RMII_CLK)	—	50	MHz
RMII1	RMII_CLK pulse width high	35%	65%	RMII_CLK period
RMII2	RMII_CLK pulse width low	35%	65%	RMII_CLK period
RMII3	RXD[1:0], CRS_DV, RXER to RMII_CLK setup	4	—	ns
RMII4	RMII_CLK to RXD[1:0], CRS_DV, RXER hold	2	—	ns
RMII7	RMII_CLK to TXD[1:0], TXEN invalid	4	—	ns
RMII8	RMII_CLK to TXD[1:0], TXEN valid	—	15	ns

6.8.2 USB electrical specifications

The USB electricals for the USB On-the-Go module conform to the standards documented by the Universal Serial Bus Implementers Forum. For the most up-to-date standards, visit <http://www.usb.org>.

6.8.3 USB DCD electrical specifications

Table 42. USB DCD electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V _{DP_SRC}	USB_DP source voltage (up to 250 μ A)	0.5	—	0.7	V
V _{LGC}	Threshold voltage for logic high	0.8	—	2.0	V
I _{DP_SRC}	USB_DP source current	7	10	13	μ A
I _{DM_SINK}	USB_DM sink current	50	100	150	μ A
R _{DM_DWN}	D- pulldown resistance for data pin contact detect	14.25	—	24.8	k Ω
V _{DAT_REF}	Data detect voltage	0.25	0.325	0.4	V

6.8.4 USB VREG electrical specifications

Table 43. USB VREG electrical specifications

Symbol	Description	Min.	Typ. ¹	Max.	Unit	Notes
V _{REGIN}	Input supply voltage	2.7	—	5.5	V	
I _{DDon}	Quiescent current — Run mode, load current equal zero, input supply (V _{REGIN}) > 3.6 V	—	120	186	μ A	
I _{DDstby}	Quiescent current — Standby mode, load current equal zero	—	1.1	1.54	μ A	
I _{DDoff}	Quiescent current — Shutdown mode <ul style="list-style-type: none"> V_{REGIN} = 5.0 V and temperature=25C Across operating voltage and temperature 	—	650	—	nA	
		—	—	4	μ A	
I _{LOADrun}	Maximum load current — Run mode	—	—	120	mA	
I _{LOADstby}	Maximum load current — Standby mode	—	—	1	mA	
V _{Reg33out}	Regulator output voltage — Input supply (V _{REGIN}) > 3.6 V <ul style="list-style-type: none"> Run mode Standby mode 	3	3.3	3.6	V	
		2.1	2.8	3.6	V	
V _{Reg33out}	Regulator output voltage — Input supply (V _{REGIN}) < 3.6 V, pass-through mode	2.1	—	3.6	V	2
C _{OUT}	External output capacitor	1.76	2.2	8.16	μ F	
ESR	External output capacitor equivalent series resistance	1	—	100	m Ω	
I _{LIM}	Short circuit current	—	290	—	mA	

1. Typical values assume V_{REGIN} = 5.0 V, Temp = 25 °C unless otherwise stated.

2. Operating in pass-through mode: regulator output voltage equal to the input voltage minus a drop proportional to I_{Load}.

6.8.5 ULPI timing specifications

The ULPI interface is fully compliant with the industry standard UTMI+ Low Pin Interface. Control and data timing requirements for the ULPI pins are given in the following table. These timings apply to synchronous mode only. All timings are measured with respect to the clock as seen at the USB_CLKIN pin.

Table 44. ULPI timing specifications

Num	Description	Min.	Typ.	Max.	Unit
	USB_CLKIN operating frequency	—	60	—	MHz
	USB_CLKIN duty cycle	—	50	—	%
U1	USB_CLKIN clock period	—	16.67	—	ns
U2	Input setup (control and data)	5	—	—	ns
U3	Input hold (control and data)	1	—	—	ns
U4	Output valid (control and data)	—	—	9.5	ns
U5	Output hold (control and data)	1	—	—	ns

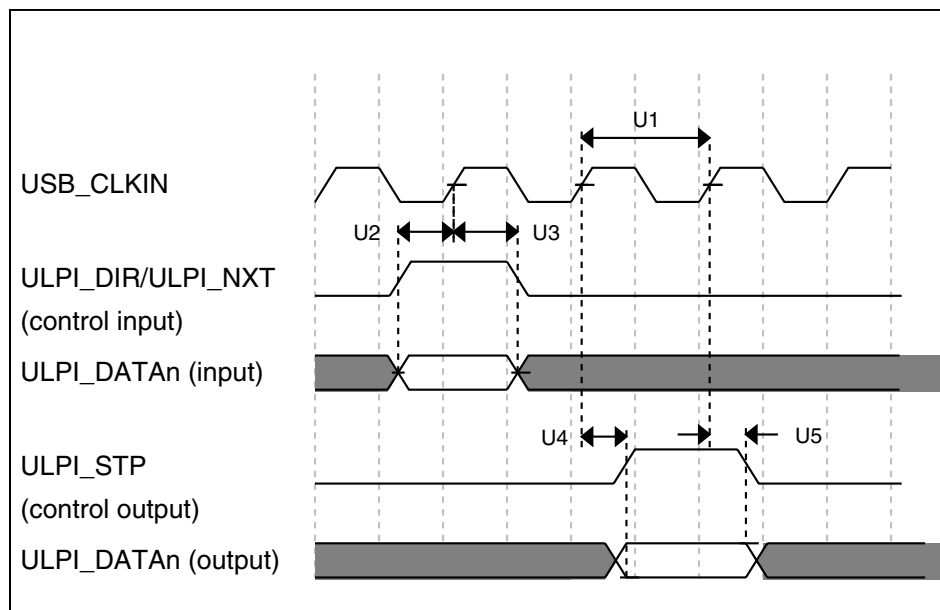


Figure 30. ULPI timing diagram

6.8.6 CAN switching specifications

See [General switching specifications](#).

6.8.7 DSPI switching specifications (limited voltage range)

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provide DSPI timing characteristics for classic SPI timing modes. Refer to the DSPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

Table 45. Master mode DSPI timing (limited voltage range)

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	2.7	3.6	V	
	Frequency of operation	—	30	MHz	
DS1	DSPI_SCK output cycle time	$2 \times t_{BUS}$	—	ns	
DS2	DSPI_SCK output high/low time	$(t_{SCK}/2) - 2$	$(t_{SCK}/2) + 2$	ns	
DS3	DSPI_PCSn valid to DSPI_SCK delay	$(t_{BUS} \times 2) - 2$	—	ns	1
DS4	DSPI_SCK to DSPI_PCSn invalid delay	$(t_{BUS} \times 2) - 2$	—	ns	2
DS5	DSPI_SCK to DSPI_SOUT valid	—	8.5	ns	
DS6	DSPI_SCK to DSPI_SOUT invalid	-2	—	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	15	—	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	—	ns	

1. The delay is programmable in SPIx_CTARn[PSSCK] and SPIx_CTARn[CSSCK].
2. The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC].

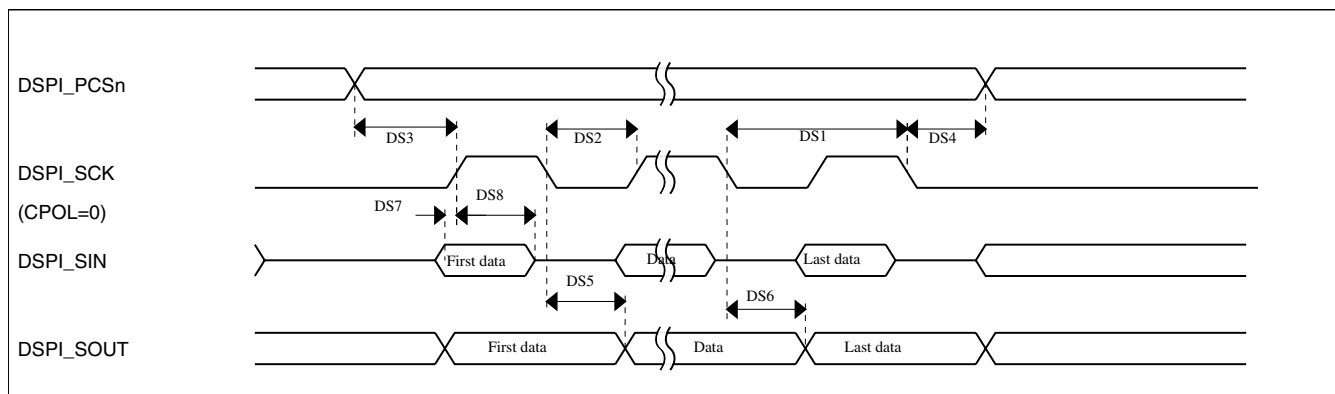


Figure 31. DSPI classic SPI timing — master mode

Table 46. Slave mode DSPI timing (limited voltage range)

Num	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
	Frequency of operation		15	MHz
DS9	DSPI_SCK input cycle time	4 x t _{BUS}	—	ns
DS10	DSPI_SCK input high/low time	(t _{SCK/2}) - 2	(t _{SCK/2}) + 2	ns
DS11	DSPI_SCK to DSPI_SOUT valid	—	10	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns
DS13	DSPI_SIN to DSPI_SCK input setup	2	—	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7	—	ns
DS15	$\overline{\text{DSPI_SS}}$ active to DSPI_SOUT driven	—	14	ns
DS16	$\overline{\text{DSPI_SS}}$ inactive to DSPI_SOUT not driven	—	14	ns

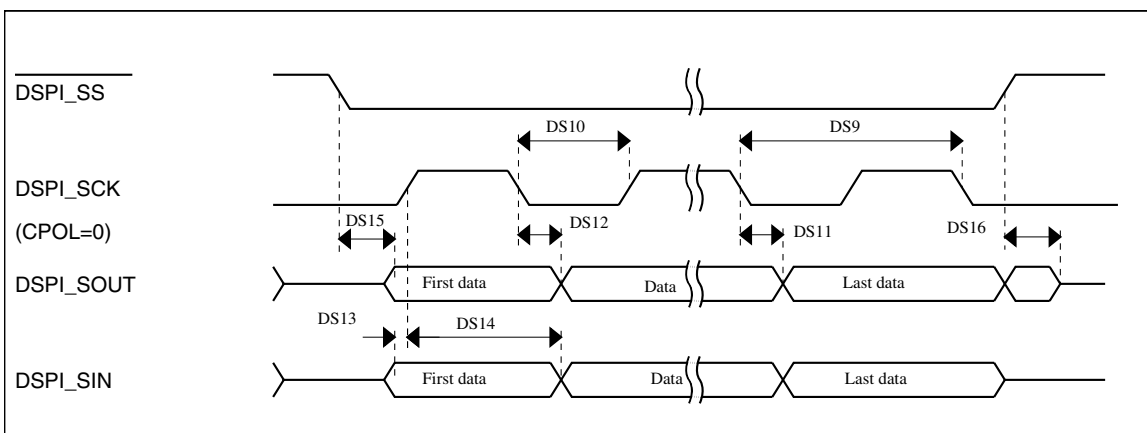


Figure 32. DSPI classic SPI timing — slave mode

6.8.8 DSPI switching specifications (full voltage range)

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provides DSPI timing characteristics for classic SPI timing modes. Refer to the DSPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

Table 47. Master mode DSPI timing (full voltage range)

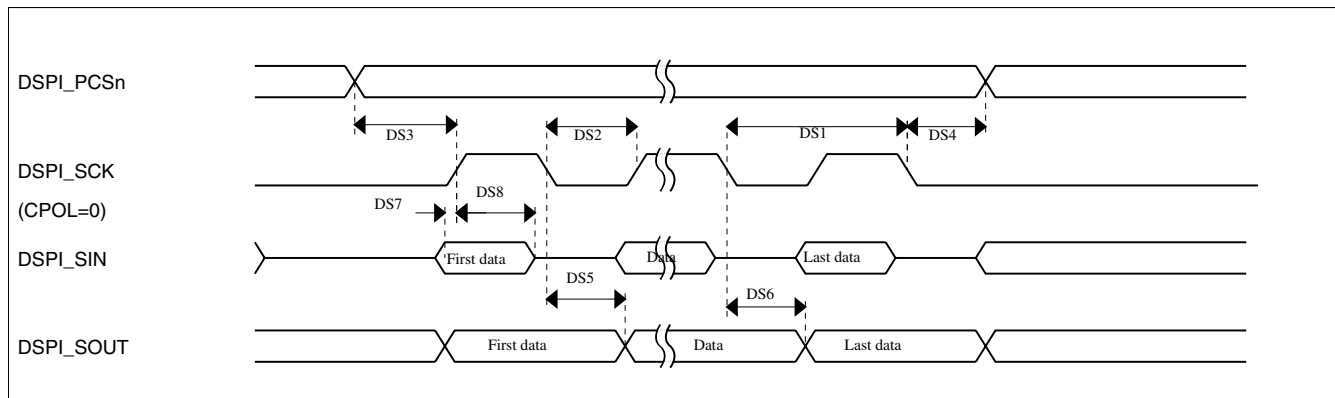
Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	1.71	3.6	V	1
	Frequency of operation	—	15	MHz	

Table continues on the next page...

Table 47. Master mode DSPI timing (full voltage range) (continued)

Num	Description	Min.	Max.	Unit	Notes
DS1	DSPI_SCK output cycle time	$4 \times t_{BUS}$	—	ns	
DS2	DSPI_SCK output high/low time	$(t_{SCK}/2) - 4$	$(t_{SCK}/2) + 4$	ns	
DS3	DSPI_PCSn valid to DSPI_SCK delay	$(t_{BUS} \times 2) - 4$	—	ns	2
DS4	DSPI_SCK to DSPI_PCSn invalid delay	$(t_{BUS} \times 2) - 4$	—	ns	3
DS5	DSPI_SCK to DSPI_SOUT valid	—	10	ns	
DS6	DSPI_SCK to DSPI_SOUT invalid	-4.5	—	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	20.5	—	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	—	ns	

1. The DSPI module can operate across the entire operating voltage for the processor, but to run across the full voltage range the maximum frequency of operation is reduced.
2. The delay is programmable in SPIx_CTARn[PSSCK] and SPIx_CTARn[CSSCK].
3. The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC].

**Figure 33. DSPI classic SPI timing — master mode****Table 48. Slave mode DSPI timing (full voltage range)**

Num	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
	Frequency of operation	—	7.5	MHz
DS9	DSPI_SCK input cycle time	$8 \times t_{BUS}$	—	ns
DS10	DSPI_SCK input high/low time	$(t_{SCK}/2) - 4$	$(t_{SCK}/2) + 4$	ns
DS11	DSPI_SCK to DSPI_SOUT valid	—	20	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns
DS13	DSPI_SIN to DSPI_SCK input setup	2	—	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7	—	ns
DS15	DSPI_SS active to DSPI_SOUT driven	—	19	ns

Table continues on the next page...

Table 48. Slave mode DSPI timing (full voltage range) (continued)

Num	Description	Min.	Max.	Unit
DS16	$\overline{\text{DSPI_SS}}$ inactive to DSPI_SOUT not driven	—	19	ns

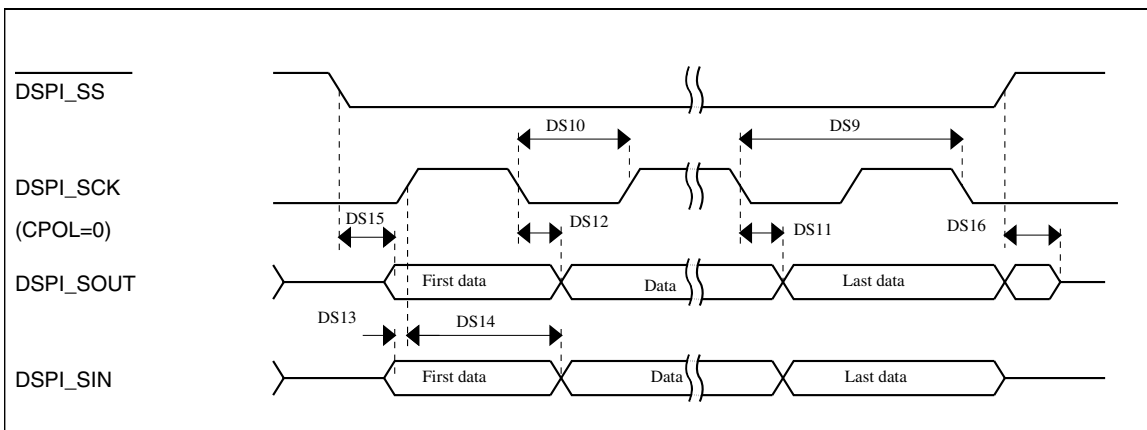


Figure 34. DSPI classic SPI timing — slave mode

6.8.9 I²C switching specifications

See [General switching specifications](#).

6.8.10 UART switching specifications

See [General switching specifications](#).

6.8.11 SDHC specifications

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface.

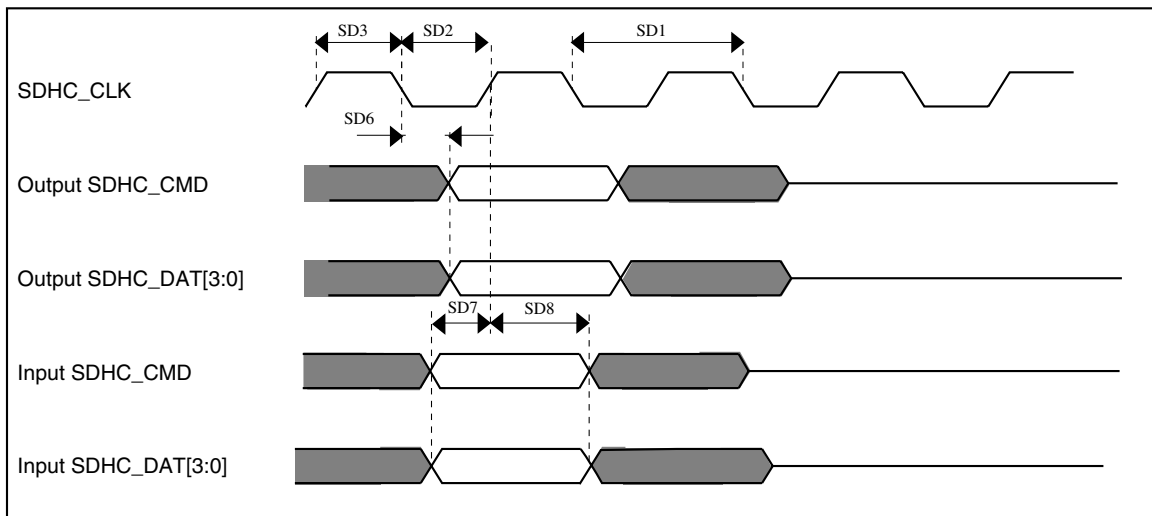
Table 49. SDHC switching specifications

Num	Symbol	Description	Min.	Max.	Unit
		Operating voltage	2.7	3.6	V
Card input clock					

Table continues on the next page...

**Table 49. SDHC switching specifications
(continued)**

Num	Symbol	Description	Min.	Max.	Unit
SD1	f _{pp}	Clock frequency (low speed)	0	400	kHz
	f _{pp}	Clock frequency (SD\SDIO full speed)	0	25	MHz
	f _{pp}	Clock frequency (MMC full speed)	0	20	MHz
	f _{OD}	Clock frequency (identification mode)	0	400	kHz
SD2	t _{WL}	Clock low time	7	—	ns
SD3	t _{WH}	Clock high time	7	—	ns
SD4	t _{TLH}	Clock rise time	—	3	ns
SD5	t _{THL}	Clock fall time	—	3	ns
SDHC output / card inputs SDHC_CMD, SDHC_DAT (reference to SDHC_CLK)					
SD6	t _{OD}	SDHC output delay (output valid)	-5	6.5	ns
SDHC input / card inputs SDHC_CMD, SDHC_DAT (reference to SDHC_CLK)					
SD7	t _{ISU}	SDHC input setup time	5	—	ns
SD8	t _{IH}	SDHC input hold time	0	—	ns

**Figure 35. SDHC timing**

6.8.12 I2S/SAI Switching Specifications

This section provides the AC timing for the I2S/SAI module in master mode (clocks are driven) and slave mode (clocks are input). All timing is given for noninverted serial clock polarity (TCR2[BCP] is 0, RCR2[BCP] is 0) and a noninverted frame sync (TCR4[FSP]

is 0, RCR4[FSP] is 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the bit clock signal (BCLK) and/or the frame sync (FS) signal shown in the following figures.

Table 50. I2S/SAI master mode timing

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S1	I2S_MCLK cycle time ¹	40		ns
S2	I2S_MCLK pulse width high/low	45%	55%	MCLK period
S3	I2S_TX_BCLK cycle time (output) ¹ I2S_RX_BCLK cycle time (output) ¹	80 160	— —	ns
S4	I2S_TX_BCLK pulse width high/low	45%	55%	BCLK period
S5	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output valid	—	15	ns
S6	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output invalid	0	—	ns
S7	I2S_TX_BCLK to I2S_TXD valid	—	15	ns
S8	I2S_TX_BCLK to I2S_TXD invalid	0	—	ns
S9	I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK	25	—	ns
S10	I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK	0	—	ns
S11	I2S_TX_FS input assertion to I2S_TXD output valid ²	—	21	ns

1. This parameter is limited in VLPx modes.
2. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear

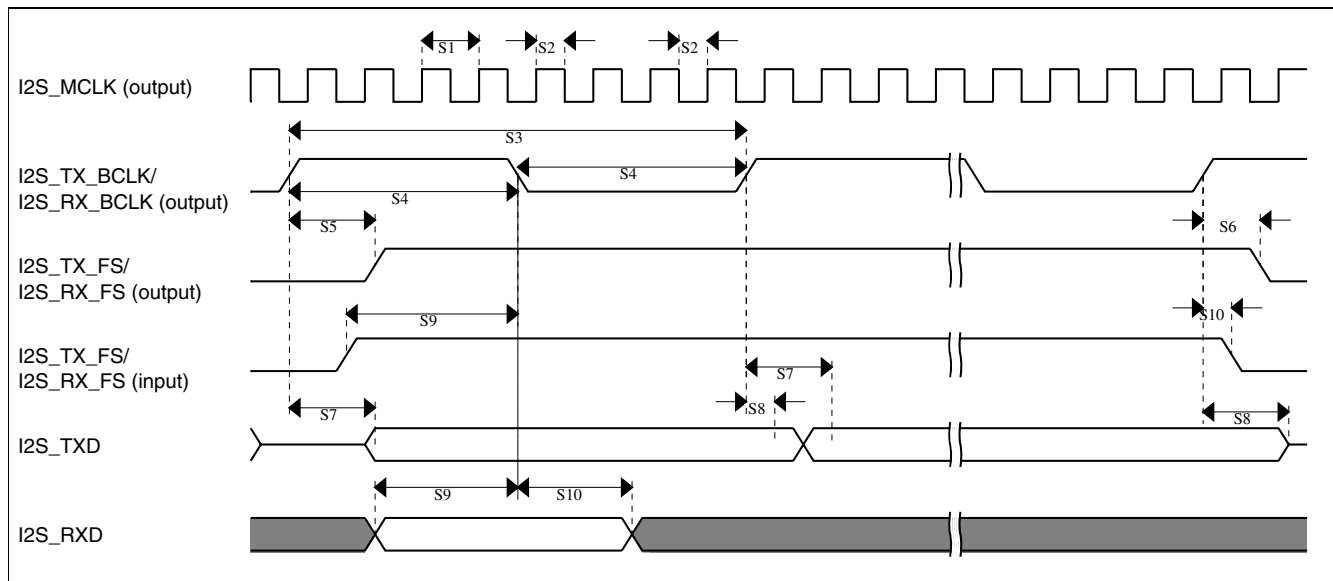
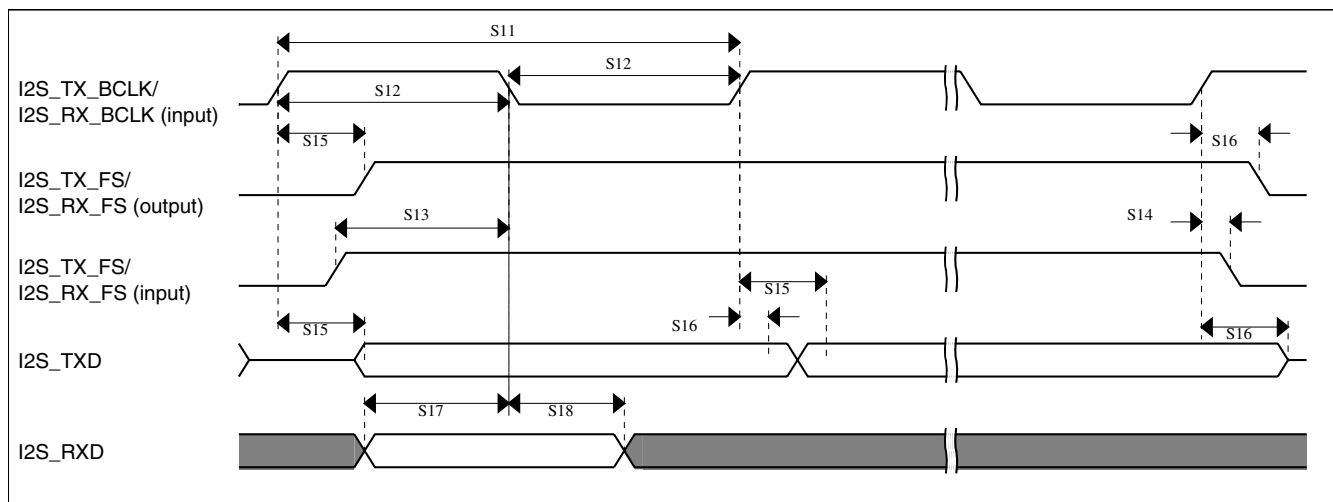


Figure 36. I2S/SAI timing — master modes

Table 51. I2S/SAI slave mode timing

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S11	I2S_RX_BCLK cycle time (input) I2S_TX_BCLK cycle time (input)	80	—	ns
S12	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input)	45%	55%	MCLK period
S13	I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK	10	—	ns
S14	I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK	2	—	ns
S15	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid	—	29	ns
S16	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid	0	—	ns
S17	I2S_RXD setup before I2S_RX_BCLK	10	—	ns
S18	I2S_RXD hold after I2S_RX_BCLK	2	—	ns
S19	I2S_TX_FS input assertion to I2S_TXD output valid ¹	—	21	ns

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear

**Figure 37. I2S/SAI timing — slave modes**

6.9 Human-machine interfaces (HMI)

6.9.1 TSI electrical specifications

Table 52. TSI electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V _{DDTSI}	Operating voltage	1.71	—	3.6	V	
C _{ELE}	Target electrode capacitance range	1	20	500	pF	1
f _{REFmax}	Reference oscillator frequency	—	8	TBD	MHz	2
f _{ELEmax}	Electrode oscillator frequency	—	0.5	TBD	MHz	2
C _{REF}	Internal reference capacitor	TBD	1	TBD	pF	
V _{DELTA}	Oscillator delta voltage	TBD	600	TBD	mV	2
I _{REF}	Reference oscillator current source base current <ul style="list-style-type: none"> • 1uA setting (REFCHRG=0) • 32uA setting (REFCHRG=31) 	— —	1.133 36	1.5 50	μA	2, 3
I _{ELE}	Electrode oscillator current source base current <ul style="list-style-type: none"> • 1uA setting (EXTCHRG=0) • 32uA setting (EXTCHRG=31) 	— —	1.133 36	1.5 50	μA	2, 4
Pres5	Electrode capacitance measurement precision	—	8.3333	38.4	pF/count	5
Pres20	Electrode capacitance measurement precision	—	8.3333	38.4	pF/count	6
Pres100	Electrode capacitance measurement precision	—	8.3333	38.4	pF/count	7
MaxSens	Maximum sensitivity	0.003	12.5	—	fF/count	8
Res	Resolution	—	—	16	bits	
T _{Con20}	Response time @ 20 pF	8	15	25	μs	9
I _{TSI_RUN}	Current added in run mode	—	55	—	μA	
I _{TSI_LP}	Low power mode current adder	—	1.3	TBD	μA	10

1. The TSI module is functional with capacitance values outside this range. However, optimal performance is not guaranteed.
2. Fixed external capacitance of 20 pF.
3. The programmable current source value is generated by multiplying the SCANC[REFCHRG] value and the base current.
4. The programmable current source value is generated by multiplying the SCANC[EXTCHRG] value and the base current.
5. Measured with a 5 pF electrode, reference oscillator frequency of 10 MHz, PS = 128, NSCN = 8; I_{ext} = 16.
6. Measured with a 20 pF electrode, reference oscillator frequency of 10 MHz, PS = 128, NSCN = 2; I_{ext} = 16.
7. Measured with a 20 pF electrode, reference oscillator frequency of 10 MHz, PS = 16, NSCN = 3; I_{ext} = 16.
8. Sensitivity defines the minimum capacitance change when a single count from the TSI module changes, it is equal to (C_{ref} * I_{ext})/(I_{ref} * PS * NSCN). Sensitivity depends on the configuration used. The typical value listed is based on the following configuration: I_{ext} = 5 μA, EXTCHRG = 4, PS = 128, NSCN = 2, I_{ref} = 16 μA, REFCHRG = 15, C_{ref} = 1.0 pF. The minimum sensitivity describes the smallest possible capacitance that can be measured by a single count (this is the best sensitivity but is described as a minimum because it's the smallest number). The minimum sensitivity parameter is based on the following configuration: I_{ext} = 1 μA, EXTCHRG = 0, PS = 128, NSCN = 32, I_{ref} = 32 μA, REFCHRG = 31, C_{ref} = 0.5 pF
9. Time to do one complete measurement of the electrode. Sensitivity resolution of 0.0133 pF, PS = 0, NSCN = 0, 1 electrode, EXTCHRG = 15.
10. REFCHRG=0, EXTCHRG=4, PS=7, NSCN=0F, LPSCNITV=F, LPO is selected (1 kHz), and fixed external capacitance of 20 pF. Data is captured with an average of 7 periods window.

7 Dimensions

7.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to <http://www.freescale.com> and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number
256-pin MAPBGA	98ASA00346D

8 Pinout

8.1 K61 Signal Multiplexing and Pin Assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

256 MAP BGA	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
E2	PTE0	ADC1_SE4a	ADC1_SE4a	PTE0	SPI1_PCS1	UART1_TX	SDHC0_D1		I2C1_SDA	RTC_CLKOUT	
F2	PTE1/LLWU_P0	ADC1_SE5a	ADC1_SE5a	PTE1/LLWU_P0	SPI1_SOUT	UART1_RX	SDHC0_D0		I2C1_SCL	SPI1_SIN	
F3	PTE2/LLWU_P1	ADC1_SE6a	ADC1_SE6a	PTE2/LLWU_P1	SPI1_SCK	UART1_CTS_b	SDHC0_DCLK				
G2	PTE3	ADC1_SE7a	ADC1_SE7a	PTE3	SPI1_SIN	UART1_RTS_b	SDHC0_CMD			SPI1_SOUT	
G7	VDD	VDD	VDD								
H7	VDDINT	VDDINT	VDDINT								
H8	VSS	VSS	VSS								
F1	PTF17	DISABLED		PTF17	SPI2_SCK	FTM0_CH4	UART0_RX				
G1	PTF18	DISABLED		PTF18	SPI2_SOUT	FTM1_CH0	UART0_TX				
G3	PTE4/LLWU_P2	DISABLED		PTE4/LLWU_P2	SPI1_PCS0	UART3_TX	SDHC0_D3				
G4	PTE5	DISABLED		PTE5	SPI1_PCS2	UART3_RX	SDHC0_D2		FTM3_CH0		
H2	PTE6	DISABLED		PTE6	SPI1_PCS3	UART3_CTS_b	I2S0_MCLK		FTM3_CH1	USB_SOF_OUT	
H1	PTF19	DISABLED		PTF19	SPI2_SIN	FTM1_CH1	UART5_RX				
H5	PTF20	DISABLED		PTF20	SPI2_PCS1	FTM2_CH0	UART5_TX				

Pinout

256 MAP BGA	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
H3	PTE7	DISABLED		PTE7		UART3_RTS_b	I2S0_RXD0		FTM3_CH2		
H4	PTE8	ADC2_SE16	ADC2_SE16	PTE8	I2S0_RXD1	UART5_TX	I2S0_RX_FS		FTM3_CH3		
J1	PTE9	ADC2_SE17	ADC2_SE17	PTE9	I2S0_TXD1	UART5_RX	I2S0_RX_BCLK		FTM3_CH4		
J2	PTE10	DISABLED		PTE10		UART5_CTS_b	I2S0_TXD0		FTM3_CH5		
K1	PTE11	ADC3_SE16	ADC3_SE16	PTE11		UART5_RTS_b	I2S0_TX_FS		FTM3_CH6		
K3	PTE12	ADC3_SE17	ADC3_SE17	PTE12			I2S0_TX_BCLK		FTM3_CH7		
G8	VDD	VDD	VDD								
H9	VSS	VSS	VSS								
J3	PTE16	ADC0_SE4a	ADC0_SE4a	PTE16	SPI0_PCS0	UART2_TX	FTM_CLKIN0		FTM0_FLT3		
K2	PTE17	ADC0_SE5a	ADC0_SE5a	PTE17	SPI0_SCK	UART2_RX	FTM_CLKIN1		LPTMR0_ALT3		
L4	PTE18	ADC0_SE6a	ADC0_SE6a	PTE18	SPI0_SOUT	UART2_CTS_b	I2C0_SDA				
M3	PTE19	ADC0_SE7a	ADC0_SE7a	PTE19	SPI0_SIN	UART2_RTS_b	I2C0_SCL		CMP3_OUT		
L2	VSS	VSS	VSS								
M1	USB0_DP	USB0_DP	USB0_DP								
M2	USB0_DM	USB0_DM	USB0_DM								
L1	VOUT33	VOUT33	VOUT33								
L3	VREGIN	VREGIN	VREGIN								
N1	PGA2_DP/ ADC2_DP0/ ADC3_DP3/ ADC0_DP1	PGA2_DP/ ADC2_DP0/ ADC3_DP3/ ADC0_DP1	PGA2_DP/ ADC2_DP0/ ADC3_DP3/ ADC0_DP1								
N2	PGA2_DM/ ADC2_DM0/ ADC3_DM3/ ADC0_DM1	PGA2_DM/ ADC2_DM0/ ADC3_DM3/ ADC0_DM1	PGA2_DM/ ADC2_DM0/ ADC3_DM3/ ADC0_DM1								
P1	PGA3_DP/ ADC3_DP0/ ADC2_DP3/ ADC1_DP1	PGA3_DP/ ADC3_DP0/ ADC2_DP3/ ADC1_DP1	PGA3_DP/ ADC3_DP0/ ADC2_DP3/ ADC1_DP1								
P2	PGA3_DM/ ADC3_DM0/ ADC2_DM3/ ADC1_DM1	PGA3_DM/ ADC3_DM0/ ADC2_DM3/ ADC1_DM1	PGA3_DM/ ADC3_DM0/ ADC2_DM3/ ADC1_DM1								
R1	PGA0_DP/ ADC0_DP0/ ADC1_DP3	PGA0_DP/ ADC0_DP0/ ADC1_DP3	PGA0_DP/ ADC0_DP0/ ADC1_DP3								
R2	PGA0_DM/ ADC0_DM0/ ADC1_DM3	PGA0_DM/ ADC0_DM0/ ADC1_DM3	PGA0_DM/ ADC0_DM0/ ADC1_DM3								

256 MAP BGA	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
T1	PGA1_DP/ ADC1_DP0/ ADC0_DP3	PGA1_DP/ ADC1_DP0/ ADC0_DP3	PGA1_DP/ ADC1_DP0/ ADC0_DP3								
T2	PGA1_DM/ ADC1_DM0/ ADC0_DM3	PGA1_DM/ ADC1_DM0/ ADC0_DM3	PGA1_DM/ ADC1_DM0/ ADC0_DM3								
N5	VDDA	VDDA	VDDA								
P4	VREFH	VREFH	VREFH								
M4	VREFL	VREFL	VREFL								
N4	VSSA	VSSA	VSSA								
P3	ADC1_SE16/ CMP2_IN2/ ADC0_SE22	ADC1_SE16/ CMP2_IN2/ ADC0_SE22	ADC1_SE16/ CMP2_IN2/ ADC0_SE22								
N3	ADC0_SE16/ CMP1_IN2/ ADC0_SE21	ADC0_SE16/ CMP1_IN2/ ADC0_SE21	ADC0_SE16/ CMP1_IN2/ ADC0_SE21								
T3	VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_SE18	VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_SE18	VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_SE18								
R3	DAC0_OUT/ CMP1_IN3/ ADC0_SE23	DAC0_OUT/ CMP1_IN3/ ADC0_SE23	DAC0_OUT/ CMP1_IN3/ ADC0_SE23								
R4	DAC1_OUT/ CMP0_IN4/ CMP2_IN3/ ADC1_SE23	DAC1_OUT/ CMP0_IN4/ CMP2_IN3/ ADC1_SE23	DAC1_OUT/ CMP0_IN4/ CMP2_IN3/ ADC1_SE23								
M5	TAMPER0/ RTC_WAKE UP_B	TAMPER0/ RTC_WAKE UP_B	TAMPER0/ RTC_WAKE UP_B								
L5	TAMPER1	TAMPER1	TAMPER1								
L6	TAMPER2	TAMPER2	TAMPER2								
R5	TAMPER3	TAMPER3	TAMPER3								
P6	TAMPER4	TAMPER4	TAMPER4								
R6	TAMPER5	TAMPER5	TAMPER5								
T6	XTAL32	XTAL32	XTAL32								
T5	EXTAL32	EXTAL32	EXTAL32								
P5	VBAT	VBAT	VBAT								
N6	TAMPER6	TAMPER6	TAMPER6								
M6	TAMPER7	TAMPER7	TAMPER7								
G9	VDD	VDD	VDD								
H10	VDDINT	VDDINT	VDDINT								
J8	VSS	VSS	VSS								
P7	PTE24	ADC0_SE17/ EXTAL1	ADC0_SE17/ EXTAL1	PTE24	CAN1_TX	UART4_TX	I2S1_TX_FS		EWM_OUT_ b	I2S1_RXD1	

Pinout

256 MAP BGA	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
R7	PTE25	ADC0_SE18/ XTAL1	ADC0_SE18/ XTAL1	PTE25	CAN1_RX	UART4_RX	I2S1_TX_BC LK		EWM_IN	I2S1_TXD1	
M7	PTE26	ADC3_SE5b	ADC3_SE5b	PTE26	ENET_1588 _CLKIN	UART4_CTS _b	I2S1_TXD0		RTC_CLKO UT	USB_CLKIN	
K7	PTE27	ADC3_SE4b	ADC3_SE4b	PTE27		UART4_RTS _b	I2S1_MCLK				
L7	PTE28	ADC3_SE7a	ADC3_SE7a	PTE28							
T7	PTA0	JTAG_TCLK/ SWD_CLK/ EZP_CLK	TSIO_CH1	PTA0	UART0_CTS _b/ UART0_COL _b	FTM0_CH5				JTAG_TCLK/ SWD_CLK	EZP_CLK
N8	PTA1	JTAG_TDI/ EZP_DI	TSIO_CH2	PTA1	UART0_RX	FTM0_CH6				JTAG_TDI	EZP_DI
T8	PTA2	JTAG_TDO/ TRACE_SW O/EZP_DO	TSIO_CH3	PTA2	UART0_TX	FTM0_CH7				JTAG_TDO/ TRACE_SW O	EZP_DO
P8	PTA3	JTAG_TMS/ SWD_DIO	TSIO_CH4	PTA3	UART0_RTS _b	FTM0_CH0				JTAG_TMS/ SWD_DIO	
R8	PTA4/ LLWU_P3	NMI_b/ EZP_CS_b	TSIO_CH5	PTA4/ LLWU_P3		FTM0_CH1				NMI_b	EZP_CS_b
T12	PTA5	DISABLED		PTA5	USB_CLKIN	FTM0_CH2	RMII0_RXE R/ MII0_RXER	CMP2_OUT	I2S0_TX_BC LK	JTAG_TRST _b	
G10	VDD	VDD	VDD								
J9	VSS	VSS	VSS								
P9	PTF21	ADC3_SE6b	ADC3_SE6b	PTF21		FTM2_CH1	UART5_RTS _b				
N9	PTF22	ADC3_SE7b	ADC3_SE7b	PTF22	I2C0_SCL	FTM1_CH0	UART5_CTS _b				
R12	PTA6	ADC3_SE6a	ADC3_SE6a	PTA6	ULPI_CLK	FTM0_CH3	I2S1_RXD0			TRACE_CLK OUT	
P12	PTA7	ADC0_SE10	ADC0_SE10	PTA7	ULPI_DIR	FTM0_CH4	I2S1_RX_BC LK			TRACE_D3	
N12	PTA8	ADC0_SE11	ADC0_SE11	PTA8	ULPI_NXT	FTM1_CH0	I2S1_RX_FS		FTM1_QD_P HA	TRACE_D2	
T13	PTA9	ADC3_SE5a	ADC3_SE5a	PTA9	ULPI_STP	FTM1_CH1	MII0_RXD3		FTM1_QD_P HB	TRACE_D1	
P13	PTA10	ADC3_SE4a	ADC3_SE4a	PTA10	ULPI_DATA 0	FTM2_CH0	MII0_RXD2		FTM2_QD_P HA	TRACE_D0	
R13	PTA11	ADC3_SE15	ADC3_SE15	PTA11	ULPI_DATA 1	FTM2_CH1	MII0_RXCLK		FTM2_QD_P HB		
M10	PTA12	CMP2_IN0	CMP2_IN0	PTA12	CAN0_TX	FTM1_CH0	RMII0_RXD1 /MII0_RXD1		I2S0_TXD0	FTM1_QD_P HA	
N10	PTA13/ LLWU_P4	CMP2_IN1	CMP2_IN1	PTA13/ LLWU_P4	CAN0_RX	FTM1_CH1	RMII0_RXD0 /MII0_RXD0		I2S0_TX_FS	FTM1_QD_P HB	
R11	PTA14	CMP3_IN0	CMP3_IN0	PTA14	SPI0_PCS0	UART0_TX	RMII0_CRS DV/ MII0_RXDV		I2S0_RX_BC LK	I2S0_TXD1	

256 MAP BGA	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
P11	PTA15	CMP3_IN1	CMP3_IN1	PTA15	SPI0_SCK	UART0_RX	RMII0_TXEN /MII0_TXEN		I2S0_RXD0		
T14	VSS	VSS	VSS								
N11	PTA16	CMP3_IN2	CMP3_IN2	PTA16	SPI0_SOUT	UART0_CTS _b/ UART0_COL _b	RMII0_TXD0 /MII0_TXD0		I2S0_RX_FS	I2S0_RXD1	
T11	PTA17	ADC1_SE17	ADC1_SE17	PTA17	SPI0_SIN	UART0_RTS _b	RMII0_TXD1 /MII0_TXD1		I2S0_MCLK		
P10	PTF23	ADC3_SE10	ADC3_SE10	PTF23	I2C0_SDA	FTM1_CH1			TRACE_CLK OUT		
R10	PTF24	ADC3_SE11	ADC3_SE11	PTF24	CAN1_RX	FTM1_QD_P HA			TRACE_D3		
R9	PTF25	ADC3_SE12	ADC3_SE12	PTF25	CAN1_TX	FTM1_QD_P HB			TRACE_D2		
T9	PTF26	ADC3_SE13	ADC3_SE13	PTF26		FTM2_QD_P HA			TRACE_D1		
T10	PTF27	ADC3_SE14	ADC3_SE14	PTF27		FTM2_QD_P HB			TRACE_D0		
J7	VDD	VDD	VDD								
K8	VSS	VSS	VSS								
T15	PTA18	EXTAL0	EXTAL0	PTA18		FTM0_FLT2	FTM_CLKIN 0				
T16	PTA19	XTAL0	XTAL0	PTA19		FTM1_FLT0	FTM_CLKIN 1		LPTMR0_AL T1		
R16	RESET_b	RESET_b	RESET_b								
N13	PTA24	CMP3_IN4	CMP3_IN4	PTA24	ULPI_DATA 2		MII0_TXD2		FB_A29		
R14	PTA25	CMP3_IN5	CMP3_IN5	PTA25	ULPI_DATA 3		MII0_TXCLK		FB_A28		
M13	PTA26	ADC2_SE15	ADC2_SE15	PTA26	ULPI_DATA 4		MII0_TXD3		FB_A27		
R15	PTA27	ADC2_SE14	ADC2_SE14	PTA27	ULPI_DATA 5		MII0_CRS		FB_A26		
P14	PTA28	ADC2_SE13	ADC2_SE13	PTA28	ULPI_DATA 6		MII0_TXER		FB_A25		
N14	PTA29	ADC2_SE12	ADC2_SE12	PTA29	ULPI_DATA 7		MII0_COL		FB_A24		
P16	PTF0	ADC2_SE11	ADC2_SE11	PTF0	CAN0_TX	FTM3_CH0		I2S1_RXD1			
L13	PTF1	ADC2_SE10	ADC2_SE10	PTF1	CAN0_RX	FTM3_CH1		I2S1_RX_BC LK			
M12	PTB0/ LLWU_P5	ADC0_SE8/ ADC1_SE8/ ADC2_SE8/ ADC3_SE8/ TSIO_CH0	ADC0_SE8/ ADC1_SE8/ ADC2_SE8/ ADC3_SE8/ TSIO_CH0	PTB0/ LLWU_P5	I2C0_SCL	FTM1_CH0	RMII0_MDIO /MII0_MDIO		FTM1_QD_P HA		

Pinout

256 MAP BGA	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
M11	PTB1	ADC0_SE9/ ADC1_SE9/ ADC2_SE9/ ADC3_SE9/ TSIO_CH6	ADC0_SE9/ ADC1_SE9/ ADC2_SE9/ ADC3_SE9/ TSIO_CH6	PTB1	I2C0_SDA	FTM1_CH1	RMII0_MDC/ MII0_MDC		FTM1_QD_P HB		
P15	PTB2	ADC0_SE12/ TSIO_CH7	ADC0_SE12/ TSIO_CH7	PTB2	I2C0_SCL	UART0_RTS _b	ENET0_158 8_TMR0		FTM0_FLT3		
M14	PTB3	ADC0_SE13/ TSIO_CH8	ADC0_SE13/ TSIO_CH8	PTB3	I2C0_SDA	UART0_CTS _b/ UART0_COL _b	ENET0_158 8_TMR1		FTM0_FLT0		
N15	PTB4	ADC1_SE10	ADC1_SE10	PTB4			ENET0_158 8_TMR2		FTM1_FLT0		
M15	PTB5	ADC1_SE11	ADC1_SE11	PTB5			ENET0_158 8_TMR3		FTM2_FLT0		
L14	PTB6	ADC1_SE12	ADC1_SE12	PTB6				FB_AD23			
L15	PTB7	ADC1_SE13	ADC1_SE13	PTB7				FB_AD22			
K14	PTB8	DISABLED		PTB8		UART3_RTS _b		FB_AD21			
K15	PTB9	DISABLED		PTB9	SPI1_PCS1	UART3_CTS _b		FB_AD20			
J13	PTB10	ADC1_SE14	ADC1_SE14	PTB10	SPI1_PCS0	UART3_RX	I2S1_TX_BC LK	FB_AD19	FTM0_FLT1		
J14	PTB11	ADC1_SE15	ADC1_SE15	PTB11	SPI1_SCK	UART3_TX	I2S1_TX_FS	FB_AD18	FTM0_FLT2		
K9	VSS	VSS	VSS								
J10	VDD	VDD	VDD								
N16	PTF2	ADC2_SE6a	ADC2_SE6a	PTF2	I2C1_SCL	FTM3_CH2		I2S1_RX_FS			
M16	PTF3	ADC2_SE7a	ADC2_SE7a	PTF3	I2C1_SDA	FTM3_CH3		I2S1_RXD0			
L16	PTF4	ADC2_SE4b	ADC2_SE4b	PTF4		FTM3_CH4		I2S1_TXD0			
J15	PTB16	TSIO_CH9	TSIO_CH9	PTB16	SPI1_SOUT	UART0_RX	I2S1_TXD0	FB_AD17	EWM_IN		
H13	PTB17	TSIO_CH10	TSIO_CH10	PTB17	SPI1_SIN	UART0_TX	I2S1_TXD1	FB_AD16	EWM_OUT_ b		
H14	PTB18	TSIO_CH11	TSIO_CH11	PTB18	CAN0_TX	FTM2_CH0	I2S0_TX_BC LK	FB_AD15	FTM2_QD_P HA		
K16	PTF5	ADC2_SE5b	ADC2_SE5b	PTF5		FTM3_CH5		I2S1_TX_FS			
J16	PTF6	ADC2_SE6b	ADC2_SE6b	PTF6		FTM3_CH6		I2S1_TX_BC LK			
H15	PTB19	TSIO_CH12	TSIO_CH12	PTB19	CAN0_RX	FTM2_CH1	I2S0_TX_FS	FB_OE_b	FTM2_QD_P HB		
G13	PTB20	ADC2_SE4a	ADC2_SE4a	PTB20	SPI2_PCS0			FB_AD31/ NFC_DATA1 5	CMP0_OUT		
G14	PTB21	ADC2_SE5a	ADC2_SE5a	PTB21	SPI2_SCK			FB_AD30/ NFC_DATA1 4	CMP1_OUT		

256 MAP BGA	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
G15	PTB22	DISABLED		PTB22	SPI2_SOUT			FB_AD29/ NFC_DATA1 3	CMP2_OUT		
H16	PTB23	DISABLED		PTB23	SPI2_SIN	SPI0_PCS5		FB_AD28/ NFC_DATA1 2	CMP3_OUT		
G16	PTC0	ADC0_SE14/ TSIO_CH13	ADC0_SE14/ TSIO_CH13	PTC0	SPI0_PCS4	PDB0_EXTR G		FB_AD14/ NFC_DATA1 1	I2S0_TXD1		
F13	PTC1/ LLWU_P6	ADC0_SE15/ TSIO_CH14	ADC0_SE15/ TSIO_CH14	PTC1/ LLWU_P6	SPI0_PCS3	UART1_RTS _b	FTM0_CH0	FB_AD13/ NFC_DATA1 0	I2S0_TXD0		
F14	PTC2	ADC0_SE4b/ CMP1_IN0/ TSIO_CH15	ADC0_SE4b/ CMP1_IN0/ TSIO_CH15	PTC2	SPI0_PCS2	UART1_CTS _b	FTM0_CH1	FB_AD12/ NFC_DATA9	I2S0_TX_FS		
E13	PTC3/ LLWU_P7	CMP1_IN1	CMP1_IN1	PTC3/ LLWU_P7	SPI0_PCS1	UART1_RX	FTM0_CH2	CLKOUT	I2S0_TX_BC LK		
F15	PTF7	ADC2_SE7b	ADC2_SE7b	PTF7		FTM3_CH7	UART3_RX	I2S1_TXD1			
L9	VSS	VSS	VSS								
K10	VDD	VDD	VDD								
F16	PTF8	DISABLED		PTF8		FTM3_FLT0	UART3_TX	I2S1_MCLK			
E14	PTC4/ LLWU_P8	DISABLED		PTC4/ LLWU_P8	SPI0_PCS0	UART1_TX	FTM0_CH3	FB_AD11/ NFC_DATA8	CMP1_OUT	I2S1_TX_BC LK	
E15	PTC5/ LLWU_P9	DISABLED		PTC5/ LLWU_P9	SPI0_SCK	LPTMR0_AL T2	I2S0_RXD0	FB_AD10/ NFC_DATA7	CMP0_OUT	I2S1_TX_FS	
F12	PTC6/ LLWU_P10	CMP0_IN0	CMP0_IN0	PTC6/ LLWU_P10	SPI0_SOUT	PDB0_EXTR G	I2S0_RX_BC LK	FB_AD9/ NFC_DATA6	I2S0_MCLK		
G12	PTC7	CMP0_IN1	CMP0_IN1	PTC7	SPI0_SIN	USB_SOF_ OUT	I2S0_RX_FS	FB_AD8/ NFC_DATA5			
H12	PTC8	ADC1_SE4b/ CMP0_IN2	ADC1_SE4b/ CMP0_IN2	PTC8		FTM3_CH4	I2S0_MCLK	FB_AD7/ NFC_DATA4			
F11	PTC9	ADC1_SE5b/ CMP0_IN3	ADC1_SE5b/ CMP0_IN3	PTC9		FTM3_CH5	I2S0_RX_BC LK	FB_AD6/ NFC_DATA3	FTM2_FLT0		
G11	PTC10	ADC1_SE6b	ADC1_SE6b	PTC10	I2C1_SCL	FTM3_CH6	I2S0_RX_FS	FB_AD5/ NFC_DATA2	I2S1_MCLK		
H11	PTC11/ LLWU_P11	ADC1_SE7b	ADC1_SE7b	PTC11/ LLWU_P11	I2C1_SDA	FTM3_CH7	I2S0_RXD1	FB_RW_b/ NFC_WE			
J12	PTC12	DISABLED		PTC12		UART4_RTS _b		FB_AD27	FTM3_FLT0		
K13	PTC13	DISABLED		PTC13		UART4_CTS _b		FB_AD26			
J11	PTC14	DISABLED		PTC14		UART4_RX		FB_AD25			
K12	PTF9	CMP2_IN4	CMP2_IN4	PTF9			UART3_RTS _b				
L12	PTF10	CMP2_IN5	CMP2_IN5	PTF10			UART3_CTS _b				
F10	PTC15	DISABLED		PTC15		UART4_TX		FB_AD24			

Pinout

256 MAP BGA	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
N7	VSS	VSS	VSS								
L10	VDD	VDD	VDD								
K11	PTF11	DISABLED		PTF11			UART2_RTS_b				
L11	PTF12	DISABLED		PTF12			UART2_CTS_b				
F9	PTC16	DISABLED		PTC16	CAN1_RX	UART3_RX	ENET0_158_8_TMR0	FB_CS5_b/ FB_TSIZ1/ FB_BE23_16_b	NFC_RB		
E9	PTC17	DISABLED		PTC17	CAN1_TX	UART3_TX	ENET0_158_8_TMR1	FB_CS4_b/ FB_TSIZ0/ FB_BE31_24_b	NFC_CE0_b		
M9	PTC18	DISABLED		PTC18		UART3_RTS_b	ENET0_158_8_TMR2	FB_TBST_b/ FB_CS2_b/ FB_BE15_8_b	NFC_CE1_b		
M8	PTC19	DISABLED		PTC19		UART3_CTS_b	ENET0_158_8_TMR3	FB_CS3_b/ FB_BE7_0_b	FB_TA_b		
L8	PTD0/ LLWU_P12	DISABLED		PTD0/ LLWU_P12	SPI0_PCS0	UART2_RTS_b	FTM3_CH0	FB_ALE/ FB_CS1_b/ FB_TS_b	I2S1_RXD1		
F8	PTD1	ADC0_SE5b	ADC0_SE5b	PTD1	SPI0_SCK	UART2_CTS_b	FTM3_CH1	FB_CS0_b	I2S1_RXD0		
K6	PTD2/ LLWU_P13	DISABLED		PTD2/ LLWU_P13	SPI0_SOUT	UART2_RX	FTM3_CH2	FB_AD4	I2S1_RX_FS		
J6	PTD3	DISABLED		PTD3	SPI0_SIN	UART2_TX	FTM3_CH3	FB_AD3	I2S1_RX_BC LK		
K5	PTD4/ LLWU_P14	DISABLED		PTD4/ LLWU_P14	SPI0_PCS1	UART0_RTS_b	FTM0_CH4	FB_AD2/ NFC_DATA1	EWM_IN		
J5	PTD5	ADC0_SE6b	ADC0_SE6b	PTD5	SPI0_PCS2	UART0_CTS_b/ UART0_COL_b	FTM0_CH5	FB_AD1/ NFC_DATA0	EWM_OUT_b		
K4	PTD6/ LLWU_P15	ADC0_SE7b	ADC0_SE7b	PTD6/ LLWU_P15	SPI0_PCS3	UART0_RX	FTM0_CH6	FB_AD0	FTM0_FLT0		
H6	PTF13	DISABLED		PTF13			UART2_RX				
G6	PTF14	DISABLED		PTF14			UART2_TX				
T4	VSS	VSS	VSS								
E7	PTD7	DISABLED		PTD7	CMT_IRO	UART0_TX	FTM0_CH7		FTM0_FLT1		
J4	PTD8	DISABLED		PTD8	I2C0_SCL	UART5_RX			FB_A16/ NFC_CLE		
F7	PTD9	DISABLED		PTD9	I2C0_SDA	UART5_TX			FB_A17/ NFC_ALE		
E6	PTD10	DISABLED		PTD10		UART5_RTS_b			FB_A18/ NFC_RE		

256 MAP BGA	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
G5	PTD11	DISABLED		PTD11	SPI2_PCS0	UART5_CTS_b	SDHC0_CLKIN		FB_A19		
F5	PTD12	DISABLED		PTD12	SPI2_SCK	FTM3_FLT0	SDHC0_D4		FB_A20		
F4	PTD13	DISABLED		PTD13	SPI2_SOUT		SDHC0_D5		FB_A21		
E5	PTD14	DISABLED		PTD14	SPI2_SIN		SDHC0_D6		FB_A22		
E4	PTD15	DISABLED		PTD15	SPI2_PCS1		SDHC0_D7		FB_A23		
F6	PTF15	DISABLED		PTF15			UART0_RTS_b				
E1	PTF16	DISABLED		PTF16	SPI2_PCS0	FTM0_CH3	UART0_CTS_b/ UART0_COL_b				
B1	DDR_VDD	DDR_VDD		DDR_VDD							
A1	DDR_VSS	DDR_VSS		DDR_VSS							
D3	DDR_DQS1	DISABLED		DDR_DQS1							
D1	DDR_DQ8	DISABLED		DDR_DQ8							
C1	DDR_DQ9	DISABLED		DDR_DQ9							
B5	DDR_VDD	DDR_VDD		DDR_VDD							
A5	DDR_VSS	DDR_VSS		DDR_VSS							
D5	DDR_VSS	DDR_VSS		DDR_VSS							
C2	DDR_DQ10	DISABLED		DDR_DQ10							
B2	DDR_DQ11	DISABLED		DDR_DQ11							
C3	DDR_DQ12	DISABLED		DDR_DQ12							
B8	DDR_VDD	DDR_VDD		DDR_VDD							
A12	DDR_VSS	DDR_VSS		DDR_VSS							
C4	DDR_DQ13	DISABLED		DDR_DQ13							
B3	DDR_DQ14	DISABLED		DDR_DQ14							
A2	DDR_DQ15	DISABLED		DDR_DQ15							
A3	DDR_DM1	DISABLED		DDR_DM1							
E8	DDR_VSS	DDR_VSS		DDR_VSS							
B12	DDR_VDD	DDR_VDD		DDR_VDD							
A16	DDR_VSS	DDR_VSS		DDR_VSS							
C6	DDR_VREF	DDR_VREF		DDR_VREF							
C5	DDR_DQ0	DISABLED		DDR_DQ0							
B4	DDR_DQ1	DISABLED		DDR_DQ1							
A4	DDR_DQ2	DISABLED		DDR_DQ2							
C16	DDR_VDD	DDR_VDD		DDR_VDD							
C7	DDR_VSS	DDR_VSS		DDR_VSS							
B6	DDR_DQ3	DISABLED		DDR_DQ3							
D6	DDR_DQ4	DISABLED		DDR_DQ4							
A6	DDR_DQ5	DISABLED		DDR_DQ5							
A7	DDR_ODT	DISABLED		DDR_ODT							

Pinout

256 MAP BGA	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
E11	DDR_VSS	DDR_VSS		DDR_VSS							
D2	DDR_VDD	DDR_VDD		DDR_VDD							
C9	DDR_VSS	DDR_VSS		DDR_VSS							
B7	DDR_DQ6	DISABLED		DDR_DQ6							
A8	DDR_DQ7	DISABLED		DDR_DQ7							
C8	DDR_DQS0	DISABLED		DDR_DQS0							
D9	DDR_DM0	DISABLED		DDR_DM0							
D4	DDR_VDD	DDR_VDD		DDR_VDD							
C14	DDR_VSS	DDR_VSS		DDR_VSS							
A9	DDR_BA0	DISABLED		DDR_BA0							
B10	DDR_BA1	DISABLED		DDR_BA1							
B9	DDR_BA2	DISABLED		DDR_BA2							
A10	DDR_CKB	DISABLED		DDR_CKB							
A11	DDR_CK	DISABLED		DDR_CK							
D7	DDR_VDD	DDR_VDD		DDR_VDD							
D8	DDR_VSS	DDR_VSS		DDR_VSS							
D10	DDR_A0	DISABLED		DDR_A0							
C11	DDR_A1	DISABLED		DDR_A1							
B11	DDR_A2	DISABLED		DDR_A2							
C12	DDR_A3	DISABLED		DDR_A3							
E10	DDR_VDD	DDR_VDD		DDR_VDD							
D12	DDR_VSS	DDR_VSS		DDR_VSS							
C10	DDR_A4	DISABLED		DDR_A4							
A13	DDR_A5	DISABLED		DDR_A5							
A14	DDR_A6	DISABLED		DDR_A6							
D11	DDR_A7	DISABLED		DDR_A7							
A15	DDR_A8	DISABLED		DDR_A8							
E12	DDR_VDD	DDR_VDD		DDR_VDD							
E3	DDR_VSS	DDR_VSS		DDR_VSS							
B16	DDR_CKE	DISABLED		DDR_CKE							
B15	DDR_A9	DISABLED		DDR_A9							
B13	DDR_A10	DISABLED		DDR_A10							
B14	DDR_A11	DISABLED		DDR_A11							
C15	DDR_A12	DISABLED		DDR_A12							
D16	DDR_A13	DISABLED		DDR_A13							
D15	DDR_A14	DISABLED		DDR_A14							
E16	DDR_RAS_ B	DISABLED		DDR_RAS_ B							
C13	DDR_CAS_ B	DISABLED		DDR_CAS_ B							
D14	DDR_CS_B	DISABLED		DDR_CS_B							

256 MAP BGA	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
D13	DDR_WE_B	DISABLED		DDR_WE_B							

8.2 K61 Pinouts

The below figure shows the pinout diagram for the devices supported by this document. Many signals may be multiplexed onto a single pin. To determine what signals can be used on which pin, see the previous section.

Revision History

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	DDR_VSS	DDR_DQ15	DDR_DM1	DDR_DQ2	DDR_VSS	DDR_DQ5	DDR_ODT	DDR_DQ7	DDR_BA0	DDR_CKB	DDR_CK	DDR_VSS	DDR_A5	DDR_A6	DDR_A8	DDR_VSS	A
B	DDR_VDD	DDR_DQ11	DDR_DQ14	DDR_DQ1	DDR_VDD	DDR_DQ3	DDR_DQ6	DDR_VDD	DDR_BA2	DDR_BA1	DDR_A2	DDR_VDD	DDR_A10	DDR_A11	DDR_A9	DDR_CKE	B
C	DDR_DQ9	DDR_DQ10	DDR_DQ12	DDR_DQ13	DDR_DQ0	DDR_VREF	DDR_VSS	DDR_DQS0	DDR_VSS	DDR_A4	DDR_A1	DDR_A3	DDR_CAS_B	DDR_VSS	DDR_A12	DDR_VDD	C
D	DDR_DQ8	DDR_VDD	DDR_DQS1	DDR_VDD	DDR_VSS	DDR_DQ4	DDR_VDD	DDR_VSS	DDR_DM0	DDR_A0	DDR_A7	DDR_VSS	DDR_WE_B	DDR_CS_B	DDR_A14	DDR_A13	D
E	PTF16	PTE0	DDR_VSS	PTD15	PTD14	PTD10	PTD7	DDR_VSS	PTC17	DDR_VDD	DDR_VSS	DDR_VDD	PTC3/ LLWU_P7	PTC4/ LLWU_P8	PTC5/ LLWU_P9	DDR_RAS_B	E
F	PTF17	PTE1/ LLWU_P0	PTE2/ LLWU_P1	PTD13	PTD12	PTF15	PTD9	PTD1	PTC16	PTC15	PTC9	PTC6/ LLWU_P10	PTC1/ LLWU_P6	PTC2	PTF7	PTF8	F
G	PTF18	PTE3	PTE4/ LLWU_P2	PTE5	PTD11	PTF14	VDD	VDD	VDD	VDD	PTC10	PTC7	PTB20	PTB21	PTB22	PTC0	G
H	PTF19	PTE6	PTE7	PTE8	PTF20	PTF13	VDDINT	VSS	VSS	VDDINT	PTC11/ LLWU_P11	PTC8	PTB17	PTB18	PTB19	PTB23	H
J	PTE9	PTE10	PTE16	PTD8	PTD5	PTD3	VDD	VSS	VSS	VDD	PTC14	PTC12	PTB10	PTB11	PTB16	PTF6	J
K	PTE11	PTE17	PTE12	PTD6/ LLWU_P15	PTD4/ LLWU_P14	PTD2/ LLWU_P13	PTE27	VSS	VSS	VDD	PTF11	PTF9	PTC13	PTB8	PTB9	PTF5	K
L	VOUT33	VSS	VREGIN	PTE18	TAMPER1	TAMPER2	PTE28	PTD0/ LLWU_P12	VSS	VDD	PTF12	PTF10	PTF1	PTB6	PTB7	PTF4	L
M	USB0_DP	USB0_DM	PTE19	VREFL	TAMPER0/ RTC WAKEUP_B	TAMPER7	PTE26	PTC19	PTC18	PTA12	PTB1	PTB0/ LLWU_P5	PTA26	PTB3	PTB5	PTF3	M
N	PGA2_DP/ ADC2_DP0/ ADC3_DP3/ ADC0_DP1	PGA2_DM/ ADC2_DM0/ ADC3_DM3/ ADC0_DM1	ADC0_SE16/ CMP1_IN2/ ADC0_SE21	VSSA	VDDA	TAMPER6	VSS	PTA1	PTF22	PTA13/ LLWU_P4	PTA16	PTA8	PTA24	PTA29	PTB4	PTF2	N
P	PGA3_DP/ ADC3_DP0/ ADC2_DP3/ ADC1_DP1	PGA3_DM/ ADC3_DM0/ ADC2_DM3/ ADC1_DM1	ADC1_SE16/ CMP2_IN2/ ADC0_SE22	VREFH	VBAT	TAMPER4	PTE24	PTA3	PTF21	PTF23	PTA15	PTA7	PTA10	PTA28	PTB2	PTF0	P
R	PGA0_DP/ ADC0_DP0/ ADC1_DP3	PGA0_DM/ ADC0_DM0/ ADC1_DM3	DAC0_OUT/ CMP1_IN3/ CMP2_IN2/ ADC0_SE23	DAC1_OUT/ CMP0_IN4/ CMP2_IN3/ ADC1_SE23	TAMPER3	TAMPER5	PTE25	PTA4/ LLWU_P3	PTF25	PTF24	PTA14	PTA6	PTA11	PTA25	PTA27	RESET_b	R
T	PGA1_DP/ ADC1_DP0/ ADC0_DP3	PGA1_DM/ ADC1_DM0/ ADC0_DM3	VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_SE18	VSS	EXTAL32	XTAL32	PTA0	PTA2	PTF26	PTF27	PTA17	PTA5	PTA9	VSS	PTA18	PTA19	T

Figure 38. K61 256 MAPBGA Pinout Diagram

9 Revision History

The following table provides a revision history for this document.

Table 53. Revision History

Rev. No.	Date	Substantial Changes
1	6/2011	Initial public revision. Corrected USB conditions.
2	11/2011	<ul style="list-style-type: none"> • Added AC electrical specifications. • Updated Part identification section for 120 MHz CPU frequency. • Updated Voltage and current operating ratings section. • Updated Voltage and current operating requirements section. • Updated LVD and POR operating requirements section. • Updated Voltage and current operating behaviors section. • Updated Power mode transition operating behaviors section. • Updated Power consumption operating behaviors section. • In Run mode supply current vs. core frequency section, added Run and VLPR modes supply current vs. core frequency diagrams. • In Device clock specifications section, updated flash clock frequency and DDR clock frequency. • Updated Thermal attributes. • In MCG specifications section, updated total deviation of trimmed average DCO output Frequency, PLL reference frequency range, and lock detector detection time. • In Oscillator frequency specifications section, updated crystal startup time — 32 kHz. • Updated NFC specifications section. • Updated DDR controller specifications section. • In DryIce Tamper Electrical Specifications section, updated supply current. • In DSPI switching specifications section, updated master and slave modes frequency of operation for limited voltage and full voltage ranges. • In I2S/SAI Switching Specifications section, updated cycle time for master and slave modes. • In USB DCD electrical specifications section, updated data detect voltage. • In TSI electrical specifications, updated reference oscillator frequency. • Updated Pinouts. • Updated Pinouts.

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