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PRODUCT OVERVIEW

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The KS57C2308/C2316 single-chip CMOS microcontroller has been designed for high performance using Samsung's newest 4-bit CPU core, SAM47 (Samsung Arrangeable Microcontrollers).

With features such as LCD direct drive capability, 8-bit timer/counter, and serial I/O, the KS57C2308/C2316 offer an excellent design solution for a wide variety of applications that require LCD functions.

Up to 40 pins of the 80-pin QFP package can be dedicated to I/O. Six vectored interrupts provide fast response to internal and external events. In addition, the KS57C2308/C2316's advanced CMOS technology provides for low power consumption and a wide operating voltage range.

OTP

The KS57C2308/C2316 microcontroller is also available in OTP (One Time Programmable) version, KS57P2308/P2316. KS57P2308/P2316 microcontroller has an on-chip 8/16-Kbyte one-time-programmable EPROM instead of masked ROM. The KS57P2308/P2316 is comparable to KS57C2308/C2316, both in function and in pin configuration.

FEATURES

Memory

- 512 × 4-bit RAM
- 8 K × 8-bit ROM (KS57C2308/P2308)
- 16 K × 8-bit ROM (KS57C2316/P2316)

I/O Pins

- Input only: 8 pins
- I/O: 24 pins
- Output: 8 pins sharing with segment driver outputs

LCD Controller/Driver

- Maximum 16-digit LCD direct drive capability
- 32 segment, 4 common pins
- Display modes: Static, 1/2 duty (1/2 bias), 1/3 duty (1/2 or 1/3 bias), 1/4 duty (1/3 bias)

8-Bit Basic Timer

- Programmable interval timer
- Watchdog timer

8-Bit Timer/Counter 0

- Programmable 8-bit timer
- External event counter
- Arbitrary clock frequency output
- Serial I/O interface clock generator

Watch Timer

- Real-time and interval time measurement
- Four frequency outputs to BUZ pin
- Clock source generation for LCD

8-Bit Serial I/O Interface

- 8-bit transmit/receive mode
- 8-bit receive only mode
- LSB-first or MSB-first transmission selectable
- Internal or external clock source

Bit Sequential Carrier

- Support 16-bit serial data transfer in arbitrary format

Interrupts

- Three internal vectored interrupts
- Three external vectored interrupts
- Two quasi-interrupts

Memory-Mapped I/O Structure

- Data memory bank 15

Two Power-Down Modes

- Idle mode (only CPU clock stops)
- Stop mode (main or sub system oscillation stops)

Oscillation Sources

- Crystal, ceramic, or RC for main system clock
- Crystal or external oscillator for subsystem clock
- Main system clock frequency: 4.19 MHz (typical)
- Subsystem clock frequency: 32.768 kHz
- CPU clock divider circuit (by 4, 8, or 64)

Instruction Execution Times

- 0.95, 1.91, 15.3 μ s at 4.19 MHz (main)
- 122 μ s at 32.768 kHz (subsystem)

Operating Temperature

- –40 °C to 85 °C

Operating Voltage Range

- 1.8 V to 5.5 V

Package Type

- 80-pin QFP

BLOCK DIAGRAM

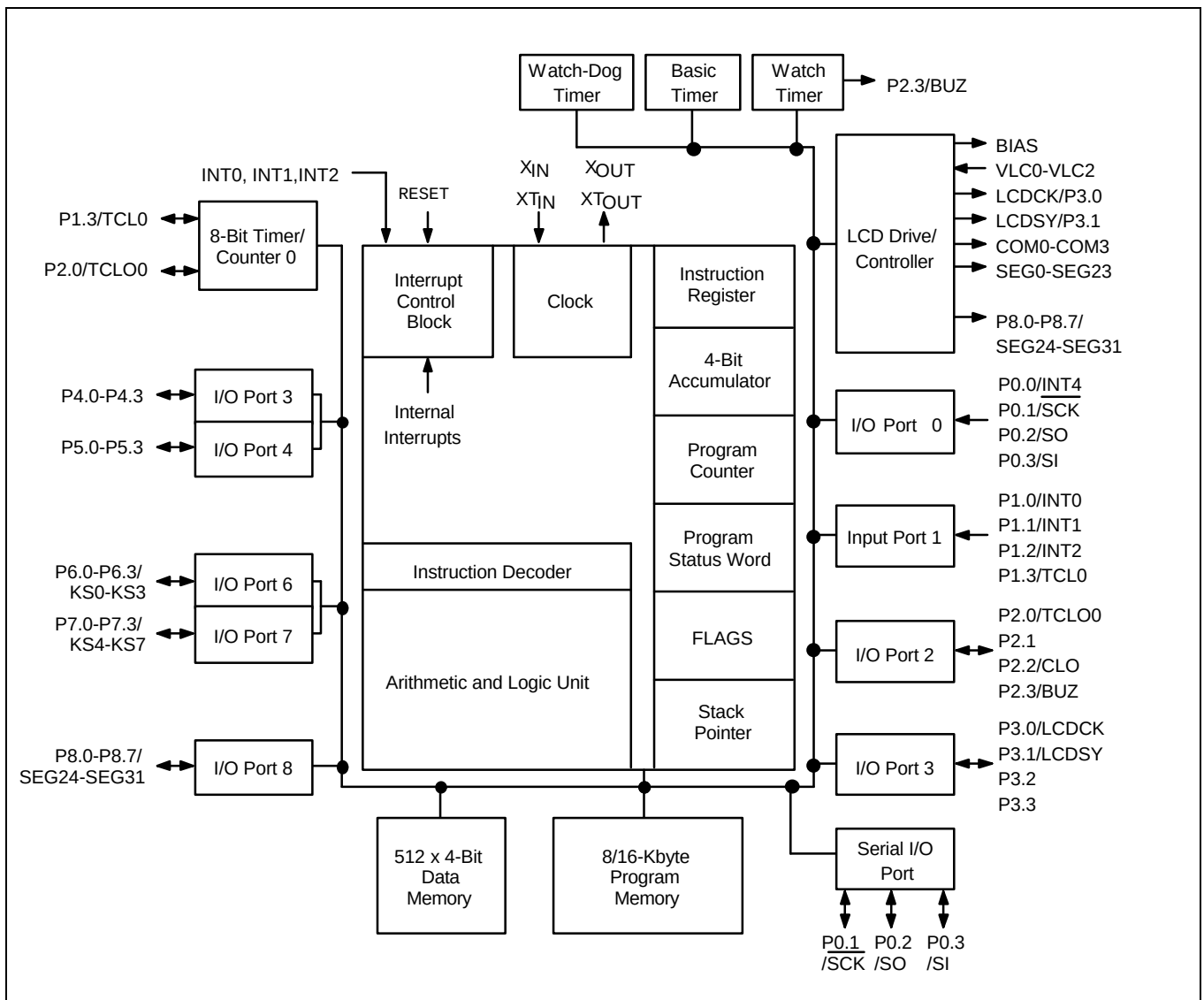


Figure 1-1. KS57C2308/C2316 Simplified Block Diagram

PIN ASSIGNMENTS

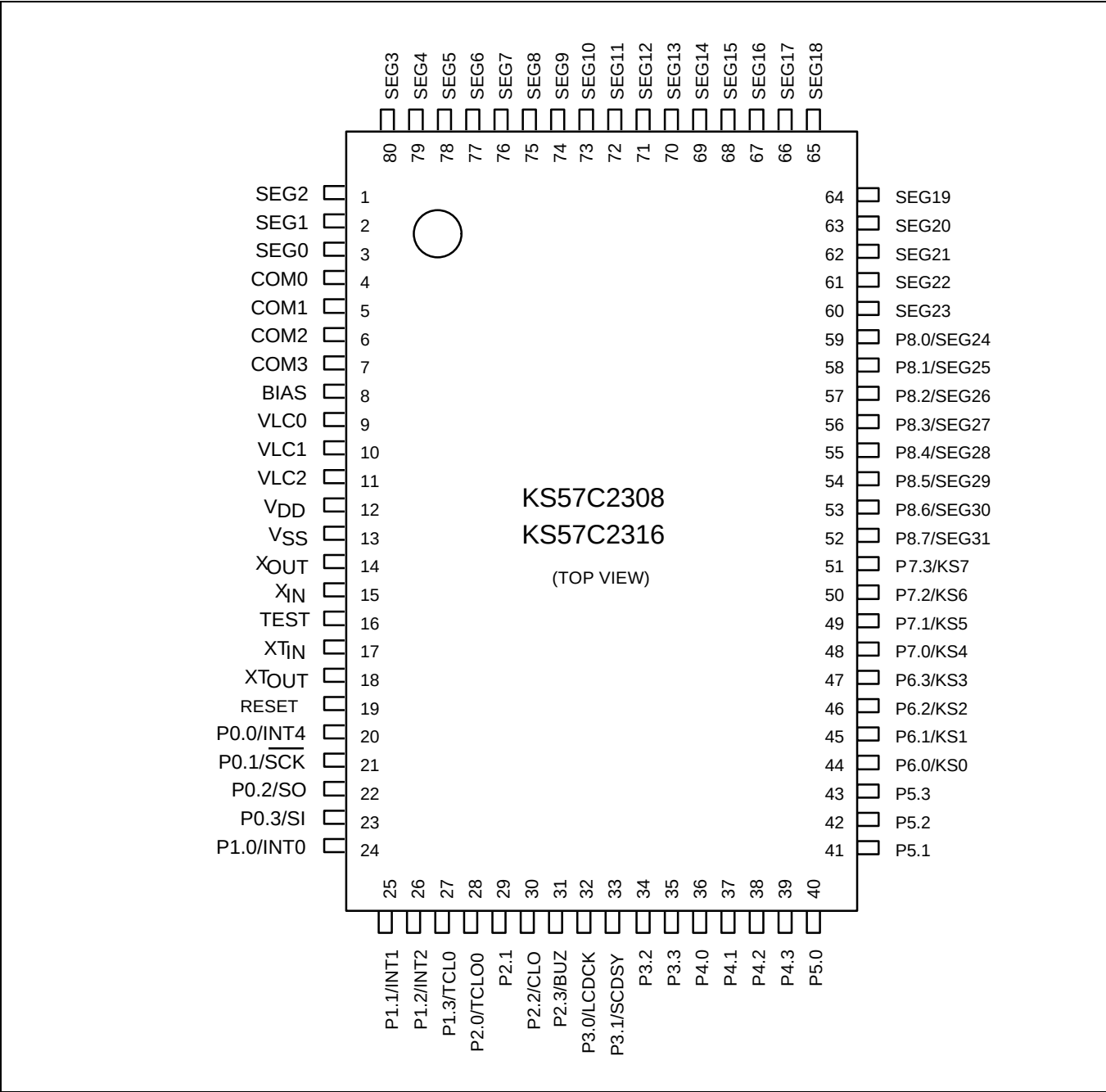


Figure 1-2. KS57C2308/C2316 80-QFP Pin Assignment Diagram

PIN DESCRIPTIONS

Table 1-1. KS57C2308/C2316 Pin Descriptions

Pin Name	Pin Type	Description	Number	Share Pin	Reset Value	Circuit Type
P0.0	I	4-bit input port.	20	INT4	Input	A-1
P0.1	I/O	1-bit and 4-bit read and test are possible.	21	SCK		D *
P0.2	I/O	4-bit pull-up resistors are software assignable.	22	SO		D *
P0.3	I		23	SI		A-1
P1.0	I	4-bit input port.	24	INT0	Input	A-1
P1.1		1-bit and 4-bit read and test are possible.	25	INT1		
P1.2		4-bit pull-up resistors are software assignable.	26	INT2		
P1.3			27	TCL0		
P2.0	I/O	4-bit I/O port.	28	TCL00	Input	D
P2.1		1-bit and 4-bit read/write and test are possible.	29	–		
P2.2		4-bit pull-up resistors are software assignable.	30	CLO		
P2.3			31	BUZ		
P3.0	I/O	4-bit I/O port.	32	LCDCK	Input	D
P3.1		1-bit and 4-bit read/write and test are possible.	33	LCDSY		
P3.2		Each individual pin can be specified as input or output. 4-bit pull-up resistors are software assignable.	34			
P3.3			35			
P4.0–P4.3 P5.0–P5.3	I/O	4-bit I/O ports. N-channel open-drain output up to 5 V. 1-, 4-, and 8-bit read/write and test are possible. Ports 4 and 5 can be paired to support 8-bit data transfer. 4-bit pull-up resistors are software assignable.	36–43	–	Input	E
P6.0–P6.3 P7.0–P7.3	I/O	4-bit I/O ports. Port 6 pins are individually software configurable as input or output. 1-bit and 4-bit read/write and test are possible. 4-bit pull-up resistors are software assignable. Ports 6 and 7 can be paired to enable 8-bit data transfer.	44–51	KS0–KS3 KS4–KS7	Input	D *
P8.0–P8.7	O	Output port for 1-bit data (for use as CMOS driver only)	59–52	SEG24–SEG31	Output	H-16
SEG0–SEG23	O	LCD segment signal output	3–1, 80–60	–	Output	H-15
SEG24–SEG31	O	LCD segment signal output	59–52	P8.0–P8.7	Output	H-16
COM0–COM3	O	LCD common signal output	4–7	–	Output	H-15
V _{LC0} –V _{LC2}	–	LCD power supply. Voltage dividing resistors are assignable by mask option	9–11	SCLK SDAT	–	–
BIAS	–	LCD power control	8	–	–	–
LCDCK	I/O	LCD clock output for display expansion	32	P3.0	Input	D

Table 1-1. KS57C2308/C2316 Pin Descriptions (Continued)

Pin Name	Pin Type	Description	Number	Share Pin	Reset Value	Circuit Type
LCDSY	I/O	LCD synchronization clock output for LCD display expansion	33	P3.1	Input	D
TCL0	I/O	External clock input for timer/counter 0	27	P1.3	Input	A-1
TCLO0	I/O	Timer/counter 0 clock output	28	P2.0	Input	D
SI	I	Serial interface data input	23	P0.3	Input	A-1
SO	I/O	Serial interface data output	22	P0.2	Input	D *
SCK	I/O	Serial I/O interface clock signal	21	P0.1	Input	D *
INT0 INT1	I	External interrupts. The triggering edge for INT0 and INT1 is selectable. Only INT0 is synchronized with the system clock.	24 25	P1.0 P1.1	Input	A-1
INT2	I	Quasi-interrupt with detection of rising edge signals.	26	P1.2	Input	A-1
INT4	I	External interrupt input with detection of rising or falling edge	20	P0.0	Input	A-1
KS0-KS7	I/O	Quasi-interrupt inputs with falling edge detection.	44-51	P6.0-P7.3	Input	D *
CLO	I/O	CPU clock output	30	P2.2	Input	D
BUZ	I/O	2, 4, 8 or 16 kHz frequency output for buzzer sound with 4.19 MHz main system clock or 32.768 kHz subsystem clock.	31	P2.3	Input	D
X _{IN} , X _{OUT}	—	Crystal, ceramic or RC oscillator pins for main system clock. (For external clock input, use X _{IN} and input X _{IN} 's reverse phase to X _{OUT})	15,14	—	—	—
XT _{IN} , XT _{OUT}	—	Crystal oscillator pins for subsystem clock. (For external clock input, use XT _{IN} and input XT _{IN} 's reverse phase to XT _{OUT})	17,18	—	—	—
V _{DD}	—	Main power supply	12	—	—	—
V _{SS}	—	Ground	13	—	—	—
RESET	—	Reset signal	19	—	Input	B
TEST	—	Test signal input (must be connected to V _{SS})	16	—	—	—

NOTES:

1. Pull-up resistors for all I/O ports are automatically disabled if they are configured to output mode.
2. D * Type has a schmitt trigger circuit at input.