

AN-6075

Compact Green-Mode Adapter Using FSQ500L for Low Cost

1. Introduction

This application note describes a detailed design strategy for a compact flyback converter. Design considerations and mathematical equations are presented, as well as guidelines for a printed circuit board layout. The FSQ500L is designed for a replacement of linear power supplies to achieve low cost. This device combines current-mode Pulse Width Modulator (PWM) with a single-chip 700V senseFET. The integrated PWM controller features include: fixed operating frequency (130KHz), under-voltage lockout (UVLO) protection, soft-start time tuned by external capacitor, overload protection (OLP), leading-edge blanking (LEB), optimized gate turn-on/turn-off driver, thermal shutdown (TSD) protection with hysteresis, and temperature-compensated precision-current sources for loop compensation. The no-load power consumption can be less than 250mW without auxiliary bias winding and down to 60mW with auxiliary bias winding for universal AC input voltage range to meet the power conservation requirements.

When compared to a linear power supply, the FSQ500L reduces total size and weight, while increasing efficiency, productivity, and system reliability. This device provides a platform for cost-effective flyback converters.

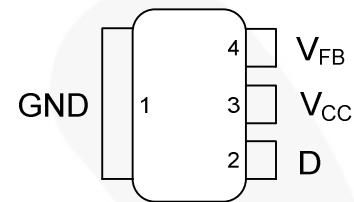


Figure 1. SOT-223 Pin Configuration

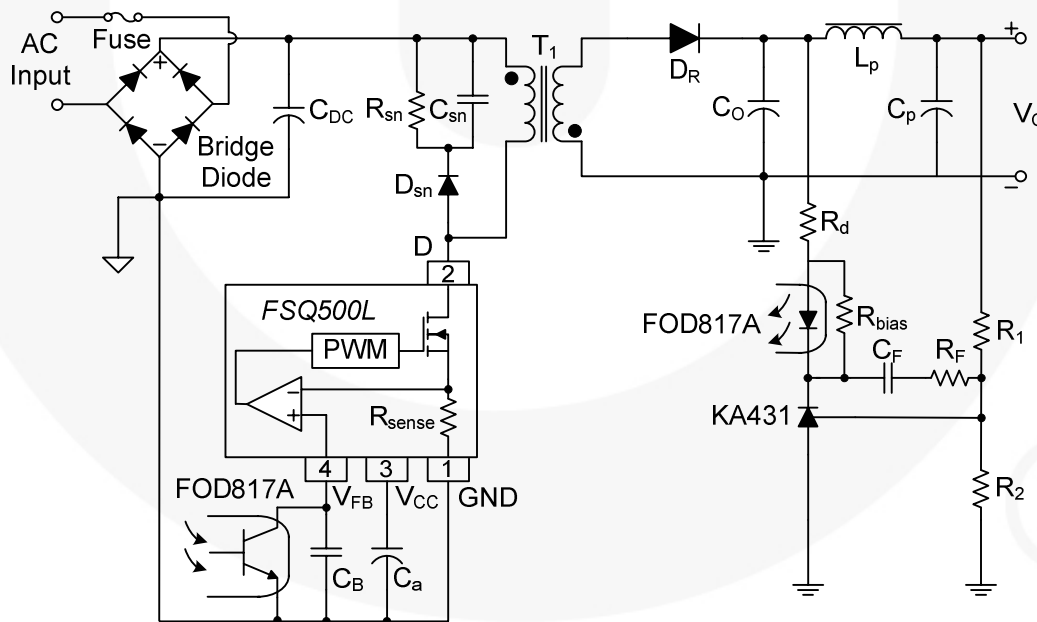


Figure 2. Typical Application

2. Device Block Description

2.1 Startup Circuit and Soft Start

At startup, an internal high-voltage current source supplies the internal bias and charges the external capacitor (C_a) connected to the V_{CC} pin, as illustrated in Figure 4. An internal high-voltage regulator (HV/REG) located between the D and VCC pins regulates the V_{CC} to be 6.5V and supplies operating current. FSQ500L needs no auxiliary bias winding.

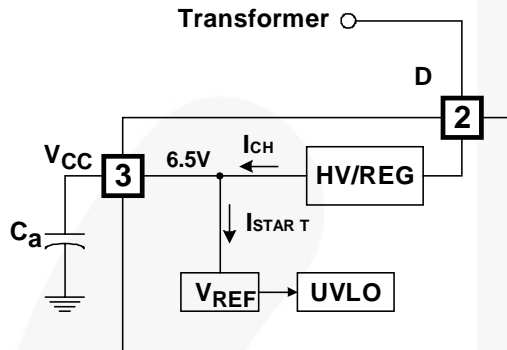


Figure 3. Startup Block

The soft-start time of FSQ500L is tuned by an external V_{CC} capacitor (C_a), which increases PWM comparator non-inverting input voltage, together with the senseFET current, slowly after it starts up. Before V_{CC} reaches V_{START} , C_a is charged by the current $I_{CH}-I_{START}$, where I_{CH} and I_{START} are described in Figure 3. After V_{CC} reaches V_{START} , all internal blocks are activated, so that the current consumed inside the IC becomes I_{OP} . Therefore, C_a is charged by the current $I_{CH}-I_{OP}$, which makes the increasing slope of V_{CC} become sluggish. Make the soft-start time long or short by selecting C_a as described in Figure 4. During $t_{S/S}$, I_{DELAY} is disabled to avoid unwanted OLP. Typically, $t_{S/S}$ is around 8ms with 47 μ F of C_a .

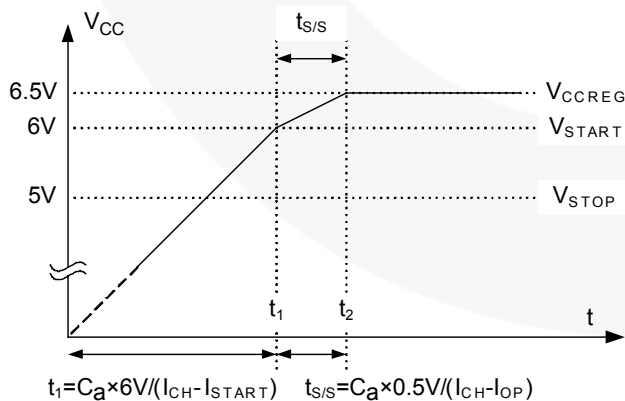


Figure 4. Soft-Start Function

The peak value of the drain current of the power switching device is progressively increased to establish the correct working conditions for transformers, inductors, and capacitors. The voltage on the output capacitors is

progressively increased with the intention of smoothly establishing the required output voltage. It also helps to prevent transformer saturation and reduce the stress on the secondary diode during startup.

2.2 Feedback Control

FSQ500L employs current-mode control, as shown in Figure 5. An opto-coupler (such as the FOD817A) and shunt regulator (such as the KA431) are typically used to implement the feedback network. Comparing the feedback voltage with the voltage across the R_{sense} resistor makes it possible to control the switching duty cycle. When the reference pin voltage of the shunt regulator exceeds the internal reference voltage of 2.5V, the opto-coupler LED current increases, pulling down the feedback voltage and reducing the duty cycle. This typically occurs when the line input voltage increases or the output load current decreases.

2.3 Pulse-by-Pulse Current Limit

Because current-mode control is employed, the peak current through the senseFET is limited by the non-inverting input of PWM comparator (V_{fb}^*), as shown in Figure 5. Assuming that 225 μ A current source flows only through the internal resistor ($8R + R = 12\text{ k}\Omega$), the cathode voltage of diode D2 is about 2.7V. Since D1 is blocked when the feedback voltage (V_{fb}) exceeds 2.7V, the maximum voltage of the cathode of D2 is clamped at this voltage, clamping V_{fb}^* . Therefore, the peak value of the current through the senseFET is limited.

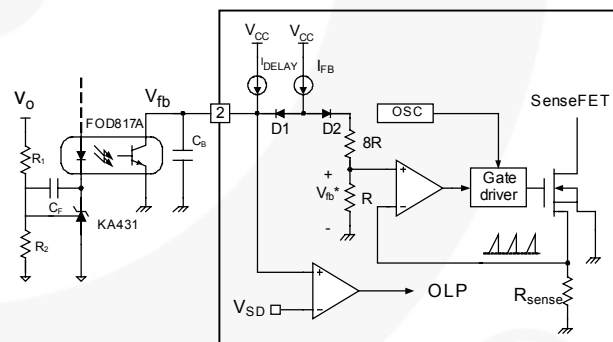


Figure 5. Pulse-Width Modulation (PWM) Circuit

2.4 Leading-Edge Blanking (LEB)

At the instant the internal senseFET is turned on, a high-current spike occurs through the senseFET, caused by primary-side capacitance and secondary-side rectifier reverse recovery. Excessive voltage across the R_{sense} resistor would lead to incorrect feedback operation in the current mode PWM control. To counter this effect, the FSQ500L employs a leading-edge blanking (LEB) circuit. This circuit inhibits the PWM comparator for a short time ($t_{LEB}=250\text{ns}$) after the senseFET turns on.

2.5 Protection Functions

The FSQ500L has two self-protective functions: overload protection (OLP) and thermal shutdown (TSD). While OLP is implemented as auto-restart mode, there is no switching when TSD triggers. Once the overload condition is detected, switching is terminated, the senseFET remains off, and HV/REG turns off. This causes V_{CC} to fall. When V_{CC} falls down to the under-voltage lockout (UVLO) stop voltage of 5.0V, the protection is reset and the startup circuit charges V_{CC} capacitor. When V_{CC} reaches the start voltage of 6.0V, the FSQ500L resumes normal operation. If the fault condition is still not removed, the senseFET and HV/REG remain off and V_{CC} drops to V_{STOP} again. In this manner, the auto-restart can alternately enable and disable the switching of the power senseFET until the fault condition, is eliminated, as shown in Figure 6.

Because these protection circuits are fully integrated into the IC without external components, the reliability can be improved without increasing cost.

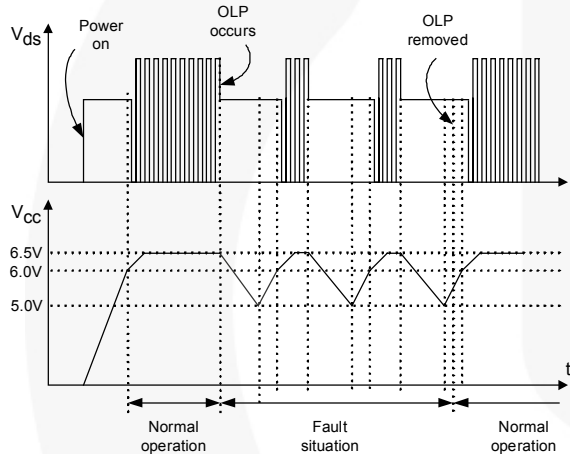


Figure 6. Auto-Restart Protection Waveforms

2.5.1 Overload Protection (OLP)

Overload is defined as the load current exceeding normal level due to an unexpected abnormal event. In this situation, the protection circuit should trigger to protect the SMPS. However, even when the SMPS is in normal operation, the over load protection circuit can be triggered during the load transition. To avoid this undesired operation, the overload protection circuit is designed to trigger after a specified time to determine whether it is a transient situation or an overload situation. Because of the pulse-by-pulse current limit capability, the maximum peak current through the senseFET is limited and, therefore, the maximum input power is restricted with a given input voltage. If the output consumes more than this maximum power, the output voltage (V_O) decreases below the set voltage. This reduces the current through the opto-coupler LED, which also reduces the opto-coupler transistor current, increasing the feedback voltage (V_{fb}). If V_{fb} exceeds 2.7V, D1 is blocked and the 5 μ A current source starts to charge C_B slowly up to

V_{CC} . In this condition, V_{fb} continues increasing until it reaches 4.5V, when the switching operation is terminated, as shown in Figure 7.

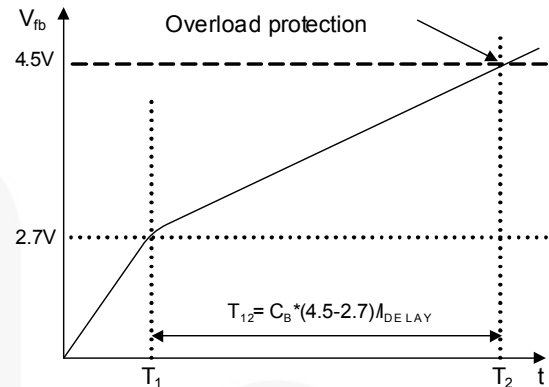


Figure 7. Overload Protection

The OLP delay time is:

$$t_{12} = \frac{C_B \cdot (4.5 - 2.7)}{I_{\text{Delay}}} \quad (1)$$

Under 50ms delay time (the C_B value should be smaller than 138nF) is applied for most applications. This protection is implemented in auto restart mode.

2.5.2 Thermal Shutdown (TSD)

The senseFET and the control IC are built in one package. This makes it easy for the control IC to detect the abnormal over-temperature of the senseFET. When the temperature exceeds approximately 140°C, thermal shutdown triggers.

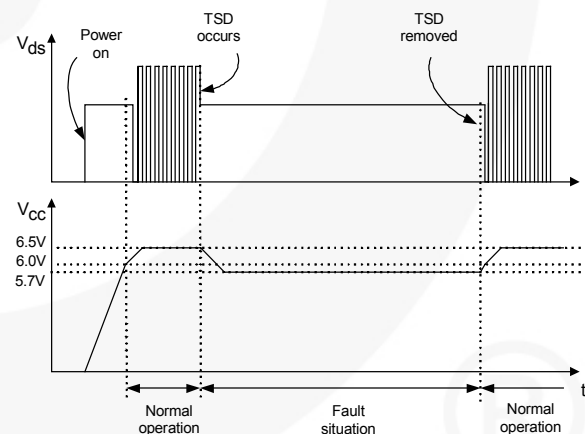


Figure 8. Over-Temperature Protection

When TSD triggers, delay current is disabled, switching operation stops, and V_{CC} through the internal high-voltage current source is set to 5.7V from 6.5V, as shown in Figure 8. Since the TSD signal prohibits the senseFET from switching, there is no switching until the junction temperature decreases sufficiently. If the junction temperature is lower than 60°C typically, the TSD signal is removed and V_{CC} is set to 6.5V again. While V_{CC} increases

from 5.7V to 6.5V, the soft-start function turns the senseFET on and off with no voltage and/or current stress.

2.6 Burst Operation

To minimize power dissipation in standby mode, the FSQ500L enters burst-mode operation. As the load decreases, the feedback voltage decreases. As shown in Figure 10, the device automatically enters burst mode when the feedback voltage drops below V_{BURL} (750mV). At this point, switching stops and the output voltages start to drop at a rate dependent on standby current load. This causes the feedback voltage to rise. Once it passes V_{BURH} (800mV), switching resumes. The feedback voltage then falls and the process repeats. Burst-mode operation alternately enables and disables switching of the power senseFET, thereby reducing switching loss in standby mode.

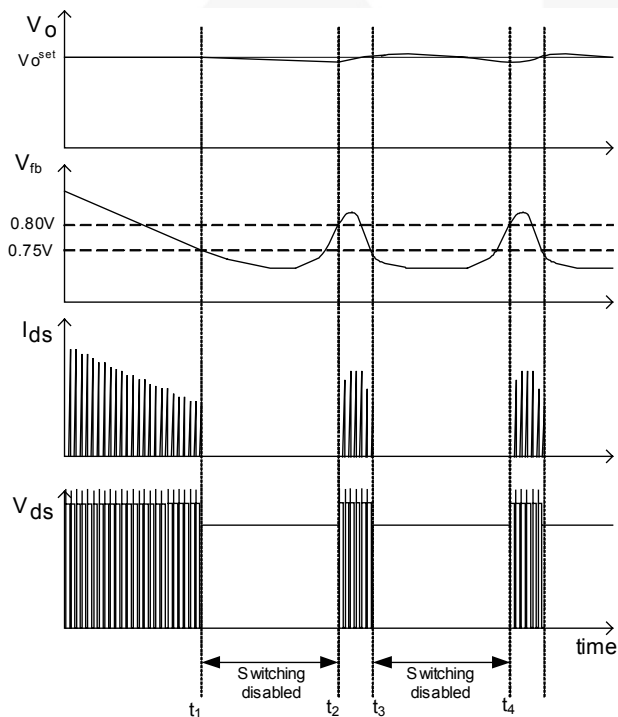


Figure 9. Burst-Mode Operation

3. Design Example

The following is design example for 2W compact adapter.

3.1 Determine System Specifications

Output Power, $P_O=2.04W$ ($5.1V/0.4A$); V_{AC} input range=85 to 264V_{AC} (universal input), line frequency, $f_L=60Hz$; Efficiency, $\eta>50\%$.

3.2 Determine DC Link Capacitor (C_{DC}) and DC Link Voltage Range

It is typical to select the DC link capacitor as 2-3 μF per watt of input power for universal input range (85-264V_{AC}) and 1 μF per watt of input power for European input range (195-264V_{AC}). Figure 10 shows the corrected input voltage waveform. The red line shows ripple voltage on the DC link capacitor and the minimum and maximum voltage on the DC link capacitor are expressed in Equations 2 and 3.

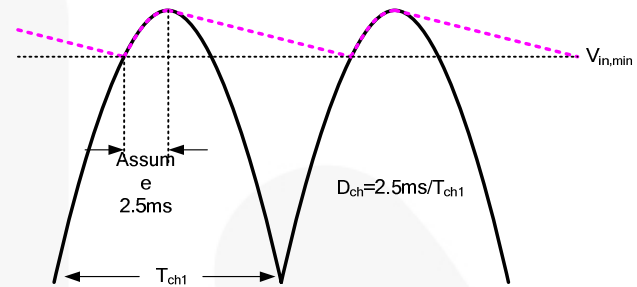


Figure 10. Bridge Rectifier and Bulk Capacitor Voltage Waveform

$$V_{DC,min} = \sqrt{2V_{ac,min}^2 - \frac{2V_O \times I_O \times (1 - D_{ch})}{\eta \times C_{DC} \times 2f_L}} \quad (2)$$

$$= \sqrt{2 \times 85V_{ac}^2 - \frac{2 \times 5.1V \times 0.4A \times (1 - 0.3)}{0.5 \times 5.7 \mu F \times 120Hz}}$$

$$= 87V$$

$$V_{DC,max} = \sqrt{2}V_{ac,max} = \sqrt{2} \times 264V = 373V \quad (3)$$

where D_{ch} is DC link capacitor charging duty ratio defined as shown in Figure 10, which is typically about 0.3.

Output power is 2.04W, so the V_{DC} capacitor is 6.08 μF . Select the nearest standard value 5.7 μF (4.7 μF +1 μF) for C_{DC} and substitute it above. Therefore; from Equation 2 and 3, the $V_{DC,min}$ is 87V and $V_{DC,max}$ is 373V.

3.3 Determine the Turn Ratio

The transformer turn ratio ($n=N_{pri}/N_{sec}$) is an important parameter of the flyback converter; it affects the maximum duty ratio when the input voltage is at a minimum value. It also influences the voltage stresses on the MOSFET and the secondary rectifier. The permissible voltage stresses and the maximum voltage stresses on the MOSFET, as well as the secondary rectifier, can be expressed as:

$$V_{DS,max} = V_{DC,max} + n(V_O + V_F)$$

$$= 373V + 11.5 \times (5.1V + 0.7V) \quad (4)$$

$$= 440V$$

$$V_{DR,max} = \frac{V_{DC,max}}{n} + V_O = \frac{373V}{11.5} + 5.1V = 37.5V \quad (5)$$

where V_F is the forward-voltage of output diode.

It is typical to set $V_{DS,max}$ as 420V~560V (60%~80% of MOSFET rated voltage). Select the transformer turn ratio, n , to be 11.5. According to Equation 4, $V_{DS,max}=440V$, which satisfies 60%~80% of MOSFET rated voltage. The maximum voltage stress on the secondary rectifier can be calculated from Equation 5. Select SB260 rectifier diode from Equation 5 results. (Specification of SB260 as: the maximum reverse voltage, V_{RRM} is 60V and average forward current, I_F is 2A).

3.4 Determine Transformer Primary-Side Inductance (L_P), Maximum Duty (D_{max}), and Primary RMS Current (I_{RMS})

The primary-side inductance (L_P) of the transformer is designed specifically for DCM operation and obtained as:

$$L_P = \frac{2 \times P_O}{I_{PK}^2 \times \eta \times f_S} = \frac{2 \times 5.1V \times 0.4A}{(0.28A)^2 \times 0.5 \times 130KHz} \cong 800\mu H \quad (6)$$

where I_{PK} is primary-side peak current, given in the datasheet as I_{LIM} .

The maximum duty ratio (D_{max}) can be derived as:

$$D_{max} = \frac{L_P \times f_S \times I_{PK}}{V_{DC,min}} = \frac{800\mu H \times 130KHz \times 0.28A}{87V} = 33\% \quad (7)$$

The maximum duty ratio should be kept below 50% for DCM operation.

The primary-side RMS current can be derived as:

$$I_{RMS} = I_{PK} \times \sqrt{\frac{D_{max}}{3}} = 0.28 \times \sqrt{\frac{0.33}{3}} = 0.09A \quad (8)$$

3.5 Determine Transformer Core Size (A_e) and Minimum Primary-Side Turns ($N_{P,min}$)

Table 1 shows the commonly used cores with output power under 10W. The cores recommended are typical for the universal input range and 130kHz switch frequency. Choose the EE16 core to meet this output power from Table 1.

Table 1. Core Quick Select Table
(for universal input, $f_S=130KHz$ and 5V output)

Core	Cross-Sectional Area (A_e)	Window Area (A_w)	Output Power Range
EE13-Z	17.1mm ²	33.4mm ²	1-5W
EI16-Z	19.8mm ²	42.3mm ²	1-5W
EE16-Z	19.2mm ²	39.8mm ²	1-10W
EI19-Z	24.0mm ²	54.4mm ²	1-10W

Base on Faraday's law and the peak inductor current, the minimum turns for the primary inductance is calculated as:

$$N_{P,min} = \frac{L_P \times I_{PK}}{B_{max} \times A_e} \times 10^6 \quad (9)$$

$$= \frac{800\mu H \times 0.28A}{0.24T \times 19.2mm^2} \times 10^6 = 48 \text{ Turns}$$

where B_{max} is the saturation magnetic flux density, typical set 0.2~0.3Tesla; A_e is the cross-sectional of the core.

3.6 Determine Secondary-Side Turns ($N_{P,min}$)

The number of turns for the secondary winding is defined as:

$$N_S = \frac{N_P}{n} = \frac{104}{11.5} \cong 9 \text{ Turns} \quad (10)$$

Select primary-side turns, N_P to be 104 turns, so the secondary-side turns is 9 turns, based on Equation 10.

3.7 Determine Primary-Side RCD Snubber

When the MOSFET turns off, a high-voltage spike occurs on the drain pin because of a resonance between the leakage inductor (L_{lk}) of the main transformer and the output capacitor (C_{oss}) of the MOSFET. The excessive voltage on the drain pin may lead to an avalanche breakdown and eventually damage the MOSFET. Therefore, it is necessary to add an additional circuit to clamp the voltage.

The RCD snubber circuit and MOSFET drain voltage waveforms are shown in Figure 11 and Figure 12, respectively. The RCD snubber circuit absorbs the current in the leakage inductor by turning on the snubber diode (D_{sn}) when V_{DS} exceeds $V_{in}+nV_O$. It is assumed that the snubber capacitance is large enough that its voltage does not change during one switching period. The R_{sn2} can reduce the spike damping wave and affect EMI.

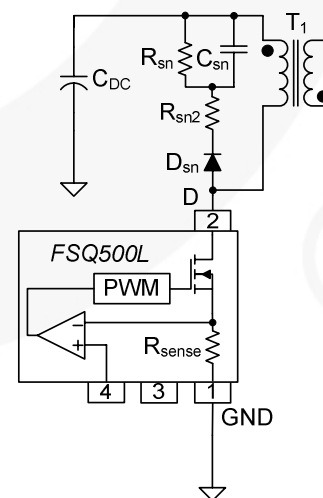


Figure 11. Primary-Side RCD Snubber Circuit

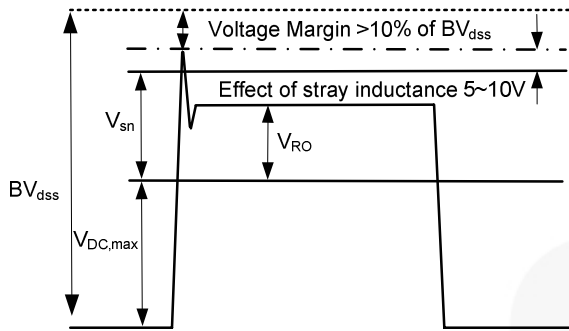


Figure 12. MOSFET Drain Voltage Waveform

The snubber capacitor voltage (V_{sn}) should be determined at the minimum input voltage and full-load condition. Once V_{sn} is determined, the power dissipated in the snubber circuit at the minimum input voltage and full-load condition is obtained by:

$$\text{Loss}_{sn} = \frac{V_{sn}^2}{R_{sn}} = \frac{1}{2} L_{lk} \times I_{pk}^2 \times f_s \times \frac{V_{sn}}{V_{sn} - nV_O} \quad (11)$$

where f_s is the switching frequency of FSQ500L.

V_{sn} should be 2~2.5 times of nV_O . Very small V_{sn} results in a severe loss in the snubber circuit, as shown Equation 11.

The resistance is obtained by:

$$\begin{aligned} R_{sn} &= \frac{V_{sn}^2}{\frac{1}{2} L_{lk} \times I_{pk}^2 \times f_s \times \frac{V_{sn}}{V_{sn} - nV_O}} \\ &= \frac{130^2}{0.5 \times 90 \mu\text{H} \times 0.28\text{A}^2 \times 130\text{kHz} \times \frac{130}{130 - 11.55 \times 5.1}} \\ &= 20\text{k}\Omega \end{aligned} \quad (12)$$

The power loss from R_{sn} can be calculated as:

$$P_{sn} = \frac{V_{sn}^2}{R_{sn}} = \frac{130}{20\text{k}\Omega} \cong 0.845\text{W} \quad (13)$$

To reduce the power loss from R_{sn} , the R_{sn} should be selected higher than $20\text{k}\Omega$. From Equation 12 if the R_{sn} increases, the V_{sn} also increases, the R_{sn} recommended value is between $200\text{k}\Omega$ and $47\text{k}\Omega$.

The maximum ripple of the snubber capacitor voltage is obtained as:

$$\begin{aligned} C_{sn} &= \frac{V_{sn}}{\Delta V_{sn} \times R_{sn} \times f_s} \\ &= \frac{130}{5\% \times 130 \times 200\text{k}\Omega \times 130\text{kHz}} \cong 0.7\text{nF}, \text{ selected } 1\text{nF} \end{aligned} \quad (14)$$

where f_s is the switching frequency and R_{sn} uses $200\text{k}\Omega$. In general, 5~10% ripple is reasonable.

3.8 External V_{CC} Auxiliary Winding Circuit for Improving Power Saving

Figure 13 shows an external V_{CC} auxiliary winding circuit for improving power saving. The external V_{CC} auxiliary winding circuit reduces internal circuit power loss to improve power saving.

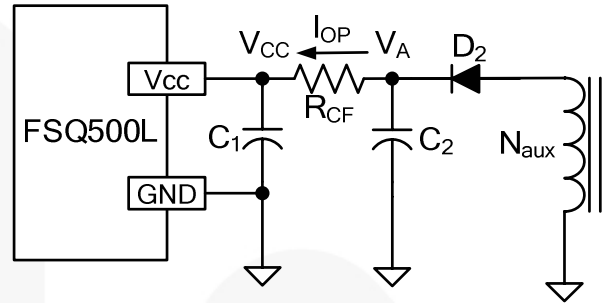


Figure 13. External V_{CC} Auxiliary Winding Circuit for Improving Power Saving

The number of turns for the V_{CC} auxiliary winding is defined as:

$$N_{aux} = \frac{V_A + V_{D2F}}{V_O + V_F} \times N_S = \frac{7.7 + 0.7}{5.1 + 0.7} \times 9 \cong 13 \text{ Turns} \quad (15)$$

where V_A is the voltage of V_{CC} auxiliary winding and V_{D2F} is forward-voltage of D_2 diode.

Because the FSQ500L has an internal high-voltage regulator (HV/REG) located between the D and VCC pins that regulates the V_{CC} to be 6.5V and supplies operating current. If using the auxiliary winding, the V_{CC} should be set higher than 6.5V. Assume V_A is 7.7V and V_{CC} is 6.8V, according to Equation 15, $N_{aux} = 13$ turns is solved. The R_{CF} is limited operation current; it can be obtained as:

$$R_F \leq \frac{V_A - V_{CC}}{I_{OP}} = \frac{7.7 - 6.8}{760 \mu\text{A}} = 1.18\text{k}\Omega, \text{ using } 1\text{k}\Omega \quad (16)$$

where I_{OP} is operation current, in the datasheet as I_{OP} .

In this circuit, a smaller capacitor C_1 (~1 μF) can be used to reduce startup time. The energy supporting the FSQ500L after startup is mainly from a larger capacitor C_2 (~22 μF). In this design example, if using the V_{CC} auxiliary winding, the no-load power saving is down to 60mW.

Note:

1. If using the external V_{CC} auxiliary circuit, the V_{SD} voltage of FB pin follows as V_{CC} voltage.

4. Printed Circuit Board Layout

High-frequency switching current / voltage makes printed circuit board layout a very important design issue. Good PCB layout minimizes excessive EMI helps the power supply survive during surge/ESD tests.

4.1 Guidelines

To improve EMI performance and reduce line frequency ripples, the output of the bridge rectifier should be connected to capacitor C_{DC} first, then to the switching circuits. Refer to Figure 14.

- The high-frequency current loop is in C_{DC} – Transformer – Drain PIN – GND PIN – C_{DC} . The area enclosed by this current loop should be as small as possible. Keep the traces (especially 2→1) short, direct, and wide. High-voltage traces related the drain of MOSFET and RCD snubber should be kept far way from control circuits to prevent unnecessary interference. If a heatsink is used for MOSFET, connect this heatsink to ground.
- As indicated by 2, the ground of control circuits should be connected first, then to other circuitry.
- Place C_a close to the controller for good decoupling.

Two suggestions with different pro and cons for ground connections are recommended.

- **GND2→1**: This could avoid common impedance interference for the sense signal.
- Regarding the ESD discharge path, the charges go from secondary, through the transformer stray capacitance, to **GND1** first, and back to mains. It should be noted that control circuits should not be placed on the discharge path. Point discharge for common choke can decrease high-frequency impedance and increase ESD immunity.
- **3** should be a point-discharger route to bypass the static electricity energy. As shown in Figure 12, it is suggested to map out this discharge route.
- Should a Y-cap be required between primary and secondary, connect this Y-cap to the positive terminal of C_{DC} . If this Y-cap is connected to primary GND, it should be connected to the negative terminal of C_{DC} (**GND1**) directly. Point discharge of this Y-cap helps for ESD; however, the creepage between these two pointed ends should be at least 5mm according to safety requirements.

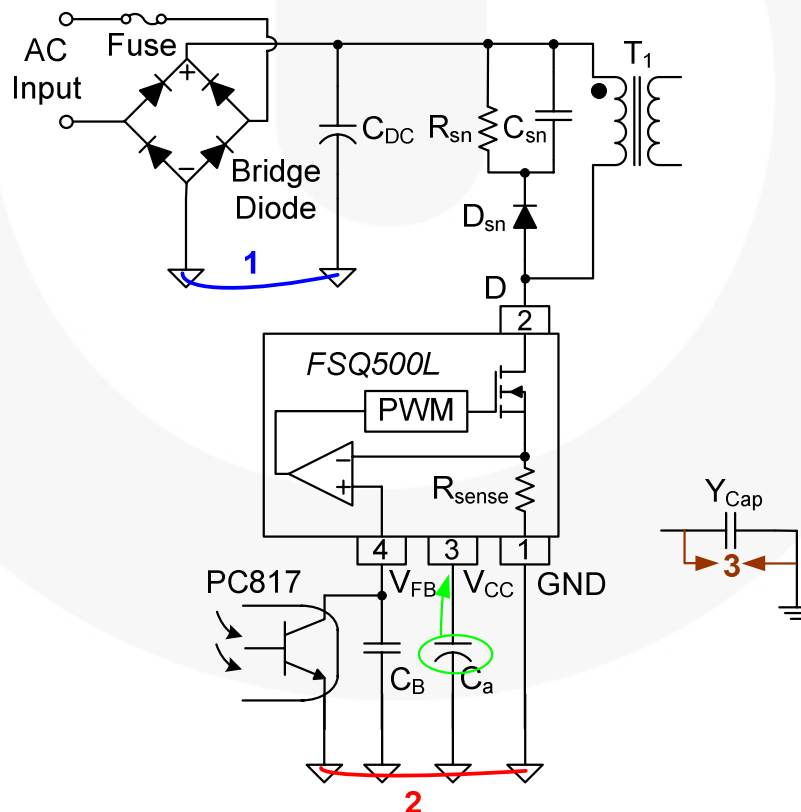


Figure 14. Layout Considerations

5. Typical Application Circuit

Application	Output Power	Input Voltage Range	Output Voltage/Maximum Current
Adapter	2.04W	Universal Input (85-264V _{AC})	5.1V/0.4A

5.1 Features

- Single Chip 700V SenseFET Power Switch
- Soft-Start Time Tuned by External Capacitor
- Built-in Overload Protection (OLP) and Internal Thermal Shutdown Function (TSD) with Hysteresis
- Low Standby Mode Power Consumption (Input Wattage <0.3W at No-Load Condition)

5.2 Key Design Notes

- Resistors R₁ and inductance L₁ improve EMI.
- External V_{CC} auxiliary circuit is from with D₆, C₉, C₁₀, and R₉. The external V_{CC} auxiliary winding circuit reduces internal circuit power loss and improves power saving.

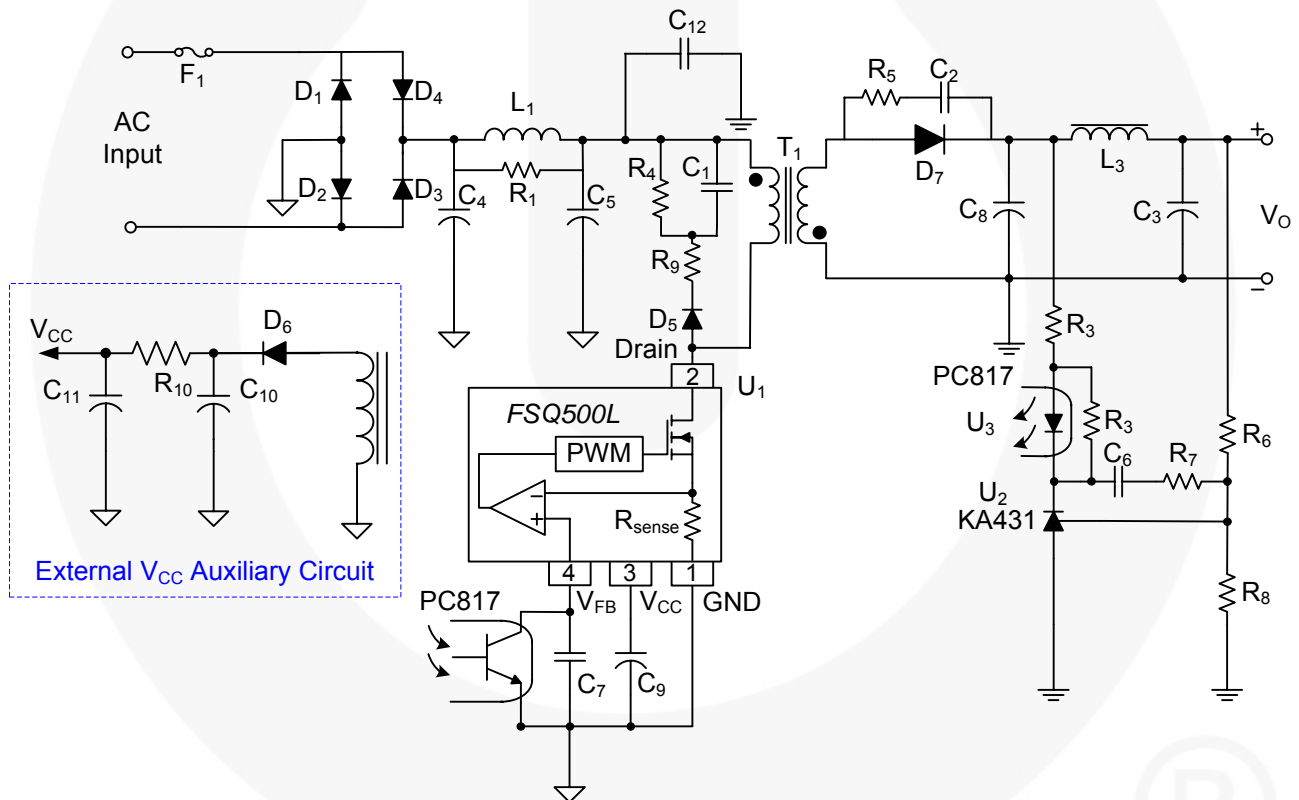


Figure 15. Schematic

Table 2. 2W Compact Green-Mode Adapter Evaluation Board Part List

PART#	VALUE	NOTE	PART#	VALUE	NOTE
Fuse			Capacitor		
F1	18Ω	1W	C1	1nF/1kV	Ceramic
Resistor			C2	NC	
R1	4.7kΩ	SMD 0805+/-5%	C3	220μF/10V	Electrolytic
R2	1kΩ	SMD 0805+/-5%	C4	1μF/400V	Electrolytic
R3	30Ω	SMD 0805+/-5%	C5	4.7μF/400V	Electrolytic
R4	200kΩ	SMD 1206+/-5%	C6	330nF	SMD 1206
R5	NC		C7	22nF	SMD 1206
R6	2.2kΩ	SMD 0805 +/-5%	C8	330μF/10V	Electrolytic
R7	300Ω	SMD 0805 +/-5%	C9	47μF/16V	Electrolytic
R8	2KΩ	SMD 0805 +/-5%	C10	22μF/50V	Electrolytic
R9	30Ω	SMD 0805 +/-5%	C11	1μF	SMD 1206
R10	1kΩ	1/4W	C12	2.2nF/250V	Y2, Ceramic
IC			D1, D2, D3, D4, D5,	IN4007	1000V/1A
U1	FSQ500L	Fairchild	D6	1N4148	
U2	PC817	Fairchild	D7	SB260	60V/2A
U3	TL431	Fairchild	Filter		
			L1	470μH	Resistance
			L3	3μH	

5.3 Transformer Specification

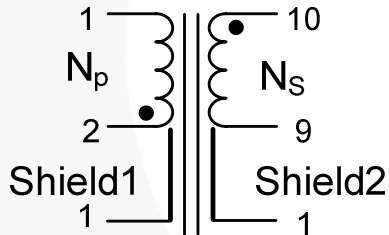


Figure 16. Transformer Schematic

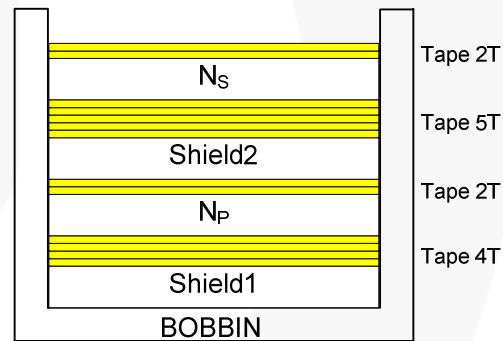


Figure 17. Winding Sequence

5.3.1 Winding Specification

No	Pin(s-f)	Wire	Turns	Winding Method
Shield1	1-	0.15Φ	46Ts	Solenoid Winding
Insulation: Polyester Tape t = 0.03mm, 4 Layers				
N _p	2-1	0.2Φ	104Ts	Solenoid Winding
Insulation: Polyester Tape t = 0.03mm, 2 Layers				
Shield2	1-	0.15Φ	46Ts	Solenoid Winding
Insulation: Polyester Tape t = 0.03mm, 5 Layers				
N _s	10-9	TEX-E 0.4Φ	9Ts	Solenoid Winding
Insulation: Polyester Tape t = 0.03mm, 2 Layers				

5.3.2 Electrical Specification

	Pin	Value	Remarks
Inductance	6-4	800 μ H \pm 5%	1KHz, 0.25V
Leakage	6-4	90 μ H	2nd Shorted

- Core and Bobbin: EE16
- Ae: 19.2 [mm²]

5.4 Experimental Results

Table 3. No-Load Input Wattage, Efficiency, Out Current Protection, Experimental Result

Input Voltage	Input Wattage (No Load without V _{CC} Auxiliary Winding)	Input Wattage (No Load with V _{CC} Auxiliary Winding)	Efficiency (without V _{CC} Auxiliary Winding)	Efficiency (with V _{CC} Auxiliary Winding)	Output Current Protection
85V/60Hz	0.094W	0.04W	65.93%	69.55%	0.611A
120V/60Hz	0.116W	0.043W	66.34%	71.08%	0.65A
230V/50Hz	0.209W	0.053W	56.62%	63.00%	0.836A
264V/50Hz	0.242W	0.06W	53.14%	59.59%	0.881A

Table 4. Experimental Waveform

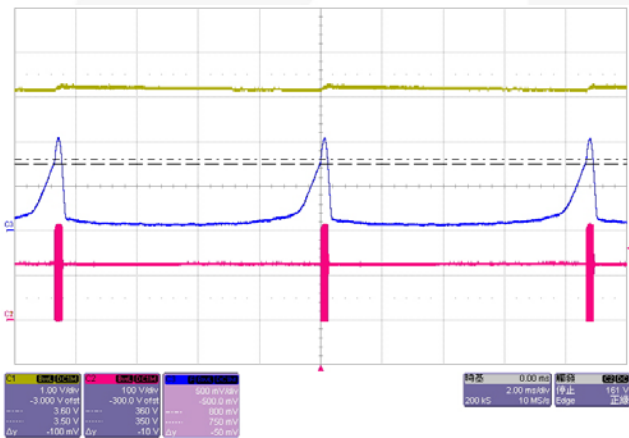


Figure 18. Burst-Mode Operation at Input Voltage 85V_{AC} (CH1:V_O, CH2: V_{DS}, CH3: V_{FB})

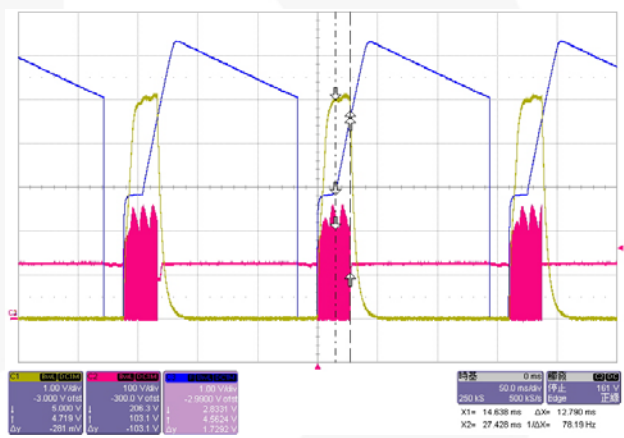


Figure 19. Over-Current Protection Waveform at Input Voltage 85V_{AC}; Delay time is ~ 12.7ms (CH1:V_O, CH2: V_{DS}, CH3: V_{FB})

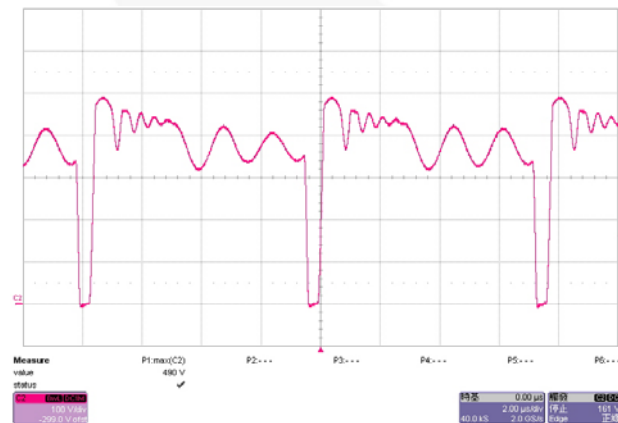


Figure 20. Voltage Stress of MOSFET at Input Voltage 264V_{AC}; Maximum Voltage is ~490V (CH2: V_{DS})

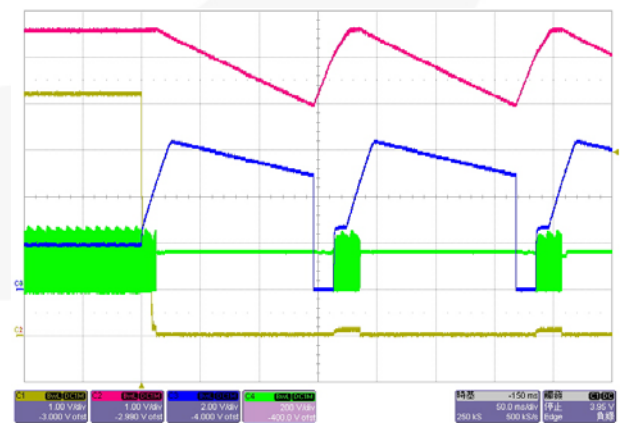


Figure 21. Short-Circuit Protection at Input Voltage 120V_{AC} (CH1:V_O, CH2: V_{CC}, CH3: V_{FB}, CH4:V_{DS})

6. Reference

[FSQ500L — Compact Green-Mode Fairchild Power Switch \(FPS™\)](#)

[AN-4137 — Design Guidelines for Off-line Flyback Converters Using the FPS™](#)

[AN-4147 — Design Guideline for RCD Snubber of Flyback Converters](#)

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