

HITJ0201MP

Silicon P Channel MOS FET
Power Switching

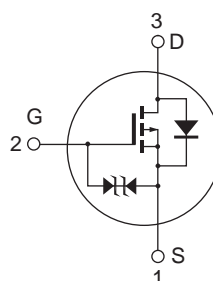
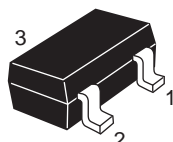
R07DS0473EJ0100
Rev.1.00
Jun 22, 2011

Features

- Low on-resistance
 $R_{DS(on)} = 53 \text{ m}\Omega$ typ ($V_{GS} = -4.5 \text{ V}$, $I_D = -1.8 \text{ A}$)
- Low drive current
- High speed switching
- 2.5 V gate drive

Outline

RENESAS Package code: PLSP0003ZB-A
(Package name: MPAK)



1. Source
2. Gate
3. Drain

Note: Marking is "UG".

Absolute Maximum Ratings

($T_a = 25^\circ\text{C}$)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	-20	V
Gate to source voltage	V_{GSS}	+8 / -12	V
Drain current	I_D	-3.4	A
Drain peak current	$I_{D(pulse)}$ ^{Note1}	-10	A
Body - drain diode reverse drain current	I_{DR}	-3.4	A
Channel dissipation	$P_{ch(pulse)}$ ^{Note2}	0.8	W
Channel temperature	T_{ch}	150	$^\circ\text{C}$
Storage temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

Notes: 1. $PW \leq 10 \mu\text{s}$, duty cycle $\leq 1\%$

2. When using the glass epoxy board (FR-4: 40 x 40 x 1 mm)

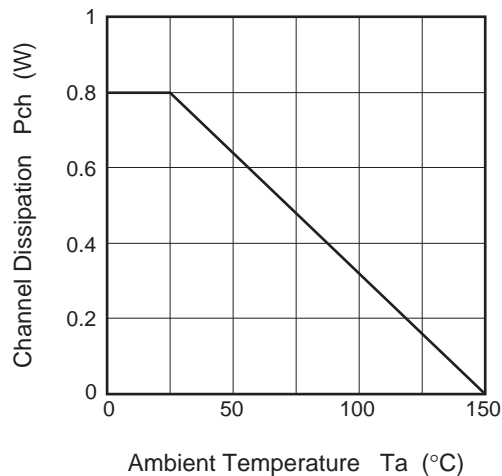
Electrical Characteristics

(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	-20	—	—	V	$I_D = -10 \text{ mA}$, $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	+8	—	—	V	$I_G = +100 \text{ } \mu\text{A}$, $V_{DS} = 0$
	$V_{(BR)GSS}$	-12	—	—	V	$I_G = -100 \text{ } \mu\text{A}$, $V_{DS} = 0$
Gate to source leak current	I_{GSS}	—	—	+10	μA	$V_{GS} = +6 \text{ V}$, $V_{DS} = 0$
	I_{GSS}	—	—	-10	μA	$V_{GS} = -10 \text{ V}$, $V_{DS} = 0$
Drain to source leak current	I_{DSS}	—	—	-1	μA	$V_{DS} = -20 \text{ V}$, $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	-0.4	—	-1.4	V	$V_{DS} = -10 \text{ V}$, $I_D = -1 \text{ mA}$
Drain to source on state resistance	$R_{DS(on)}$	—	53	69	$\text{m}\Omega$	$I_D = -1.8 \text{ A}$, $V_{GS} = -4.5 \text{ V}$ ^{Note3}
	$R_{DS(on)}$	—	80	112	$\text{m}\Omega$	$I_D = -1.8 \text{ A}$, $V_{GS} = -2.5 \text{ V}$ ^{Note3}
Forward transfer admittance	$ y_{fs} $	4.5	6.5	—	S	$I_D = -1.8 \text{ A}$, $V_{DS} = -10 \text{ V}$ ^{Note3}
Input capacitance	C_{iss}	—	597	—	pF	$V_{DS} = -10 \text{ V}$ $V_{GS} = 0$ $f = 1 \text{ MHz}$
Output capacitance	C_{oss}	—	149	—	pF	
Reverse transfer capacitance	C_{rss}	—	93	—	pF	
Turn - on delay time	$t_{d(on)}$	—	18	—	ns	$I_D = -1.8 \text{ A}$ $V_{GS} = -4.5 \text{ V}$ $R_L = 5.5 \text{ } \Omega$ $R_g = 4.7 \text{ } \Omega$
Rise time	t_r	—	43	—	ns	
Turn - off delay time	$t_{d(off)}$	—	37	—	ns	
Fall time	t_f	—	12	—	ns	
Total gate charge	Q_g	—	6.3	—	nC	$V_{DD} = -10 \text{ V}$ $V_{GS} = -4.5 \text{ V}$ $I_D = -3.4 \text{ A}$
Gate to source charge	Q_{gs}	—	1.1	—	nC	
Gate to drain charge	Q_{gd}	—	2.5	—	nC	
Body - drain diode forward voltage	V_{DF}	—	-0.85	-1.1	V	$I_F = -3.4 \text{ A}$, $V_{GS} = 0$ ^{Note3}

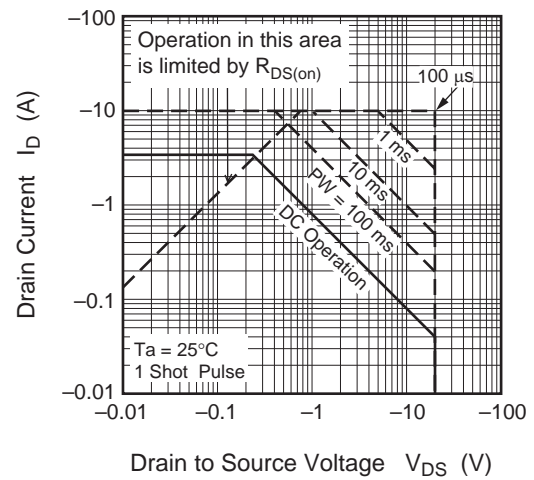
Notes: 3. Pulse test

Main Characteristics

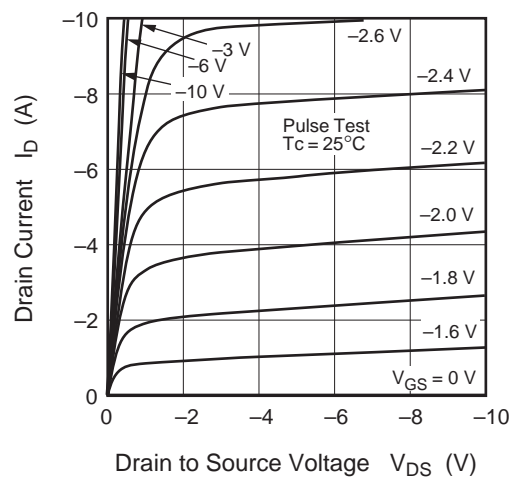
Maximum Channel Power
Dissipation Curve

*When using the glass epoxy board (FR-4: 40 × 40 × 1 mm)

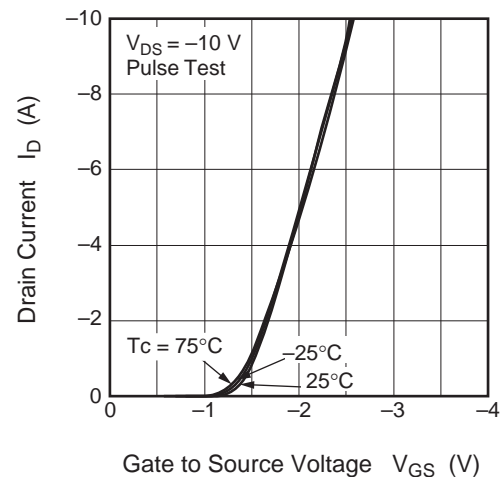
Maximum Safe Operation Area



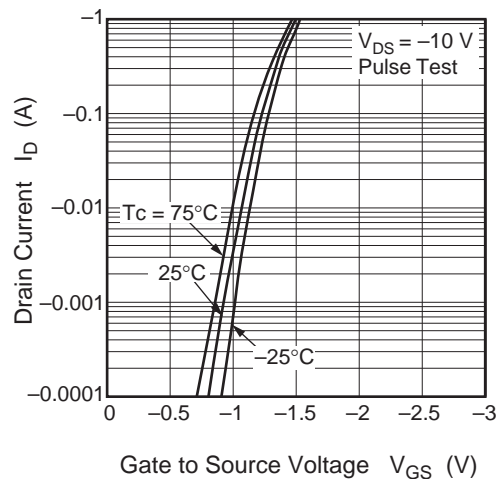
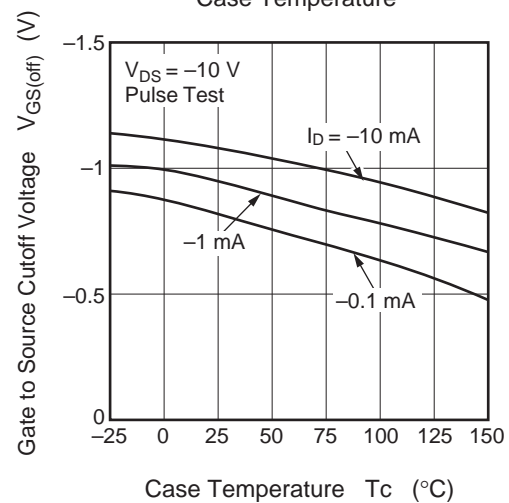
Typical Output Characteristics

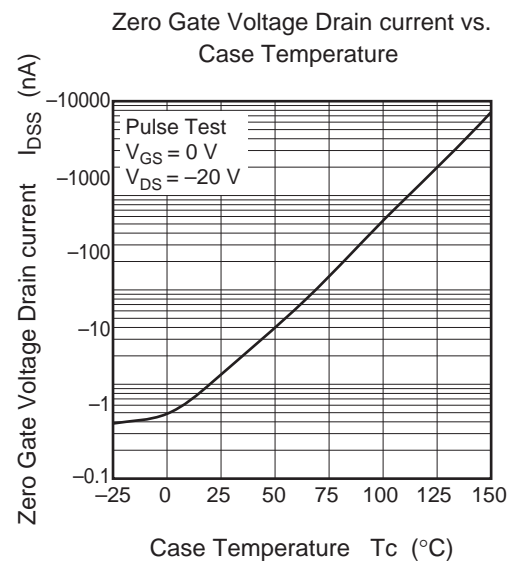
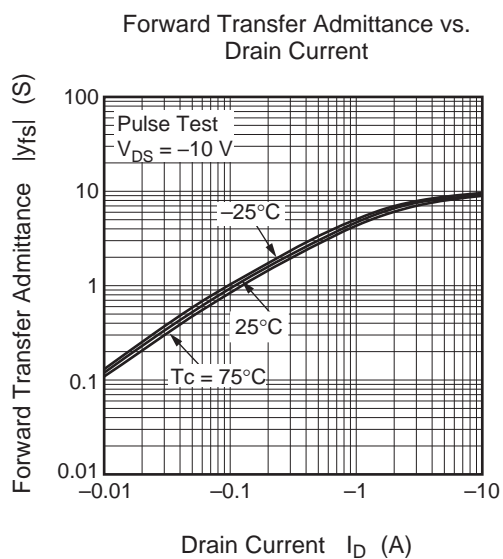
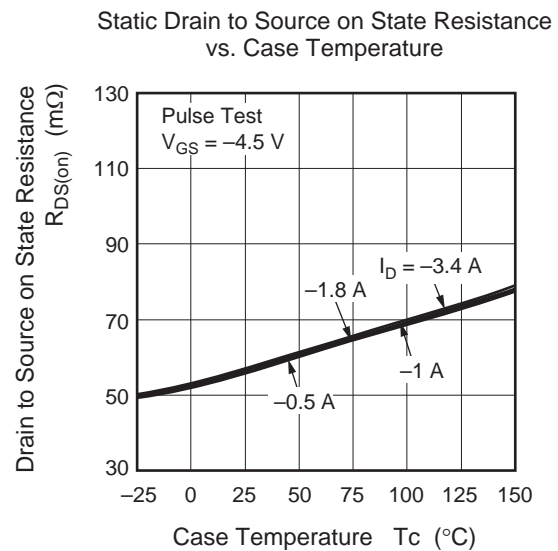
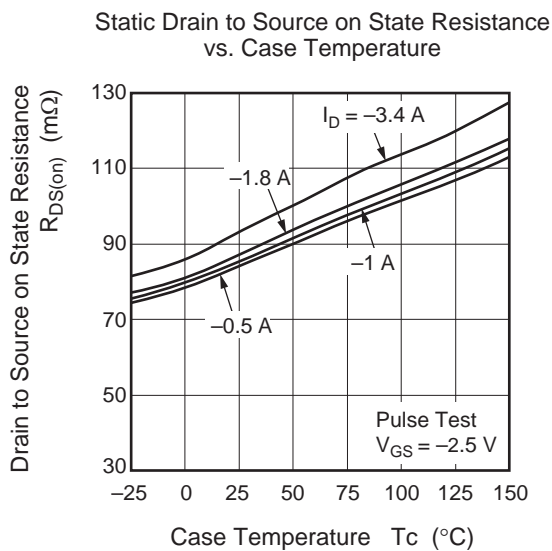
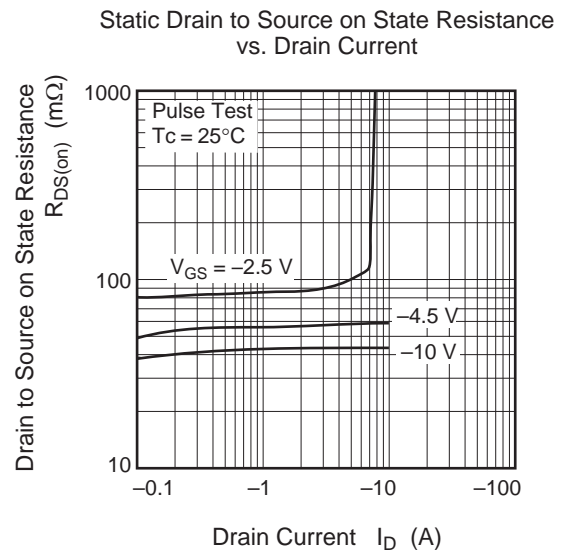
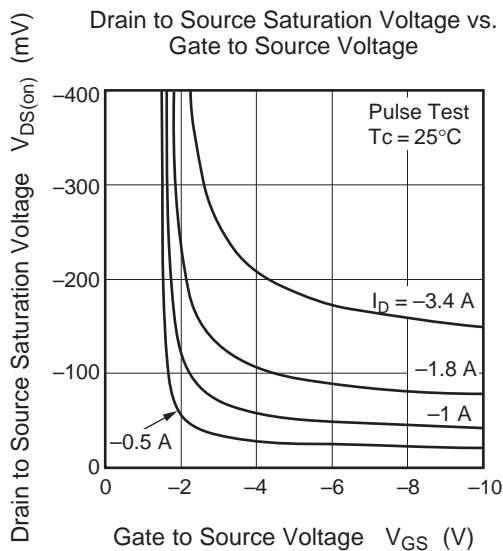


Typical Transfer Characteristics (1)

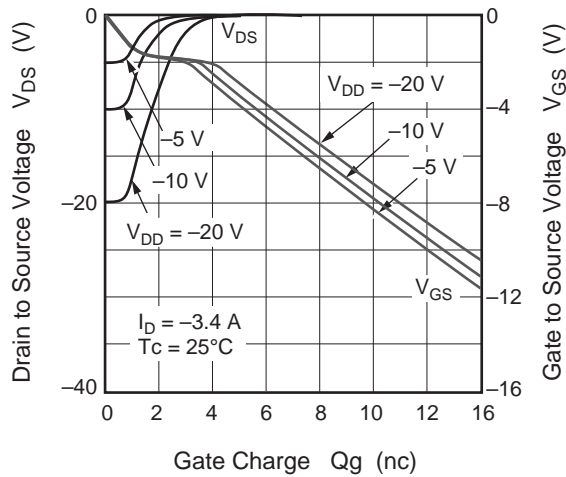


Typical Transfer Characteristics (2)

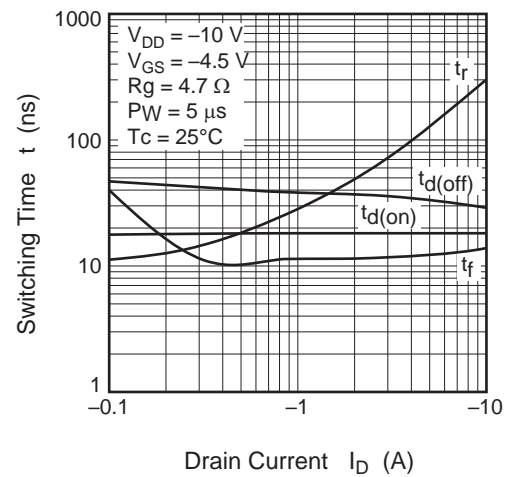
Gate to Source Cutoff Voltage vs.
Case Temperature



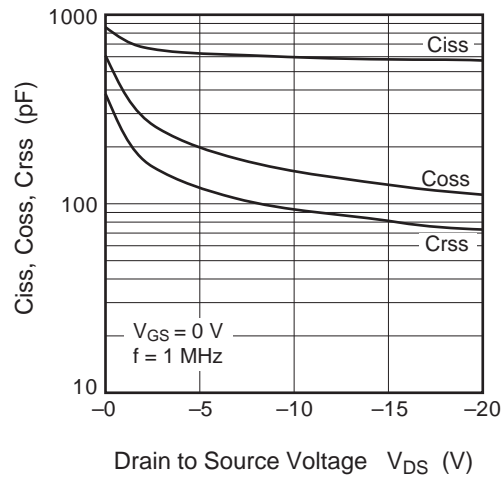
Dynamic Input Characteristics



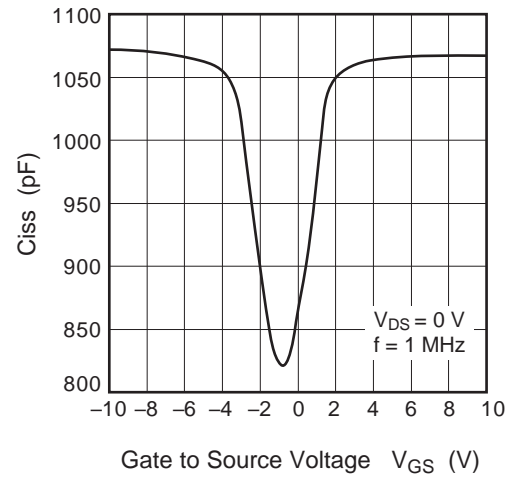
Switching Characteristics



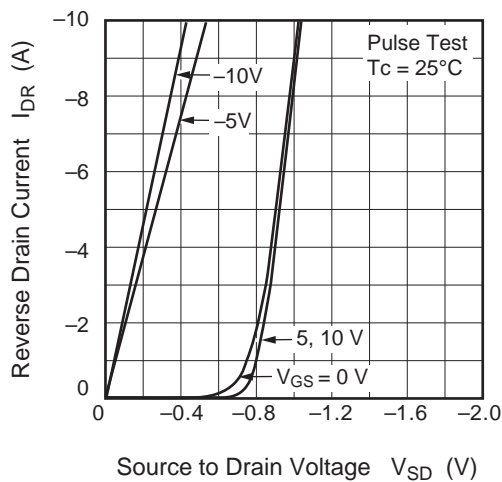
Typical Capacitance vs. Drain to Source Voltage



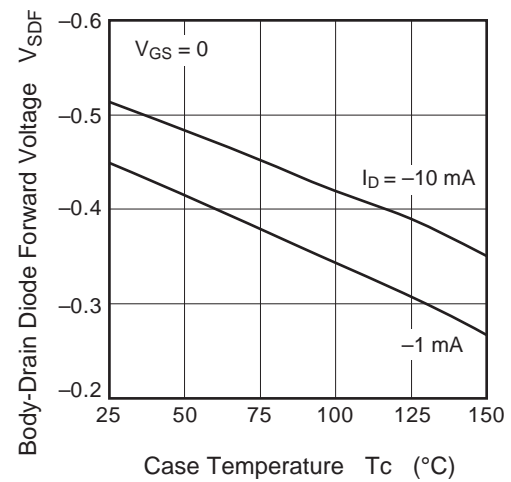
Input Capacitance vs. Gate to Source Voltage



Reverse Drain Current vs. Source to Drain Voltage



Body-Drain Diode Forward Voltage vs. Case Temperature



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