Preliminary

Flyback configuration LED driver with integrated PFC and no feedback

General Description

The IS31LT3929 is a primary side, peak current mode, isolated type HBLED driver. The device works at a constant frequency in discontinuous conduction mode to provide a constant power to the input. It eliminates the need for an opto-coupler, TL431, or any other type of secondary side feedback. It operates from an input voltage range of 85VAC to 265VAC.
The IS31LT3929 integrates over current/voltage protection, as well as includes a thermal shutdown to halt the switching action in the case of abnormally high operating temperatures.

Features

- Power factor correction to > 0.9
- 3% typical current accuracy
- No loop compensation required
- Wide input voltage range: 85V to 265VAC
- Internal over-temperature protection

Applications

- AC/DC constant current LED driver
- General AC/DC power supply
- General LED Lighting

Typical Operating Circuit

Figure 1 Typical Operating Circuit

Pin Configurations

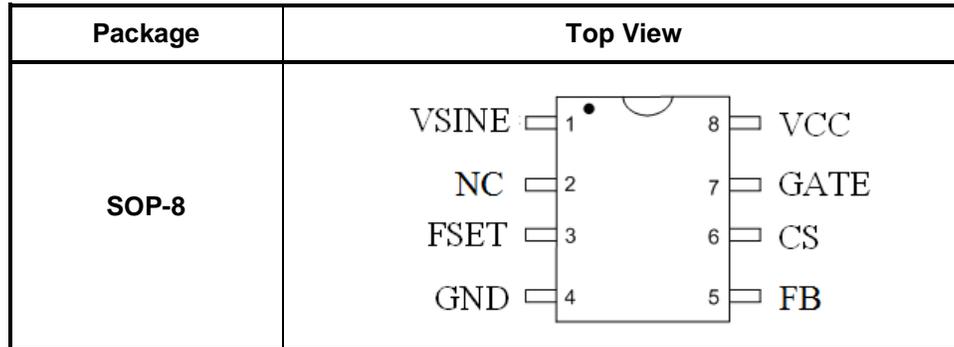| Package	Top View
SOP-8	VSINE ⊏ 1 ● 8 ⊐ VCC NC ⊏ 2 7 ⊐ GATE FSET ⊏ 3 6 ⊐ CS GND ⊏ 4 5 ⊐ FB

Pin Descriptions

Pin	Name	Function
1	VSINE	Line voltage sense input required for PFC.
2	NC	No connect. Must leave floating in the application.
3	FSET	Connect a resistor from this pin to GND to set the operating frequency
4	GND	Ground. Common to all internal circuitry.
5	FB	Auxiliary winding voltage sensing pin for OVP.
6	CS	Primary winding peak current detection input.
7	GATE	Power NMOS gate driving output
8	VCC	Internal circuit power supply input.

Ordering Information

Order Part No.	Package	QTY/Reel
IS31LT3929-GRLS2-TR	SOP-8, Lead-free	2500

Absolute Maximum Ratings

Parameter	Value
VCC to GND	-0.3V to 30V
VSINE, NC, FSET, CS, FB	-0.3V to 5.5V
VCC Max. Input Current*(note)*	10mA
Junction Temperature Range	-40°C to +150°C
Storage Temperature Range	-65°C to +150°C
ESD Human Model	4000V

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(Unless otherwise specified, VCC=16V, FB=0V, VSINE=2.5V, RSET=300KΩ, and T$_{amb}$=25 ^{o}C)

| Symbol	Parameter	Conditions	spec			Unit
			Min	Typ	Max	
Vth_s	VCC start voltage threshold	*VCC rising*	14.5	16	17.5	V
Vth_d	VCC undervoltage threshold	VCC falling	7	8	9	V
Vgate	GATE output voltage clamp value		16	17.5	19	V
Icc	Quiescent Supply Current	Not switching		600		uA
Ist	Startup current	VCC < Vth_s		60		uA
Vcs	Primary peak current control threshold			0.5		V
Tblank	Blanking time			500		ns
Tr	Rise time	CL = 1nF		100		ns
Tf	Fall time	CL = 1nF		50		ns
Vovp_H	OVP rising threshold			1.25		V
Vovp_L	OVP falling threshold			1.0		V
f	Operating frequency	RSET = 300k		50		kHz
Dmax	Maximum duty cycle			50		%
Tre1	Short circuit protection delay	F = 50k		80		ms
Tre2	CS over current protection delay	F = 50k		80		ms

TBD

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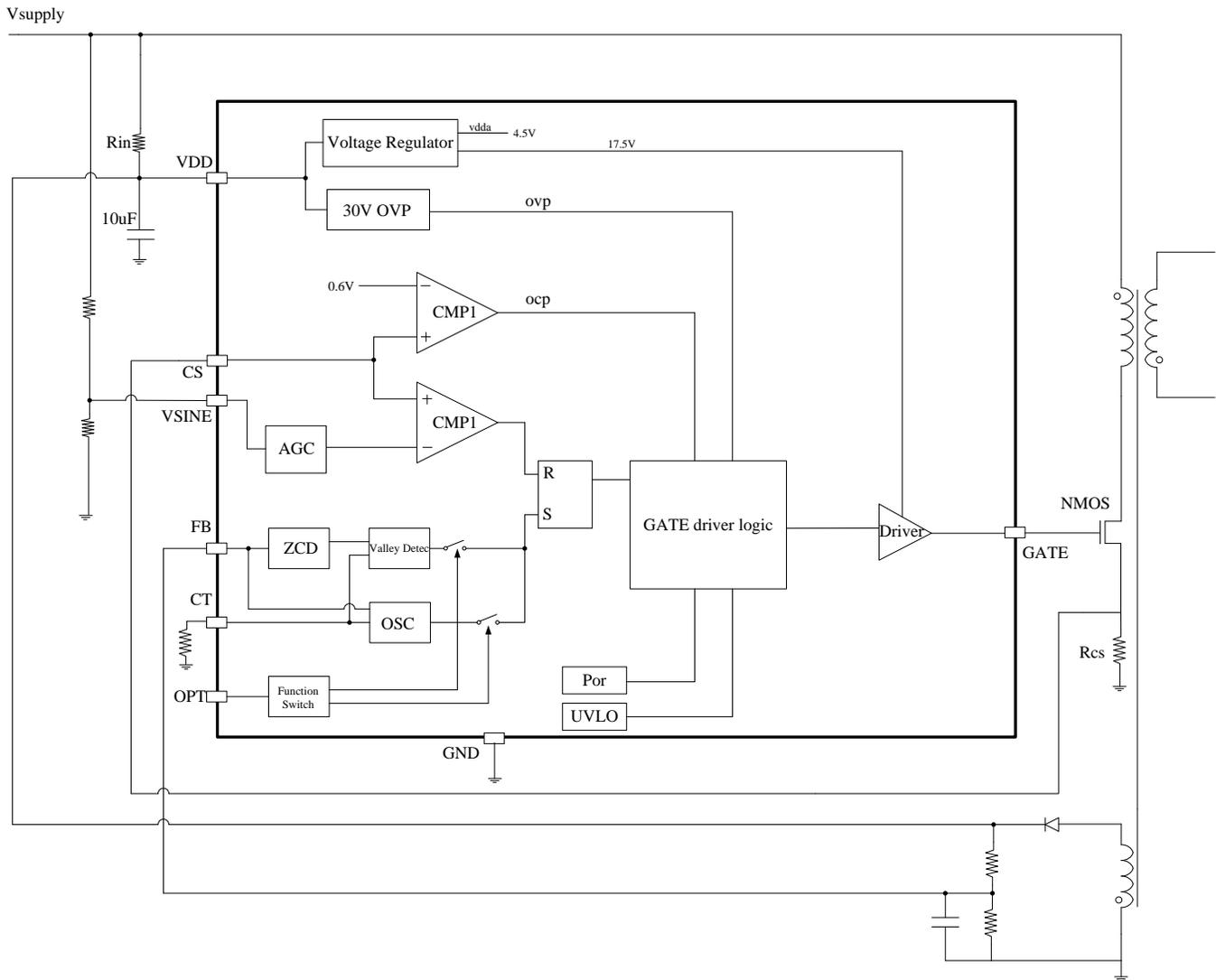
Application Information

Startup voltage

When the VCC pin of the IS31LT3929 reaches 16.5V, the IC is allowed to start.   After power is applied to the circuit, R3 provides a trickle current to allow C4 to begin charging.   The IC starts working when the voltage of C4 reaches the start threshold for the IC. The value of R3 & C4 can be determined by the input voltage.   Larger values of R3 increase the startup time, but reduce the losses after the circuit is running.   A low ESR capacitor of 10uF, 50V is recommended for C4.

VSINE detection network

The input pin, VSINE is used to detect the input voltage which controls the peak current in the inductor. This allows the IS31LT3929 to actively correct the power factor during operation.   The maximum input voltage of the VSINE pin is 2.5V.   This resistor network should be computed such that the peak input voltage condition corresponds to ~2.4VDC.   Thus, for 265VAC, the peak voltage is 374.7V.   At 374.7V input, the output of the network should be 2.4V, thus values of R1=1.56M and R2 = 10k are appropriate.   High tolerance resistors of 1% should be used.   A small, 1nF capacitor, C2, is used to filter high frequency noise.

Working Frequency

The working frequency is set by connecting a resistor between the FSET pin and ground.   The relationship between the frequency and resistance is:

$$f = \frac{15 \times 10^9}{R_{EXT}}$$

Output open circuit protection

Open circuit protection is realized by connecting a resistor network to the FB pin.   By sensing the voltage of the auxiliary winding, which is proportional to the output voltage, the IS31LT3929 detects when there is an open circuit condition on the secondary and stop the switching action.   The threshold voltage for the FB pin is 1.25V.

Output short circuit protection

If the output of the circuit is suddenly shorted, the voltage of the secondary winding is quickly reduced. This in-turn reduces the reflected voltage in the auxiliary winding, so VCC of the device drops rapidly. If the VCC voltage drops below the UVLO, the device will stop switching, thus indirectly achieving output short circuit protection.

UVLO protection

The device will not operate if the VCC voltage is below the under-voltage lockout threshold.
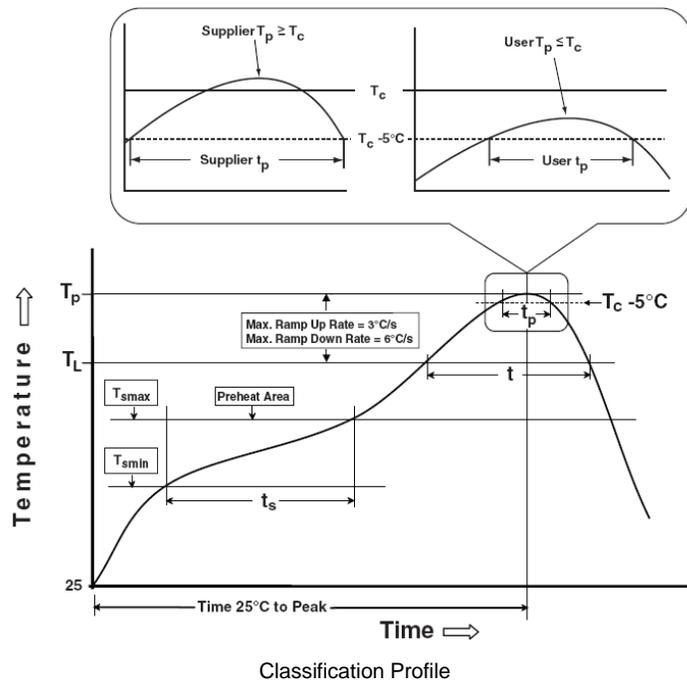
CS pin short circuit protection

If the CS pin is shorted to ground, the device can no longer detect the peak current of the inductor, and thus will quickly cause damage to the power MOS, inductor, or other circuit components.   The maximum duty cycle of the gate is limited to 50% internally to prevent a shorted CS pin from going into current runaway.

PCB design considerations

(1) Components such as R2, R4, R6, R7, etc. which are connected to the IC should be mounted as close to the IC as possible.
(2) Bypass capacitors should always be mounted as close to the IC as possible.
(3) Switching signal traces should be kept as short as possible and not be routed parallel to one another so as to prevent coupling.

Lassification Reflow Profiles

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (Tsmin) Temperature max (Tsmax) Time (Tsmin to Tsmax) (ts)	150°C 200°C 60-120 seconds
Average ramp-up rate (Tsmax to Tp)	3°C/second max.
Liquidous temperature (TL) Time at liquidous (tL)	217°C 60-150 seconds
Peak package body temperature (Tp)*	Max 260°C
Time (tp)** within 5°C of the specified classification temperature (Tc)	Max 30 seconds
Average ramp-down rate (Tp to Tsmax)	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

Classification Profile

Tape and Reel Information

NOTES:
1. CARRIER TAPE COLOR: BLACK
2. COVER TAPE WIDTH:9.50±0.10
3. COVER TAPE COLOR:TRANSPARENT
4. SURFACE ANTISTATIC COATED $10^5 \sim 10^{11}$ OHMS/SQ.
5. 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ±0.20MAX.
6. IN A REEL CARRIER THE THICKNESS CUMULATIVE TOLERANCE ±0.05MAX.
7. CAMBER NOT TO EXCEED 1 MM IN 100 MM〔载带直线弯曲度：≤1mm/100mm.〕
8. MOLD# SOP8
9. ALL DIMS IN mm.
10. THIS TAPE FORBIDS USING BANNED SUBSTANCES OF JCET PRESCRIBING.
11. THE DERECTION OF VIEW:

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Package Information

Package Outline Drawing
#D08

$\frac{5.10}{4.70}$

$\frac{6.20}{5.80}$ $\frac{4.00}{3.80}$

1.27BSC

$\frac{0.25}{0.17}$

$\frac{1.27}{0.40}$

$\frac{8°}{0°}$

$\frac{0.51}{0.33}$

$\frac{0.25}{0.10}$

$\frac{1.55}{1.35}$

$\frac{1.75}{1.35}$