IS31LT3938 Preliminary

High Voltage LED Lighting Driver with Three Level Power Sequencing

General Description

IS31LT3938 LED driver IC is a peak current detection buck converter which operates in constant off time mode. It operates over a very wide input voltage supply range of 10VDC to 450VDC or 110VAC/220VAC.

IS31LT3938 incorporates the special feature of three power sequencing levels by detecting OFF-ON cycles of the main power switch. When the switch is cycled within a 4 second period (typical) the device automatically switches the power level to the next step. As a result, the input and output power of the luminaire may be adjusted depending on the desired amount of illumination and/or power consumption. There are multiple power levels that the engineer may configure, 2 steps or 3 steps, via the external pins DIM1 and DIM2.

IS31LT3938 can also realize LED dimming using an external PWM signal. It can accept a PWM signal from 0% to 100% duty cycle. The LED current may also be adjusted linearly by applying an analog input voltage in the range of 0.5V to 2.5V.

IS31LT3938 adopts a peak current mode control architecture, which eliminates the need for any additional loop compensation while maintaining a good degree of constant output current regulation.

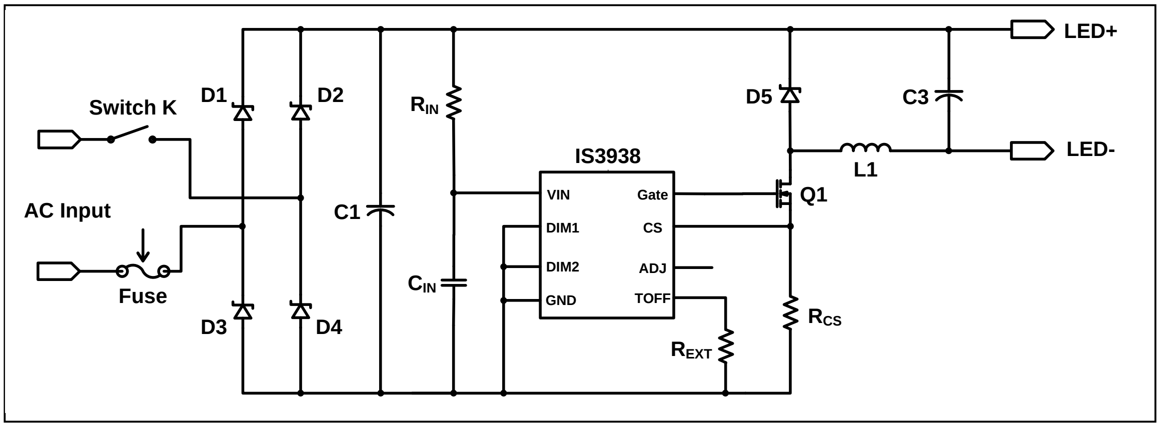
Features

- User configurable power sequencing levels
- 3% output current accuracy
- Over current, temperature protection and short circuit protection
- High efficiency (typical up to 95%)
- Higher MOS drive voltage
- Wide input voltage range: 10VDC~450VDC or 85Vac~ 265Vac
- Linear and PWM dimming
- Very few external components

Applications

- DC/DC or AC/DC constant current LED driver
- Signal and decorative lighting
- Backlight LED driver

Typical Application Circuit



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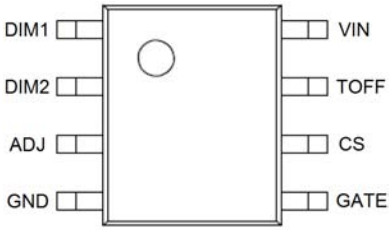
a.) the risk of injury or damage has been minimized;
b.) the user assume all such risks; and
c.) potential liability of Integrated Silicon Solution, Inc is adequately protected under the circumstances

Pin Configuration

Package	Pin Configurations
SOP-8	

Pin Description

Pin Name	Pin Number	Description
DIM1	1	These two pins configure the power sequencing levels as follows: DIM1="floating"DIM2="floating", no dimming (100% only)； DIM1="floating"DIM2="GND" , 100%-30%-100% DIM1="GND"DIM2="floating", 100%-50%-100% DIM1="GND"DIM2="GND", 100%-50%-20%-100%
DIM2	2	
ADJ	3	Linear and PWM dimming input pin. Linear dimming range: 0.5V to 2.5V. If $V_{ADJ} < 0.5V$, GATE output is off. If $0.5V \le V_{ADJ} \le 2.5V$, $V_{CSTH} = V_{ADJ}/10$. If $V_{ADJ} > 2.5V$, $V_{CSTH} = 0.25V$. when the pin is floating, there is an internal pull up to 4.5V (typical) and $V_{CSTH} = 0.25V$. Recommended PWM dimming frequency range: 200Hz -1kHz.
GND	4	Ground pin. All internal currents return through this pin.
GATE	5	This pin connects to the external NMOS's gate
CS	6	Current detect pin, uses an external resistor to sense the peak inductor current.
TOFF	7	This pin sets the off time for the switch by connecting a resistor between this pin and GND.
VIN	8	10V – 450V supply voltage is connected to this pin via an external resistor. It is internally clamped and must be bypassed using a capacitor to GND.

ORDERING INFORMATION

INDUSTRIAL RANGE: -40°C TO +85°C

Order Part No.	Package	QTY/Reel
IS31LT3938–GRLS2-TR	SOP-8, Lead-free	2500

Absolute Maximum Ratings

Parameter	Range	Unit
VIN pin to GND	-0.3 - 13.0	V
DIM1,DIM2,CS, ADJ, GATE, TOFF pin to GND	-0.3 - 6.0	V
VIN pin input current *(Note1)*	10	mA
Operating Junction temperature(T_A=T_J)	-40 - 125	^oC
Junction temperature	-40 - 150	^oC
Device storage temperature	-65 - 150	^oC
ESD（Human Body model）	2000	V

Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Electrical Characteristics

(The specifications are at TA=25°C and V_{INDC}=20V** (Note2)**, R_{IN} =10K, unless otherwise noted) *(Note3)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{INDC}	Input DC supply voltage range	Supply voltage connected to VIN via an appropriate resistor	10		450	V
V_{clamp}	VIN pin clamp voltage		8	9	10	V
UVLO	Undervoltage lockout	VIN falling		7		V
△UVLO	UVLO hysteresis			1.6		V
I_{IN}	Quiescent Current	VIN=V_{clamp}, Gate floating		450	600	uA
$I_{IN,UV}$	Input current in UVLO	VIN= UVLO		200	300	uA
V_{CSTH}	Current sense threshold	ADJ=5V	245	250	255	mV
T_{BLANK}	Current sense blanking time	V_{CS}=V_{CSTH}+50mV		500		ns
TOFF	Off time	R_{EXT}=250KΩ		10		us
V_{ADJ} *(Note 4)*	PWM input voltage high threshold			2.5		V
	PWM input voltage low threshold			0.5		V
	Linear dimming input voltage range		0.5		2.5	V
Tr	GATE rises from 0.1*Vclamp to 0.9*Vclamp	C_{GATE}=1nF		50	80	ns
Tf	GATE falls from 0.9*Vclamp to 0.1*Vclamp	C_{GATE}=1nF		50	80	ns
T_P	Over temperature protection threshold			150		^oC
△T_P	Over temperature protection hysteresis			20		^oC
V_{OCP}	Over current protection CS voltage threshold	ADJ=5V		0.4		V
$TOFF_{\_reset}$	Over current protection TOFF delay time		2.8	4	5.2	ms
T_{MAX}	Maximum switch off time for power level sequencing			4		s

Note1: Beyond the input current range, VIN pin may not clamp at 9V(typical).

Note 2: V_{INDC} is the input voltage. When V_{INDC}>9V, input voltage connected to VIN pin should via a appropriate resistor.

Note 3: Production testing of the chip is performed at 25° C. Functional operation of the chip and parameters specified are guaranteed by design, characterization and process control in other temperature

Note 4: When V_{ADJ}>2.5V, I_{out} is 100% output current. When V_{ADJ}<0.5V, I_{out} is shutdown. When 0.5V ≤V_{ADJ}≤2.5V, I_{out} is linear dimming.

Application Information

IS31LT3938 is a peak current control LED driver IC. It does not require any high side current sensing nor the design of any closed loop control, yet provides a very accurate constant LED drive current. IS31LT3938 includes an input allowing either a PWM or an analog dimming signal.

An external resistor connected to the TOFF pin determines the internal oscillator's constant off time. The off time adds to the on time, controlled by the internal switching control logic, to set the oscillation frequency. The inductor current increases when the switch is on. This current also flows through the external current sense resistor R_{CS}, and when the voltage across R_{CS} reaches the current sense threshold, V_{CSTH} or 1/10 of the ADJ input voltage, whichever is lower, the switch turns off. The current through the inductor will continue to flow through the LEDs, but will decrease linearly during the switch off time. After the programmed off-time, the switch will turn on again. A short blanking time of 500ns (typical) is implemented to block the voltage spike encountered across R_{CS}, caused by the parasitic capacitance of the switch discharging. After the blanking time the control logic again compares the CS input voltage to the current sense threshold.

Choose the acceptable level of ripple current coefficient, K, then calculate the value of the current sense resistor:

$$R_{CS} = \frac{V_{CSTH}}{(1+K/2)I_{LED}}$$

V_{CSTH}: If $V_{ADJ} < 0.5V$, GATE output is off.
If $0.5V \le V_{ADJ} \le 2.5V$, $V_{CSTH} = V_{ADJ}/10$.
If $V_{ADJ} > 2.5V$, $V_{CSTH} = 0.25V$.
When ADJ pin is floating, there is an internal pull up to 4.5V (typical) and $V_{CSTH} = 0.25V$.

K: acceptable current ripple coefficient, the recommended value range is 1~1.8。

A constant off-time peak current control scheme can easily operate at duty cycles greater than 0.5 and also gives inherent input voltage rejection making the LED current almost insensitive to input voltage variations.

Input Voltage Regulation

The VIN pin is internally clamped to 9V (typical). When supplying a voltage larger than 9V, an external resistor must be used between the input voltage and the VIN pin. Bypass the VIN pin using a low ESR capacitor to provide a high frequency path to GND. The current required by the device is 0.45mA plus the switching current of the external switch. The switching frequency of the external NMOS affects the amount of current required, as does the NMOS's gate charge requirement (found on the NMOS data sheet).

$$I_{IN} \approx 0.45mA + Q_G \cdot f_S$$

In the above equation, f_S is the switching frequency, Q_G is the external NMOS gate charge (from the NMOS datasheet).

Current Detection

The CS pin input voltage is internally provided to 2 comparators. One of the comparators uses an internal 250mV reference, while the other uses a scaled value of the ADJ pin voltage. The outputs of the comparators are ORed, thus causing the lower of the 2 thresholds to trigger the switch control logic. At the moment the switch control logic changes the gate signal to low, the TOFF timer is started. The external switch will remain off for the length of time programmed, and once the TOFF time is expired, the switch control logic again toggles the gate signal, this time from low to high, and the external switch turns on. As the external switch turns on, the parasitic capacitance on the drain of the switch must discharge through the switch channel causing a spike of current which can be quite large, but only lasts for a very short period of time. To prevent this current from causing a false triggering of the current sense comparators, the signal is blocked from the internal comparators for 500ns (typical). In some special cases, the 500ns blanking time may not be sufficient to prevent false triggering of the CS threshold logic. Under these circumstances, an additional RC filter may be added to the CS input pin to help filter the voltage spike. Careful layout of the PCB to minimize parasitic capacitance, trace resistance and inductance greatly aid in the elimination of false triggering.

Oscillator

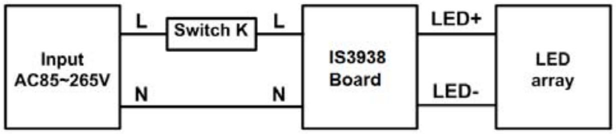
IS31LT3938's TOFF pin controls the off time of the internal oscillator. Oscillator off time is determined by the following equation:

$$Toff\,(s) = 40 \times 10^{-12} \times R_{EXT}$$

R_{EXT}： resistor connected between TOFF and GND

Switchable Power Levels

IS31LT3938 detects the external switch action of the main power switch, and can automatically adjust the level of the output current based on the action of the main power switch.



The action of the external power switch can be divided into two types. The first is "normal switch operation" wherein the switch is toggled from ON to OFF, remaining OFF for longer than 4 seconds (typical). The other is "power sequencing action" wherein the switch is toggled from ON to OFF and back ON within 4 seconds (typical).

When the device experiences normal switch operation, it merely powers on in the first state, 100%, when the power switch is toggled to ON, and the device turns off when the external power switch is changed to OFF.

Power sequencing output current levels are configured by connecting the DIM1 and DIM2 pins as indicated in the table below：

DIM1	DIM2	Power sequencing levels
Floating	Floating	No Power Sequencing
Floating	GND	2 levels：100%-30%-100%
GND	Floating	2 levels：100%-50%-100%
GND	GND	3 levels：100%-50%-20%-100%

When operating the power switch normally the device will always power up at 100% output current.

The operation of the power switch and the configuration of the DIM1 and DIM2 pins control the power sequencing process as follows：

1. When DIM1 and DIM2 pins are both floating, there is no switchable power levels, and the output current is 100% of the programmed value when the power is on.
2. When DIM1 is floating and DIM2 is GND, the output current is：
    a) 100% at power on.
    b) The first power sequencing action causes the current to change to 30%.
    c) A second power sequencing action causes the current to return to 100%.
    d) A third power sequencing action has the same effect as the first power sequencing action.
    e) Subsequent power sequencing actions causes the cycle to continue.
3. When DIM1 is GND and DIM2 is floating, the dimming sequence is as described in (2) above, except that the current sequence is 100%-50%-100%.
4. When both DIM1 and DIM2 are connected to GND, the dimming sequence is as described in (2) above, except that the current sequence is 100%-50%-20%-100%.

If the switch is operated normally, that is, switched on once after being in the OFF position for a long time, or if both the DIM1 and DIM2 pins are floating, then the output current always starts up at the initial value of 100%.

Note: Because the main power switch is used to initiate the power sequencing function, the device must have a large enough external capacitor on VIN to maintain device operation for 4 seconds.

Linear Dimming

An external voltage, 0.5V to 2.5V, connected to the ADJ pin can adjust the LED current. Two possible situations where this might be used are：

If it is not possible to change the value of R_{CS} to obtain the desired value of LED current, an external voltage reference can be connected to the ADJ pin to adjust the voltage sense level across R_{CS}, equivalent to changing the value of R_{CS}.

Connecting a resistor between the VIN and ADJ pin, then connecting a thermistor from the ADJ pin to GND can adjust the LED current based on temperature, thus realizing the temperature compensation feature.

PWM Dimming

PWM dimming may be realized by applying a low frequency PWM waveform to the ADJ pin. When the PWM signal is low, less than 0.5V, the IS31LT3938 remains off；When the PWM signal is high, greater than 2.5V, the driver is enabled and operates normally. The PWM signal does not shut down other circuit blocks of the device, thus the response to the PWM signal is relatively fast, and primarily determined by the rise and fall time of the inductor current.

To disable PWM dimming, leave the ADJ pin floating.

Application Example

Input Voltage：V_{in} = 220V DC

Output：Vo=40V（12 x 1W LEDs in series, Vf=3.3V）
I_{LED}=0.35A
No Power sequencing levels

1. VIN power supply circuit

VIN supply current is given by:

$$I_{IN} \approx 0.45mA + Q_G \cdot f_s$$

Assuming I_{IN}=1mA,

then $R_{IN} = \frac{Vin - VIN}{I_{IN}} \approx \frac{220-9}{1} = 211K\Omega$

Choose two 430KΩ/0.5W in parallel for the resistor lifetime consideration.
Choose C_{IN}: 10uF/25V ceramic capacitor.

2. Constant off time（TOFF）

Off time is given by：

$$Toff\,(s) = 40\times 10^{-12}\times R_{EXT}$$

To decide the off time, assume the desired switching frequency is 50kHz(period time T=20uS), and the duty cycle: $D = \frac{Vo}{Vin} = \frac{40}{220} = 18.18\%$
the duty cycle is decided by the ratio of the output voltage and input voltage, then TOFF:
$TOFF = T\times(1-D) = 20uS\times(1-18.18\%) = 16.36uS$,
so R_{EXT} =409KΩ, choose the closest resistor, R_{EXT} =390KΩ, the actual TOFF=15.6uS(Because the actual TOFF is smaller than theoretical TOFF, the operating frequency will be little higher than 50KHz).

3. Current Sense Resistor（R_{CS}）

The ripple current: $I_{RIPPLE} = K\times I_{LED}$, K is the ripple current coefficient, the recommended value range is 1~1.8.
The peak current :

$$I_{PEAK} = I_{LED} + \frac{I_{RIPPLE}}{2} = \left(1+\frac{K}{2}\right)\times I_{LED}$$

Because of ADJ pin floating, V_{CSTH}=0.25V. Assuming a typical value for K of 1.8.
The current sense resistor is given by：

$$R_{CS} = \frac{V_{CSTH}}{I_{PEAK}} = \frac{V_{CSTH}}{\left(1+\frac{K}{2}\right)I_{LED}} = \frac{0.25}{\left(1+\frac{1.8}{2}\right)\times 0.35} = 0.376\Omega$$

Choose R_{CS}=0.38Ω and 1% precision.

4. Inductor（L1）

The inductance of inductor L1 is dependent on the LED current, in this case 350mA. We have already chosen TOFF=15.6uS, thus:

$$L = \frac{V_O\times T_{OFF}}{I_{Ripple}} = \frac{V_O\times T_{OFF}}{K\times I_{LED}} = \frac{40\times 15.6\times 10^{-6}}{1.8\times 0.35} \approx 1mH$$

Where I_{ripple} is the design target for ripple current.
Note: The saturation of inductor must be higher than the peak current.

5. Freewheeling diode (D5) and NMOS (Q1)

Choose Q1 to have a voltage rating at least as large as the peak voltage of the maximum input voltage with approximately 50% margin.

$$V_{NMOS} = 150\%\times\sqrt{2}\times Vin$$

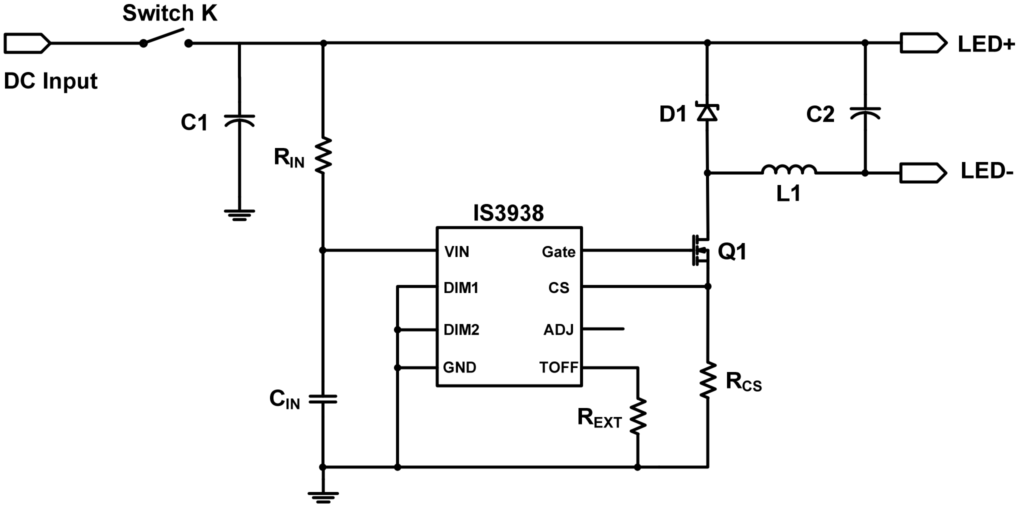
The current through the NMOS is based on the peak LED current, choose FET current rating with 50% margin.

$$I_{NMOS} = 150\%\times I_{PEAK}$$

Thus, choose 600V, 2A, NMOS, such as: 2N60

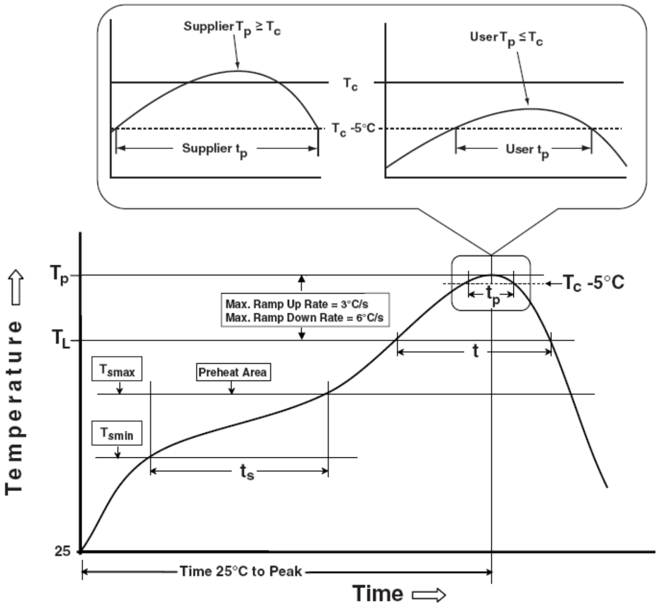
The diode ratings are equal to that of the NMOS, Q1.
Note: The diode must be a superfast recovery diode and the Reverse Recovery Time (T_{RR}) should be less than 50nS. Thus, choose 600V, 1A, superfast recovery diode, such as: ES1J, SF18

Appendix: Typical application circuit of DC voltage input


Switch K
DC Input
C1
RIN
CIN
IS3938
VIN
DIM1
DIM2
GND
Gate
CS
ADJ
TOFF
REXT
D1
C2
L1
Q1
RCS
LED+
LED-

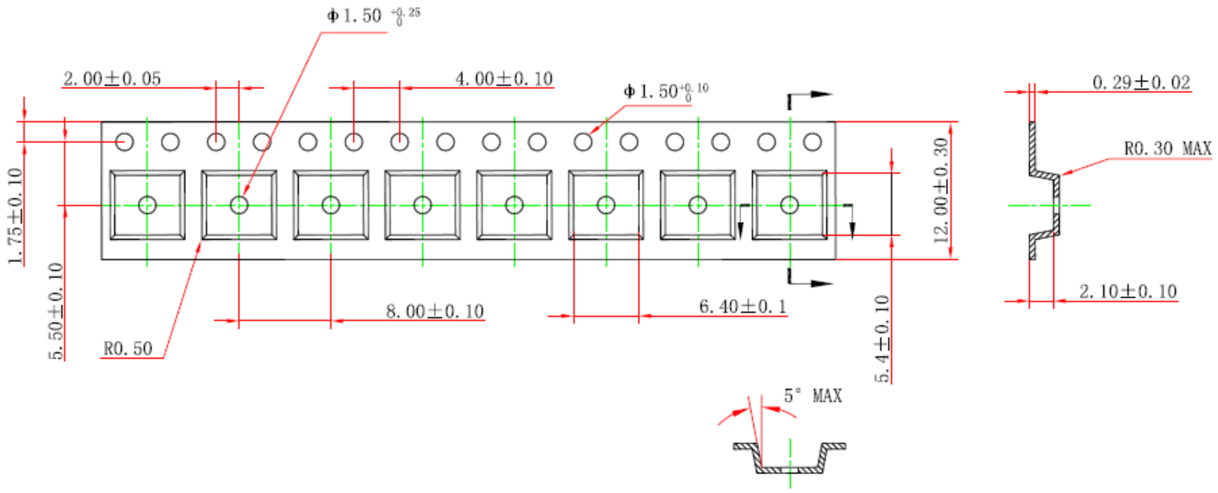
Classification Reflow Profiles

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (Tsmin) Temperature max (Tsmax) Time (Tsmin to Tsmax) (ts)	150°C 200°C 60-120 seconds
Average ramp-up rate (Tsmax to Tp)	3°C/second max.
Liquidous temperature (TL) Time at liquidous (tL)	217°C 60-150 seconds
Peak package body temperature (Tp)*	Max 260°C
Time (tp)** within 5°C of the specified classification temperature (Tc)	Max 30 seconds
Average ramp-down rate (Tp to Tsmax)	6°C/second max.
Time 25°C to peak temperature	8 minutes max.


Supplier $T_p \geq T_c$
User $T_p \leq T_c$
T_c
T_c -5°C
Supplier t_p
User t_p
T_p
T_L
T_c -5°C
t_p
Max. Ramp Up Rate = 3°C/s
Max. Ramp Down Rate = 6°C/s
t
T_{smax}
Preheat Area
T_{smin}
t_s
25
Temperature
Time 25°C to Peak
Time

Classification Profile

Tape and Reel Information


Φ1.50 +0.25/-0
2.00±0.05
4.00±0.10
Φ1.50 +0.10/-0
0.29±0.02
R0.30 MAX
1.75±0.10
5.50±0.10
12.00±0.30
R0.50
8.00±0.10
6.40±0.1
2.10±0.10
5.4±0.10
5° MAX

NOTES:[技术要求]:

1.CARRIER TAPE COLOR:BLACK[载带颜色为黑色]

2.COVER TAPE WIDTH:9.50±0.10 [配套9.5宽盖带]

3.COVER TAPE COLOR:TRANSPARENT[盖带颜色无色透明]

4. SURFACE ANTISTATIC COATED $10^5 \sim 10^{11}$ OHMS/SQ.
[单位面积表面阻抗$10^5 \sim 10^{11}$ Ω/□]

5.10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ±0.20MAX.
[10个传送定位孔间距累积公差0.20MAX.]

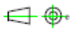
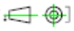
6. IN A REEL CARRIER THE THICKNESS CUMULATIVE TOLERANCE ±0.05MAX.
[在同一卷中载带厚度公差范围不得超过0.05mm]

7.CAMBER NOT TO EXCEED 1 MM IN 100 MM[载带直线弯曲度：≤1mm/100mm.]

8.MOLD# SOP8[载带规格SOP8]

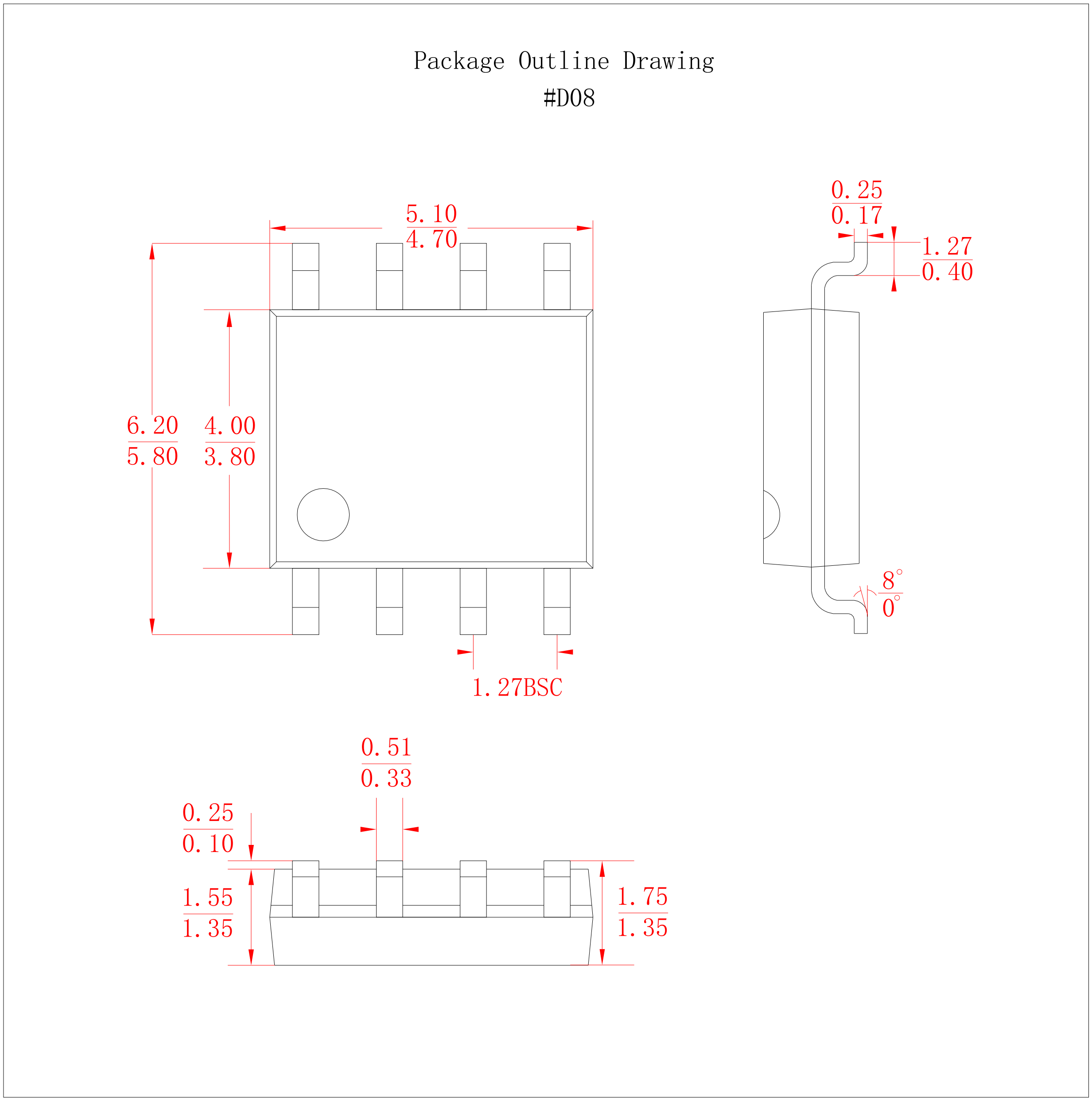
9.ALL DIMS IN mm.[所有单位为mm]

10.THIS TAPE FORBIDS USING BANNED SUBSTANCES OF JCET PRESCRIBING.
[禁止使用长电科技规定的一级环境管理物质]

11.THE DERECTION OF VIEW: . [视图方向: ]

Package Information

SOP-8


Package Outline Drawing
#D08
5.10
4.70
6.20
5.80
4.00
3.80
1.27BSC
0.25
0.17
1.27
0.40
8°
0°
0.51
0.33
0.25
0.10
1.55
1.35
1.75
1.35